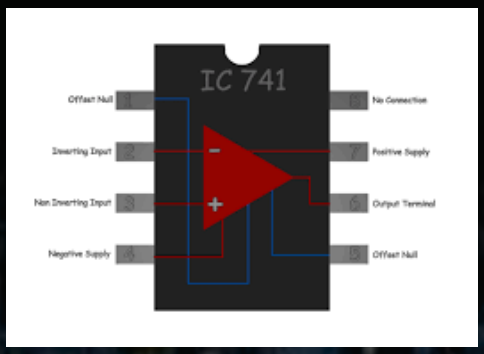
ELECTRONIC DEVICES AND ANALOG ELECTRONICS

Specially Designed for GATE Examination



VOLUME II

by Ram Niwas (IES)

ELECTRONIC DEVICES AND ANALOG ELECTRONICS

VOLUME II

First Edition

2021

ELECTRONIC DEVICES AND ANALOG ELECTRONICS

VOLUME II

RAM NIWAS, IES

B.E. (NIT, Nagpur), M.E. (DCE, Delhi), Ph.D. (IIT, Delhi)

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CONTENTS

HOW TO READ THIS BOOK

This book has been designed to meet the requirement of all Electrical, Electronics and Instrumentation Engineers. It is has been written in simple and lucid language so that students from all backgrounds, having little knowledge of English, can understand. It is designed to develop facts and concepts for competitive examinations in India like GATE, IES, PSUs and IAS examinations. The book can be referred for University Syllabus across different countries in the world. Every chapter is followed and prepared after in depth analysis of previous year questions which appeared in these competitive examinations. The focus is mainly on developing concepts along with facts. Each chapter has been followed by previous years fully solved questions of GATE of Electronics, Electrical and Instrumentation Engineering. These questions are helpful for university examination also.

For students studying in B.E./B.Tech

This book would help students studying in B.Tech to prepare for their university examination. In parallel book is equipped to prepare B.Tech students for competitive examinations like GATE and ESE. However, main focus of students of B.Tech should be to develop concepts and then practice question of GATE.

For students preparing for GATE

The theory of this book has been prepared to develop theoretical concepts for those students who are preparing for GATE. Such students should focus on theoretical concepts followed by practicing previous year GATE questions which are given at the end of each chapter along with full solutions. Students first try to solve the question themselves and the refer the solution.

For students preparing for ESE Preliminary

The theory of this book has been prepared for students preparing for ESE both Electrical and Electronics Preliminary and Mains Examinations and IAS Electrical mains examination. However, students preparing for ESE Pre examination should note down factual information and formulas in their notebook in form of brief notes. It helps in quick revision just before the Pre examination. Each chapter has been provided with fully solved questions of ESE Pre for both EE and EC. Students should practice these questions in time bound manner with one question in one minute. It would help to build speed and accuracy. Solutions should be referred only to clarify doubt if any.

For students preparing for ESE Mains and IAS Mains

The students preparing for ESE Mains of EE and EC or IAS Electrical mains should practice questions from all these examination so that they have enough practice questions. However, solutions of these question will be provided in next edition of this book. Such students should not wast much time on reading theory in whole they should relevant portion which are important for mains examination as they have already studied the whole theory while preparing for preliminary stage.

PREFACE TO FIRST EDITION

Chapter 1

Chapter 1 introduces different circuits of diodes. It presents clipping circuits, clamping circuits, peak detectors, rectifiers and zener voltage regulator. This chapter is very important for almost all the competitive examinations including GATE & ESE for students of Electronics, Electrical as well as Instrumentation Engineering. There are questions from this chapter almost every year in GATE and Engineering services Examinations.

Chapter 2

Chapter 2 presents different biasing circuits of BJT and its thermal stabilization. Different circuits has been presented on the basis of the circuits which appearing in examinations. The focus on topics which are important for different competitive examinations. It is an important topic for GATE, ESE and PSU examinations. There are frequent questions from this topic in competitive examinations of Electronics, Electrical and Instrumentation Engineering students.

Chapter 3

Chapter 3 presents different biasing circuits of MOSFETs and JFETs. This topic is important for students of Electronics Engineering special for GATE examination. Various circuits of MOSFET have been covered on the basis of questions which appeared in different competitive examinations.

Chapter 4

Chapter 4 presents the small signal analysis of BJT amplifiers. This an important topic for GATE as well as ESE mains examinations of students from Electronics and Electrical Engineering. There are frequent questions in GATE of Instrumentation Engineering as well, form this topic.

Chapter 5

Chapter 5 presents the small signal analysis of MOSFET amplifiers. This an important topic for GATE specially for students of Electronics Engineering. There topic will be important for future GATE examinations because of increased practical applications of MOSFET.

Chapter 6

Chapter 6 presents frequency response of BJT and MOFETs. It covers both low frequency as well

as high frequency responses of these devices. This is an important topic for GATE examinations of Electronics Engineering and ESE pre examination.

Chapter 7

Chapter 7 presents multistage amplifiers and their frequency response. There were few questions from frequency response of multistage amplifiers in GATE as well as ESE pre in Electronics Engineering. However, there can be one mark question in GATE, ESE pre and PSU examinations from this topic.

Chapter 8

Chapter 8 presents compound configurations of BJT and MOSFET which includes Darlington Pari, Cascase and Cascode connection and current mirrors. There are frequent question especially from current mirror in GATE examination of Electronics, Electrical and Instrumentation Engineering. It is an important topic of ESE and IAS examinations also.

CHAPTERWISE GATE SYLLABUS

S.N.	Topic	Electronics & Comm. Engineering	Electrical Engineering	Instrumentation Engineering
Ch.1	Semiconductors	Energy bands in intrinsic and extrinsic semiconductors, equilibrium carrier concentration, direct and indirect band-gap semiconductors, Carrier transport: diffusion current, drift current, mobility and resistivity, generation and recombination of carriers, Poisson and continuity equations		
Ch.2	Diodes	P-N junction, Zener diode, LED, photo diode and solar cell		Characteristics and applications of diode, Zener diode
Ch.3	Bipolar Junction Transistors	BJT		Characteristics and applications of BJT
Ch.4	Field Effect Transistors	MOSFET & MOS Capacitor		Characteristics and applications of MOSFET
Ch.5	Diodes Circuits	Diode circuits: clipping, clamping and rectifiers.	Simple diode circuits: clipping, clamping, rectifiers	
Ch.6	BJT Biasing & Thermal Stabilization	BJT amplifiers: biasing	Amplifiers: Biasing	
Ch.7	MOSFET Biasing	MOSFET amplifiers: biasing	Amplifiers: Biasing	
Ch.8	Small Signal Analysis of BJT	BJT amplifiers: ac coupling, small signal analysis	Amplifiers: Equivalent circuit	small signal analysis of transistor circuits
Ch.9	Small Signal Analysis of FET	MOSFET amplifiers: ac coupling, small signal analysis	Amplifiers: Equivalent circuit	small signal analysis of transistor circuits

Chap.	Topic	Electronics & Comm. Engineering	Electrical Engineering	Instrumentation Engineering
Ch.-10	Frequency Response	BJT and MOSFET amplifiers : frequency response	Amplifiers: Frequency response	
Ch.11	Multistage Amplifiers			
Ch.12	Compound circuits	BJT and MOSFET amplifiers : Current mirror		
Ch.13	Feedback Amplifiers		Feedback amplifiers	Feedback amplifiers
Ch.14	Differential Amplifiers	BJT and MOSFET amplifiers : differential amplifiers.	BJT and MOSFET Differential Amplifiers	
Ch.15	Operational Amplifiers & its circuits	Op-amp circuits: Amplifiers, summers, differentiators, integrators, active filters, Schmitt triggers and oscillators.	operational amplifiers: characteristics and applications; single stage active filters, Sallen Key, Butterworth, VCOs and timers	Characteristics of ideal and practical operational amplifiers; applications of opamps: adder, subtracter, integrator, differentiator, difference amplifier, instrumentation amplifier, precision rectifier, active filters, oscillators, signal generators, voltage controlled oscillators and phase locked loop, sources and effects of noise and interference in electronic circuited oscillators and phase locked oscillators, signal generators, voltage controlled oscillators and phase locked loop.
Ch.16	Oscillators		Oscillators	
Ch.17	Power Supplies			
Ch.18	Power Amplifiers			

CHAPTERWISE ANALYSIS OF GATE QUESTIONS

Electronics and Communication Engineering : EDC & Analog Electronics

Chap	Topic	2010	2011	2012	2013	2014				2015			2016			2017		2018	2019	2020	2021
						IV	III	II	I	III	II	I	III	II	I	II	I				
Ch.1	Semiconductors	4	1			7	2	3			6	1		2	5		5			1	2
Ch.2	Diodes	2	2		1		3		4			5	4	4	2	4	3	12	10	5	2
Ch.3	BJT and Its Characteristics	2	2			2		1	2	3			2	1		1	1		1	2	
Ch.4	FET and Its Characteristics	2	6	8	5		7	5	4	5	2	4	3	5	4	8	2	3	3	2	2
Ch.5	Diode circuits		4	3	4	1		2	1	3	3	1	3	2		1			5	1	2
Ch.6	Biasing of BJT		2		2		3	1		1			1			1	2				
Ch.7	Biasing of MOSFET																			2	2
Ch.8	Small Signal Analysis of BJT	2		1		7			2		2		4			2	2			2	
Ch.9	Small Signal Analysis of FET	2		1		7			2		2		4			2	2			2	1
Ch.10	Frequency Response	4															1				
Ch.11	Multistage Amplifiers							1						1							
Ch.12	Compoud circuits	1												1					4		
Ch.13	Feedback Amplifiers			2	1		1	1	1								1	1			
Ch.14	Differential Amplifiers							1				2									
Ch.15	Operational Amplifiers & its circuits	3	1	2	3	2	2		6	3	6	4	3	4	8	2	3	4		4	4
Ch.16	Oscillators																				
Ch.17	Power Supplies																			2	
Ch.18	Power Amplifiers																				
	Total Marks	**22**	**18**	**14**	**16**	**26**	**18**	**19**	**22**	**15**	**21**	**17**	**24**	**20**	**19**	**21**	**22**	**20**	**23**	**23**	**15**

Electrical Engineering : EDC & Analog Eectronics

Chap	Topic	2010	2011	2012	2013	2014				2015			2016			2017		2018	2019	2020	2021
						IV	III	II	I	III	II	I	III	II	I	II	I				
Ch.1	Semiconductors																				
Ch.2	Diodes																			2	
Ch.3	BJT and Its Characteristics										1									1	
Ch.4	FET and Its Characteristics																		1	2	
Ch.5	Diode circuits		2	2	4			2			2				3						4
Ch.6	BJT Biasing		2	2							1	1			1	2		2	2	2	1
Ch.7	FET Biasing																				
Ch.8	Small Signal Analysis of BJT									1										1	
Ch.9	Small Signal Analysis of FET																				
Ch.10	Frequency Response of BJT & MOSFET																				
Ch.11	Multistage Amplifiers																				
Ch.12	Compoud circuits																				
Ch.13	Feedback Amplifiers			2	1														1		
Ch.14	Differential Amplifiers																2			2	
Ch.15	Operational Amplifiers & its circuits	1	1	4	3		3	2	3		4	4		3		2	2		2		2
Ch.16	Oscillators																				
Ch.17	Power Supplies																			2	
Ch.18	Power Amplifiers																				
	Total Marks	**1**	**5**	**10**	**8**		**3**	**4**	**5**	**1**	**8**	**5**		**3**	**4**	**4**	**4**	**2**	**6**	**12**	**7**

Instrumentation Engineering : EDC & Analog Eectronics																
Chap	**Topic**	**2010**	**2011**	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**	**2018**	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**
Ch.1	Semiconductors															
Ch.2	Diodes and theirs circuits							3	2		1					
Ch.3	BJT & Its Characteristics															
Ch.4	FET Characteristics and its biasin						2		2							
Ch.5	Diodes Circuits		2	2	4	1	1		1	1	1	3				
Ch.6	BJT Biasing				1	4	2									
Ch.7	FET Biasing															
Ch.8	Small Signal Analysis of BJT		1		1		2				2					
Ch.9	Small Signal Analysis of FET															
Ch.10	Frequency Response of BJT & MOSFET															
Ch.11	Multistage Amplifiers															
Ch.12	Compound circuits	2									2		3			
Ch.13	Feedback Amplifiers															
Ch.14	Differential Amplifiers															
Ch.15	Operational Amplifiers	7	11	2	12	8	4	15	8	7	3		5			
Ch.16	Oscillators								1			9				
Ch.17	Power Supplies															
Ch.18	Power Amplifiers															
Ch.19	Tuned Amplifiers															
Ch.20	Multivibrators															
	Total Marks	**9**	**14**	**4**	**18**	**13**	**11**	**18**	**14**	**8**	**9**	**12**	**8**			

Ch 1 Diode Circuits

1.1 Diode as Circuit Element

When a diode is used as a circuit component it behaves like an uncontrolled switch. Ideally a diode behaves like a closed switch when it is forward biased and it behaves like an open switch when it is reverse biased. However, a diode may be represented by its equivalent circuit with different diode models.

1.1.1 Equivalent Circuit of an Diode for DC signals

The diodes are replaced by their equivalent circuit in diode circuits depending upon the biasing condition of the diode. The diodes equivalent circuit for different diode models are presented as under,

1. Ideal Diode

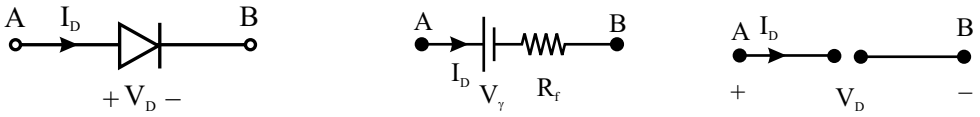
An ideal diode behaves as short circuit when it is forward biased with $V_D > 0$ and open circuit when it is reverse biased with $V_D < 0$ as shown in Fig. 1

(a) Ideal diode (b) Biased with $V_D > 0$ (c) Biased with $V_D < 0$

Fig.1 Equivalent circuits of an ideal diode under forward and reverse biased conditions

2. Piecewise Linear Model

The piecewise linear model represents a battery in series with a resistance (R_f) called forward resistance, when voltage across the diode is more than cut-in voltage (V_γ) of the diode and it acts as an open circuit when voltage across the diode is less than cut in voltage of the diode as shown below.

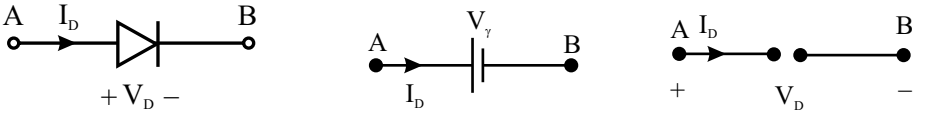


(a) Diode as circuit element (b) Biased with $V_D > V_\gamma$ (c) Biased with $V_D < V_\gamma$

Fig.2 Equivalent circuit of piece wise linear model of diode under different biasing conditions

3. Simplified Model

A diode in simplified model is represented by a battery when voltage across the diode is more than the cut-in voltage (V_γ) of the diode and it acts as an open circuit when voltage across the diode is less than cut in voltage as shown below.



(a) Diode as circuit element (b) Biased with $V_D > V_\gamma$ (c) Biased with $V_D < V_\gamma$

Fig.3 Equivalent circuit of simplified model of diode under different biasing conditions

1.2 Clipping Circuits

Clipping circuits are used for clipping a part of a waveform which lies above or below a reference voltage level. The clipping circuits can be used to clip waveforms at one or two reference levels. The clipping circuit which clips a waveform at one reference level is called one level clipper and one which clips at two reference levels is called two level clipper. The clipper which clips the waveform above a reference level is called positive level clipper and one which clips below a reference level is called a negative level clipper. While studying the clipping circuits only two cases will be discussed with diode in 'ON' condition and diode in 'OFF' condition. The diode will be considered 'ON' when voltage across the diode, $V_D > V_\gamma$, and it is considered 'OFF' when $V_D < V_\gamma$. The cut-in voltage, V_γ = 0, for an ideal diode. The diodes used in clipping circuits in the following sections will be considered ideal diodes and input signals are considered to be sinusoidally time varying.

1.2.1 One Level Clipper with Shunt Connected Diode

These are the circuits in which diode is connected in shunt with the load. The reference voltage source is connected in series with diode and this combination is connected in shunt with the load. One level clippers can be positive and negative level clippers which are further subdivided in to two sub category each with positive and negative reference voltages. All possible one level clippers with shunt connected diode are discussed as follows,

Circuit 1: Positive Level Clipper Circuits with Positive Reference

A positive level clipper with positive reference voltage consisting of a shunt branch with a reference voltage source in series with an ideal diode connected across the load is shown in Fig.4. The reference voltage is positive if its polarity matches with polarity of input voltage. It can be seen from the circuit of Fig. 4 that negative terminal of reference voltage source is common with negative terminal of input voltage so the reference voltage is called positive reference. The analysis of clipping circuits will be done by taking OFF condition of diode followed by ON condition for ease of understanding the operation of the circuit which is discussed in the following two cases.

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 5. As the diode D is ideal so it behaves like an open circuit when it is OFF. The diode D is off when voltage across the diode negative i.e. $V_D < 0$. If a KVL is applied in input loop of the circuit as shown below with diode in open circuited condition then the voltages, V_{in}, V_D and V_R are related as under,

$$V_{in} - V_D - V_R = 0 \quad (1)$$

One point should be noted here that the voltage drop across the resistance R is not considered while applying KVL in input loop because the current in R is zero when diode is open circuited, therefore, voltage drop across R is zero.

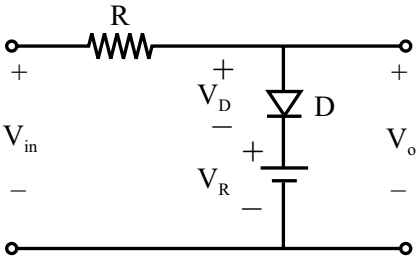


Fig.4 Shunt diode positive level clipper circuit with positive reference voltage

$$\Rightarrow \quad V_D = V_{in} - V_R \quad (2)$$

The diode D is off if, $V_D < 0$ (3)

$$\Rightarrow \quad V_{in} - V_R < 0 \quad (4)$$

$$\Rightarrow \quad V_{in} < V_R \quad (5)$$

Under open circuited condition of the diode, the current through resistance R is zero, so voltage drop across R is zero and the output voltage becomes same as input voltage.

$$\therefore \quad V_o = V_{in} \quad (6)$$

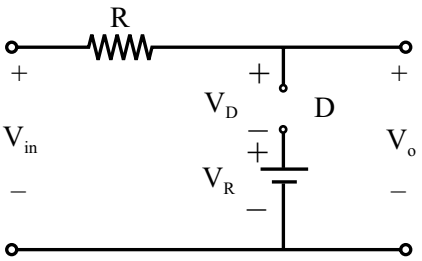


Fig.5 Equivalent circuit of positive level clipper circuit with positive reference voltage and $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig. 6. As the diode D is ideal so it behaves like a short circuit when it is ON. When diode is in OFF condition the voltage across the diode is given by equation (2). The diode will turn ON from OFF only at the instant when V_D becomes more than zero.

The diode D turns on ON when,

$$V_D > 0 \quad (7)$$

$$\Rightarrow \quad V_{in} - V_R > 0 \quad (8)$$

$$\Rightarrow \quad V_{in} > V_R \quad (9)$$

Under short circuited condition of the diode, the battery with reference voltage V_R is directly

connected across the output terminals so the output voltage becomes equal to V_R. Thus when the input voltage is greater V_R, the output voltage,

$$\therefore \quad V_o = V_R \tag{10}$$

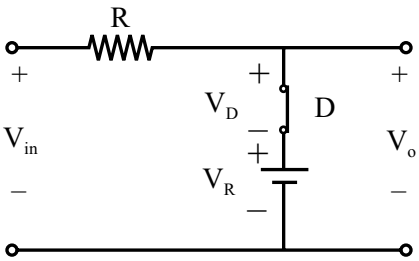


Fig.6 Equivalent circuit of positive level clipper circuit with positive reference voltage and $V_D > 0$

Waveforms:

If input signal is sinusoidal then waveform of output and input signals will be as shown in Fig.7. The sinusoidal waveform with dotted line represents the input signal and part of sinusoidal waveform with dark line represents the output signal. It can be observed from the waveform that when input signal is less the reference voltage V_R the output signal is same as input signal and when input signal becomes more than the reference voltage level the output signal is clipped at reference voltage V_R.

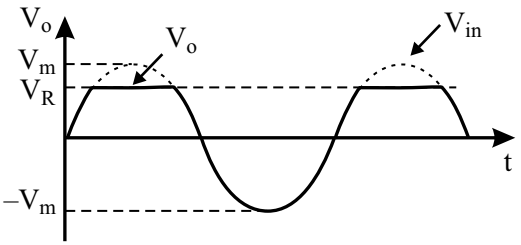


Fig.7 Waveform of input and output signals of positive level clipper circuit with positive reference voltage

Transfer characteristics:

The transfer characteristics of clipper circuit gives the variation of output voltage with respect to input voltage. It observed from the waveforms of input and output signals in Fig.7 that the input voltage varies from $-V_m$ to $+V_m$ and corresponding variation in output voltage of the circuit is from $-V_m$ to $+V_R$. Fig. 8 represents the transfer characteristics of the of a positive level clipper circuit with positive reference voltage.

When $V_{in} \leq V_R$; $\quad V_o = V_{in}$ (11)

If y-axis of transfer characteristics represents output voltage and x-axis represents input voltage then above equation represents a straight line of unit slope for the range $V_{in} \leq V_R$ as shown in Fig. 8.

When $V_{in} \geq V_R$; $\quad V_o = V_R$ (12)

So, the output voltage is V_R when the input voltage becomes more than V_R as shown in the Fig. 8.

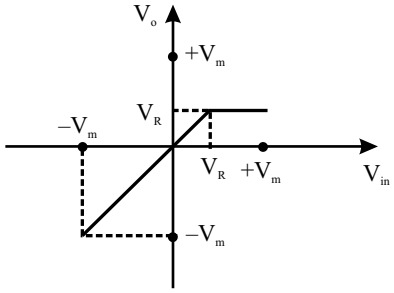


Fig.8 Transfer characteristics of positive level clipper circuit with positive reference voltage

Note : *When V_R is zero the above circuit behaves like a half wave rectifier, with only negative half cycle presents at the output.*

Circuit 2: Positive Level Clipper with Negative Reference

A positive level clipper with negative reference voltage consisting of a shunt branch with a reference voltage source in series with an ideal diode connected across the load is shown in Fig.9. The reference voltage is negative if its polarity is opposite to that of input voltage as in circuit of Fig. 9.

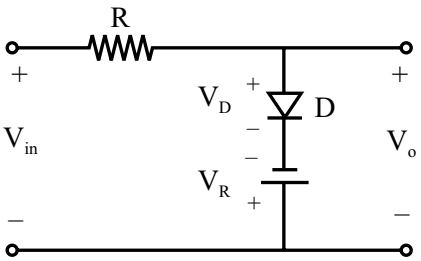


Fig.9 Shunt diode positive level clipper circuit with negative reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 10. The diode D is off when voltage across the diode negative i.e. $V_D < 0$. If a KVL is applied in input loop of the circuit as shown below with diode in open circuited condition then the voltages, V_{in}, V_D and V_R are related as under,

$$V_{in} - V_D + V_R = 0 \tag{13}$$

The voltage drop across the resistance R is not considered while applying KVL in input loop because the current in R is zero when diode is open circuited. Therefore, voltage drop across R is zero.

$$\Rightarrow \quad V_D = V_{in} + V_R \tag{14}$$

The diode D is off if, $V_D < 0$ (15)

$$\Rightarrow \quad V_{in} + V_R < 0 \tag{16}$$

$$\Rightarrow \quad V_{in} < -V_R \tag{17}$$

Under open circuited condition of the diode, the current through resistance R is zero, so voltage drop across R is zero and the output voltage becomes same as input voltage.

$$\therefore \quad V_o = V_{in} \tag{18}$$

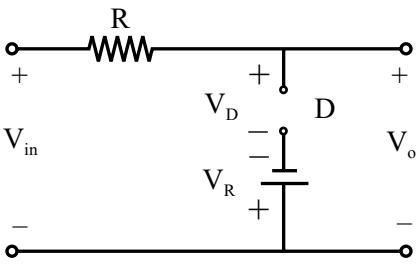


Fig.10 Equivalent circuit of positive level clipper circuit with negative reference voltage and $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig.11. When diode is in OFF condition the voltage across the diode is given by equation (14). The diode will turn ON from OFF only at the instant when V_D becomes more than zero.

The diode D turns on ON when,

$$V_D > 0 \tag{19}$$

$$\Rightarrow \quad V_{in} + V_R > 0 \tag{20}$$

$$\Rightarrow \quad V_{in} > -V_R \tag{21}$$

Under short circuited condition of the diode, the battery is directly connected across the output terminals. However, the polarity of output voltage and that of battery is opposite so the output voltage is equal to $-V_R$. Thus when the input voltage is greater than $-V_R$ the output voltage,

$$\therefore \quad V_o = -V_R \tag{22}$$

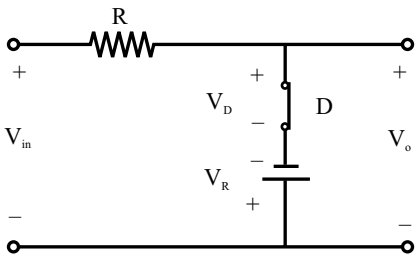


Fig.11 Equivalent circuit of positive level clipper circuit with negative reference voltage and $V_D > 0$

Waveforms:

The waveforms of output signal for a sinusoidal input signal is shown in Fig.12. The sinusoidal waveform with dotted line represents the input signal and part of sinusoidal waveform with dark line represents the output signal. It can be observed from the waveform that when input signal is less the reference voltage, $-V_R$, the output signal is same as input signal and when input signal becomes more than the reference voltage level the output signal is clipped at reference voltage $-V_R$.

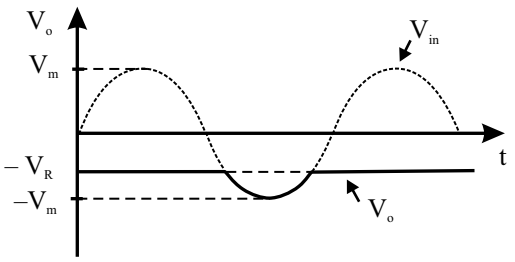


Fig.12 Waveform of input and output signals of positive level clipper with negative reference voltage

Transfer characteristics:

It observed from the waveforms of input and output signals in Fig.12 that the input voltage varies from $-V_m$ to $+V_m$ and corresponding variation in output voltage of the circuit is from $-V_m$ to $-V_R$. Fig. 13 represents the transfer characteristics of the of a positive level clipper circuit with negative reference voltage.

When $V_{in} \leq -V_R$; $V_o = V_{in}$ (23)

Above equation represents a straight ling of unit slope.

When $V_{in} \geq -V_R$; $V_o = -V_R$ (24)

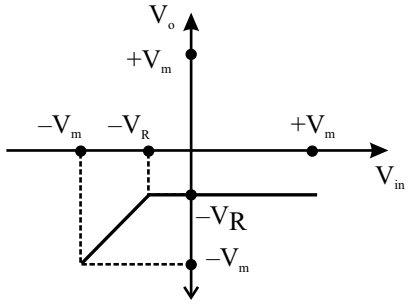


Fig.13 Transfer characteristics of positive level clipper circuit with negative reference voltage

Circuit 3: Negative Level Clipper with Positive Reference

A negative level clipper with positive reference voltage consisting of a shunt branch with a reference voltage source in series with an ideal diode connected across the load is shown in Fig.14.

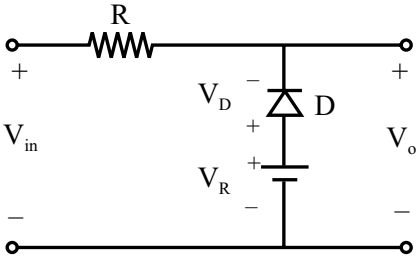


Fig.14 Shunt diode negative level clipper circuit with positive reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 15. The KVL on

input side of the circuit gives,

$$V_{in} - V_R + V_D = 0 \quad (25)$$

The voltage drop across R is zero because the diode is open.

$$\Rightarrow \quad V_D = -V_{in} + V_R \quad (26)$$

The diode D is off if, $V_D < 0$ (27)

$$\Rightarrow \quad -V_{in} + V_R < 0 \quad (28)$$

$$\Rightarrow \quad V_{in} > V_R \quad (29)$$

Under open circuited condition of the diode, the current through resistance R is zero, so voltage drop across R is zero and the output voltage becomes same as input voltage.

$$\therefore \quad V_o = V_{in} \quad (30)$$

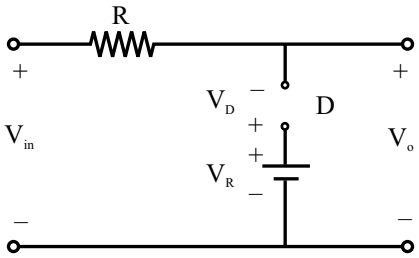


Fig.15 Equivalent circuit of negative level clipper circuit with positive reference voltage and $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig.16. When diode is in OFF condition the voltage across the diode is given by equation (26).

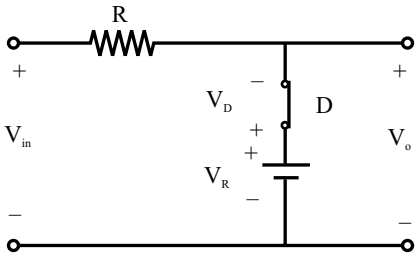


Fig.16 Equivalent circuit of negative level clipper with positive reference voltage and $V_D > 0$

The diode D turns on ON when,

$$V_D > 0 \quad (31)$$

$$\Rightarrow \quad -V_{in} + V_R > 0 \quad (32)$$

$$\Rightarrow \quad V_{in} < V_R \tag{33}$$

Under short circuited condition of the diode, the battery is directly connected across the output terminals. Then the output voltage,

$$\therefore \quad V_o = V_R \tag{34}$$

Waveforms:

The waveforms of output signal for a sinusoidal input signal is shown in Fig.17. It can be observed from the waveform that when input signal is less the reference voltage, V_R, the output signal is clipped at voltage level V_R and when input signal becomes more than the reference voltage, the output signal is same as input voltage.

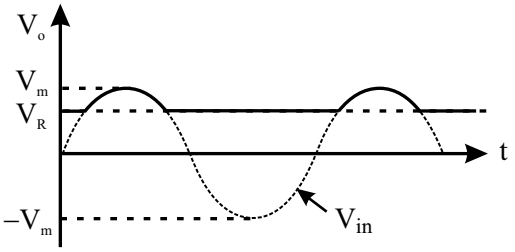


Fig.17 Waveform of input and output signals of negative level clipper with positive reference voltage

Transfer characteristics:

It is seen from above waveform that the output voltage varies from + V_R to +V_m for corresponding change of input voltage from –V_m to +V_m. Fig. 18 represents the transfer characteristics of the of a negative level clipper circuit with positive reference voltage.

When $V_{in} \leq V_R$; $\quad V_o = V_R$ (35)

When $V_{in} \geq V_R$; $\quad V_o = V_{in}$ (36)

Thus the output clipped at level V_R for $V_{in} \leq V_R$ and it is a straight line of unity slope for the range $V_{in} \geq V_R$ as shown in Fig. 18.

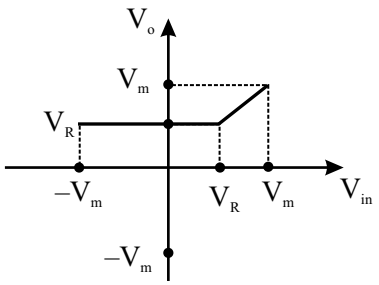


Fig.18 Transfer characteristics of negative level clipper with positive reference

Circuit 4: Negative Level Clipper with Negative Reference

A negative level clipper with negative reference voltage consisting of a shunt branch with a reference

voltage source in series with an ideal diode connected across the load is shown in Fig.19.

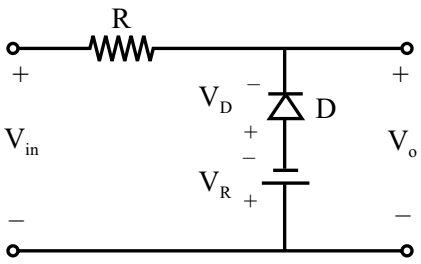


Fig.19 Shunt diode negative level clipper with negative reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 20. The KVL on input side of the circuit gives,

$$V_{in} + V_D + V_R = 0 \tag{37}$$

The voltage drop across R is zero because the diode is open.

$$\Rightarrow \quad V_D = -V_{in} - V_R \tag{38}$$

The diode D is off if, $V_D < 0$ (39)

$$\Rightarrow \quad -V_{in} - V_R < 0 \tag{40}$$

$$\Rightarrow \quad V_{in} > -V_R \tag{41}$$

Under open circuited condition of the diode, the current through resistance R is zero, so voltage drop across R is zero and the output voltage becomes same as input voltage.

$$\therefore \quad V_o = V_{in} \tag{42}$$

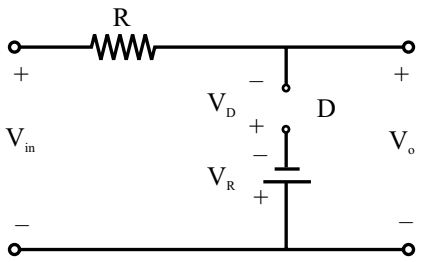


Fig.20 Equivalent circuit of negative level clipper with negative reference voltage and $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig. 21. When diode is in OFF condition the voltage across the diode is given by equation (38).

The diode D turns on ON when,

$$V_D > 0 \tag{43}$$

$$\Rightarrow \quad -V_{in} - V_R > 0 \tag{44}$$

$$\Rightarrow \quad V_{in} < -V_R \tag{45}$$

Under short circuited condition of the diode, the battery is directly connected across the output terminals. Then the output voltage,

$$\therefore \quad V_o = -V_R \tag{46}$$

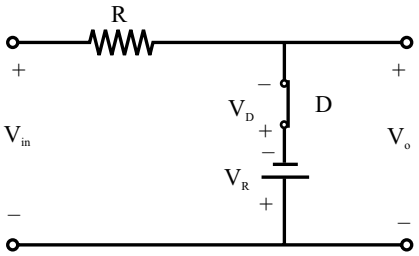


Fig.21 Equivalent circuit of negative level clipper with negative reference voltage and $V_D > 0$

Waveforms:

The waveforms of output signal for a sinusoidal input signal is shown in Fig.22. It can be observed from the waveform that when input signal is less the reference voltage, $-V_R$, the output signal is clipped at voltage level $-V_R$ and when input signal becomes more than the reference voltage, the output signal is same as input voltage.

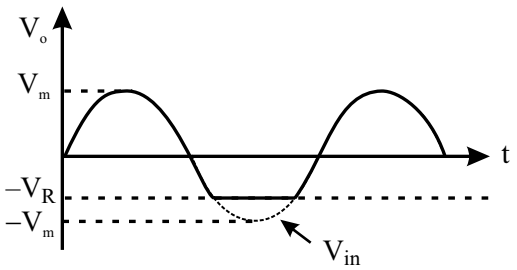


Fig.22 Waveform of input and output signals of negative level clipper with negative reference voltage

Transfer characteristics:

It is seen from above waveform that the output voltage varies from $-V_R$ to $+V_m$ for corresponding change of input voltage from $-V_m$ to $+V_m$. Fig. 23 represents the transfer characteristics of the of a negative level clipper circuit with negative reference voltage.

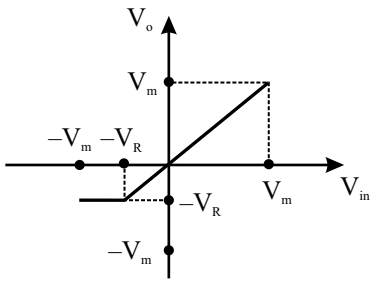


Fig.23 Transfer characteristics of negative level clipper with negative reference

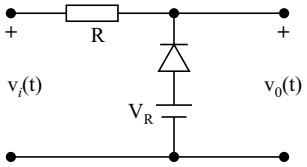
When $V_{in} \leq -V_R$; $V_o = -V_R$

When $V_{in} \geq -V_R$; $V_o = V_{in}$

Thus, the output clipped at level $-V_R$ for $V_{in} \leq -V_R$ and it is a straight line of unity slope for the range $V_{in} \geq -V_R$ as shown in Fig. 23.

Example 1

Assuming ideal diode characteristics, the input/output voltage relationship for the circuit shown in figure is



(a) $v_o(t) = v_i(t)$ for all $v_i(t)$

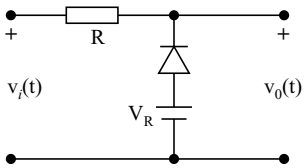
(b) $v_o(t) = v_i(t)$, for $v_i(t) > V_R$
$= V_R$, otherwise

(c) $v_o(t) = v_i(t)$, for $v_i(t) < V_R$
$= V_R$, otherwise

(d) $v_o(t) = v_i(t)$, for $v_i(t) > V_R$
$= V_R$, otherwise

GATE(IN/2004/1M)

Solution : Ans.(d)



The given circuit is clipper circuit with output given by,

Case-I : when $v_i(t) < V_R$

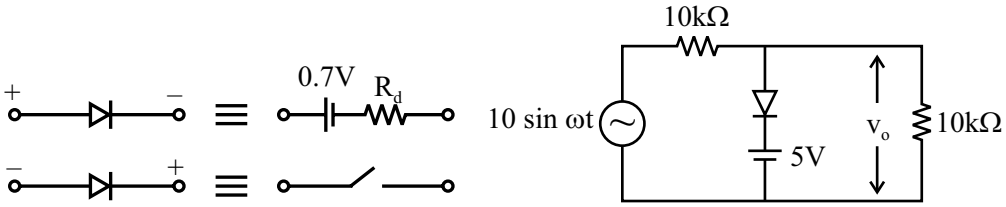
Diode is ON and $v_o(t) = V_R$

Case-II : when $v_i(t) > V_R$

Diode is OFF and $v_o(t) = v_i(t)$

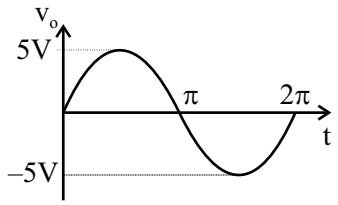
Example 2

The equivalent circuits of a diode, during forward biased and reverse biased conditions, are shown in the figure.

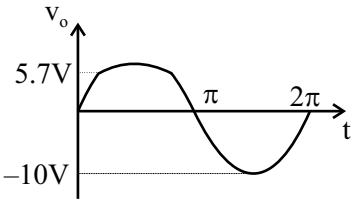


If such a diode is used in clipper circuit of figure given above, the output voltage (v_o) of the circuit will be

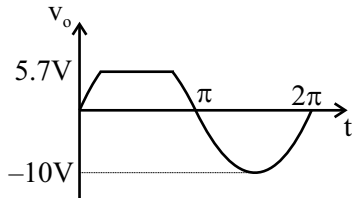
(a)



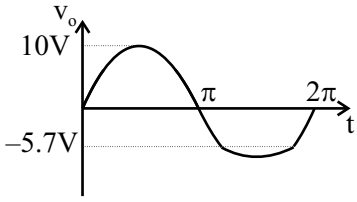
(b)



(c)

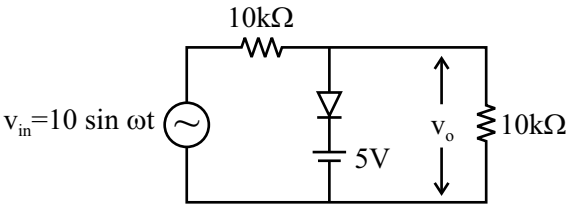


(d)



GATE(EE/2008/1 M)

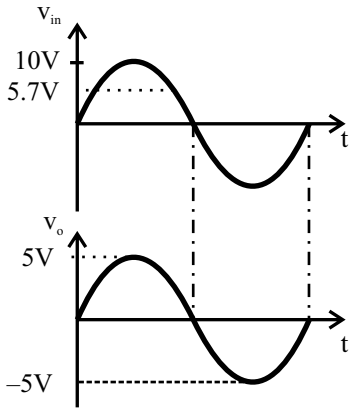
Solution : Ans.(a)



In the circuit shown above the diode will be forward biased only when $v_{in} > 5.7$ V. The maximum possible value of v_o in above circuit can reach to $v_{o\max} = \frac{10}{10\quad 10} \times 10V = 5V$. So, the diode will remain off all the times and output voltage of circuit will be,

$$v_o = \frac{10}{10+10} \times v_{in} = 5 \sin \omega t$$

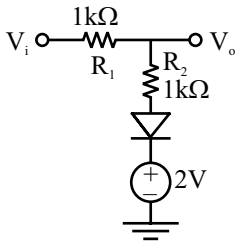
Waveforms :



Example 3

The diode in the circuit shown has V_{on} = 0.7 Volts but is ideal otherwise. If V_i = 5sin(ωt) Volts, the

minimum and maximum values of V_o (in Volts) are, respectively,



(a) – 5 and 2.7 (b) 2.7 and 5

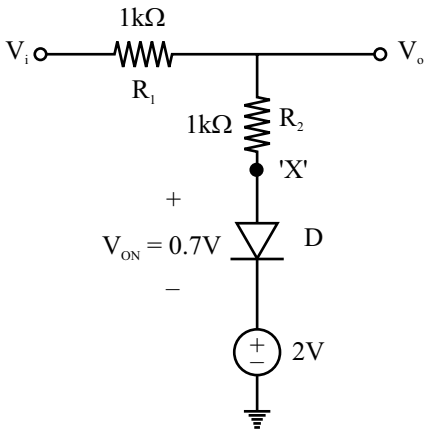
(c) – 5 and 3.85 (d) 1.3 and 5

GATE(EC-II/2014/2M)

Solution : Ans. (c)

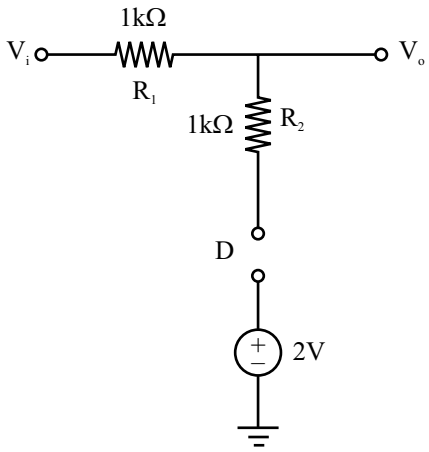
Given, $V_i = 5 \sin \omega t$

The diode will OFF when $V_x < 2.7$ V



Case-I : When $V_i < 2.7$ V

The diode D is off for $V_i < 2.7$ V. The equivalent circuit for $V_i < 2.7$ V becomes as under



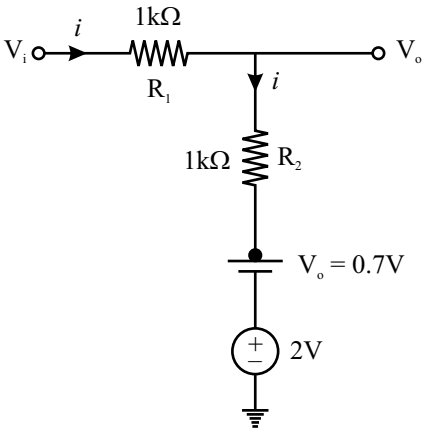
$\therefore \quad V_o = V_i = 5 \sin \omega t$

V_o is minimum when $\sin \omega t = -1$

$\therefore \quad V_{o,\,min} = -5V$

Case-II : When $V_i > 2.7$ V

The diode is turned on when input voltage $V_i \geq 2.7$ V. The equivalent voltage for $V_i \geq 2.7$ V will be as under,



Current in resistance R_2,

$$i = \frac{V_i - 2.7}{R_1 + R_2} = \frac{V_i - 2.7}{2\,k\Omega}$$

Output voltage

$\therefore \quad V_o = iR_2 + 2.7$ V

$\Rightarrow \quad V_o = \frac{V_i - 2.7}{2k} \times 1k + 2.7$

$\Rightarrow \quad V_o = \frac{5 \sin \omega t}{2} + 1.35$

$\Rightarrow \quad V_o = 2.5 \sin \omega t + 1.35V$

Output voltage V_o is maximum when $\sin \omega t = 1$

$\therefore \quad V_{o,\,max} = 2.5 + 1.35 = 3.85V$

1.2.2 One Level Clipper with Series Connected Diode

These are the circuits with a diode connected in series with load. The reference voltage source is connected in shunt with the load.

Circuit 1: Positive Level Clipper Circuits with Positive Reference

Fig. 24 shows the circuit of one level clipper with series connected diode having positive reference

voltage. Analysis of the circuit will be done by taking OFF condition of diode followed by ON condition for ease of understanding the operation of the circuit which is discussed in the following two cases.

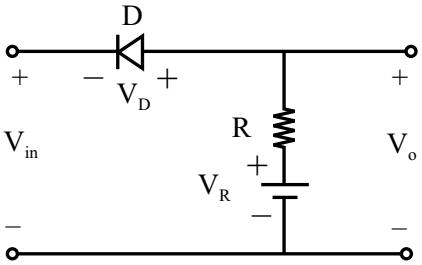


Fig.24 Series diode positive level clipper circuit with positive reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 25. The diode is assumed to be ideal and it is off when voltage across the diode negative i.e. $V_D < 0$. The KVL in input side of the circuit gives,

$$V_{in} + V_D - V_R = 0 \quad (47)$$

Voltage across R is not considered while applying KVL in input loop because the current in R is zero when diode is open.

$$\Rightarrow \quad V_D = -V_{in} + V_R \quad (48)$$

The diode D is off if, $V_D < 0$ (49)

$$\Rightarrow \quad -V_{in} + V_R < 0 \quad (50)$$

$$\Rightarrow \quad V_{in} > V_R \quad (51)$$

Under open circuited condition of the diode, the current through resistance R is zero, so voltage drop across R is zero and the output voltage becomes same as reference voltage.

$$\therefore \quad V_o = V_R \quad (52)$$

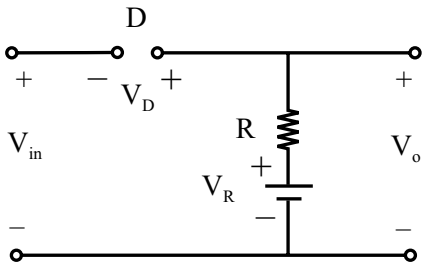


Fig.25 Equivalent circuit of series connected dide clipper with $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig. 26. The diode D turns on ON when,

$$V_D > 0 \quad (53)$$

$$\Rightarrow \quad -V_{in} + V_R > 0 \quad (54)$$

$$\Rightarrow \quad V_{in} < V_R \quad (55)$$

Under short circuited condition of the diode, the input is directly connected across the output terminals so the output voltage becomes equal to V_{in} .

$$\therefore \quad V_o = V_{in} \quad (56)$$

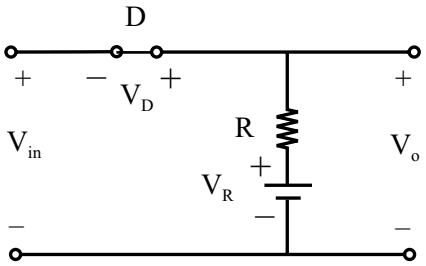


Fig.26 Equivalent circuit of positive level clipper circuit with positive reference voltage and $V_D > 0$

Waveforms:

If input signal is sinusoidal then waveform of output and input signals will be as shown in Fig.27. It can be observed from the waveform that when input signal is less the reference voltage V_R the output signal is same as input signal and when input signal becomes more than the reference voltage level the output signal is clipped at reference voltage V_R.

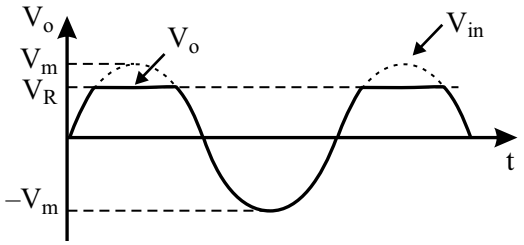


Fig.27 Waveform of input and output signals of positive level clipper circuit with positive reference voltage

Transfer characteristics:

Fig.28 represents the transfer characteristics of the of a positive level clipper circuit with positive reference voltage.

When $V_{in} \leq V_R$; $\quad V_o = V_{in} \quad (57)$

Which represents a straight line of unit slope.

When $V_{in} \geq V_R$; $\quad V_o = V_R \quad (58)$

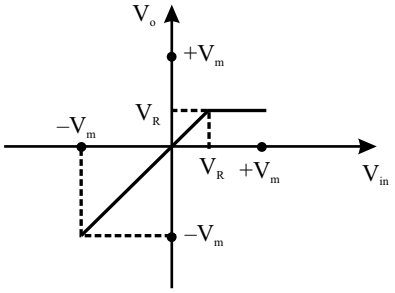


Fig.28 Transfer characteristics of positive level clipper circuit with positive reference voltage

Note : *When V_R is zero the above circuit behaves like a halfwave rectifier, with only negative half cycle presents at the output.*

Circuit 2 : Series Connected Diode Positive Level Cipper with Negative Reference

A series connected diode positive level clipper with negative reference voltage is shown in Fig.29.

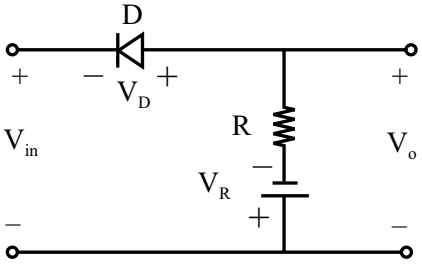


Fig.29 Series diode positive level clipper circuit with negative reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 30. The KVL in input loop of the circuit gives,

$$V_{in} + V_D + V_R = 0 \tag{59}$$

The voltage drop across R is zero when diode is open.

$$\Rightarrow \quad V_D = -V_{in} - V_R \tag{60}$$

The diode D is off if, $V_D < 0$ (61)

$$\Rightarrow \quad -V_{in} - V_R < 0 \tag{62}$$

$$\Rightarrow \quad V_{in} > -V_R \tag{63}$$

Under open circuited condition of the diode the output voltage becomes $-V_R$ because voltage drop across R is zero.

$$\therefore \quad V_o = -V_R \tag{64}$$

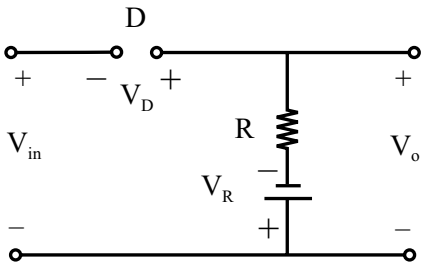


Fig.30 Equivalent circuit of positive level clipper circuit with negative reference voltage and $V_D < 0$

Case-2 : When diode D is ON

Fig. 31 shows the circuit with diode D in ON condition. The diode D turns on ON when,

$$V_D > 0 \tag{65}$$

$$\Rightarrow \quad -V_{in} - V_R > 0 \tag{66}$$

$$\Rightarrow \quad V_{in} < -V_R \tag{67}$$

Under short circuited condition of the diode, the input is directly connected across the output terminals.

$$\therefore \quad V_o = V_{in} \tag{68}$$

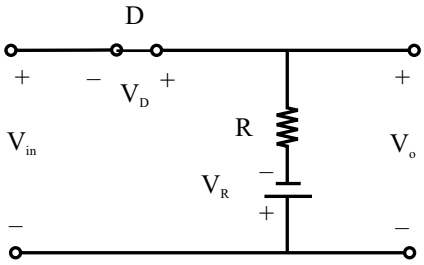


Fig.31 Equivalent circuit of positive level clipper circuit with negative reference voltage and $V_D > 0$

Waveforms:

The waveforms of output signal for a sinusoidal input signal is shown in Fig.32. It can be observed from the waveform that when input signal is less the reference voltage, $-V_R$, the output signal is same as input signal and when input signal becomes more than the reference voltage level the output signal is clipped at reference voltage $-V_R$.

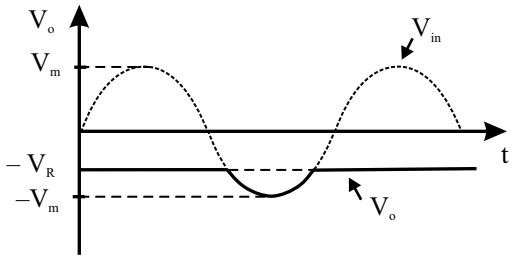


Fig.32 Iinput and output signals of positive level clipper with negative reference voltage

Transfer characteristics:

Fig. 33 represents the transfer characteristics of the of a positive level clipper circuit with negative reference voltage.

When $V_{in} \leq -V_R$; $V_o = V_{in}$ (69)

When $V_{in} \geq -V_R$; $V_o = -V_R$ (70)

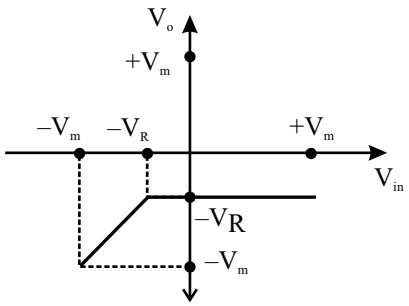


Fig.33 Transfer characteristics of positive level clipper ircuit with negative reference voltage

Circuit 3: Series Connected Diode Negative Level Clipper with Positive Reference

A negative level clipper with positive reference voltage consisting of a series connected diode is shown in Fig.34.

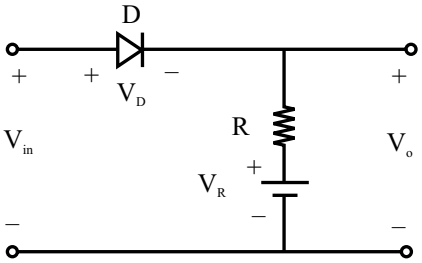


Fig.34 Series connected diode negative level clipper circuit with positive reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 35. The KVL on input side of the circuit gives,

$$V_{in} - V_D - V_R = 0 \quad (71)$$

The voltage drop across R is zero because the diode is open.

$$\Rightarrow \quad V_D = V_{in} - V_R \quad (72)$$

The diode D is off if, $V_D < 0$ (73)

$$\Rightarrow \quad V_{in} - V_R < 0 \quad (74)$$

$$\Rightarrow \quad V_{in} < V_R \quad (75)$$

Under open circuited condition of the diode, the voltage drop across R is zero and the output voltage becomes same as reference voltage.

$$\therefore \quad V_o = V_R \tag{76}$$

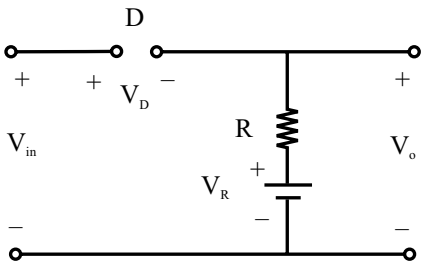


Fig.35 Equivalent circuit of negative level clipper circuit with positive reference voltage and $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig. 36. When diode is in OFF condition the voltage across the diode is given by equation (72).

The diode D turns on ON when,

$$V_D > 0 \tag{77}$$

$$\Rightarrow \quad V_{in} - V_R > 0 \tag{78}$$

$$\Rightarrow \quad V_{in} > V_R \tag{79}$$

Under short circuited condition of the diode, the output voltage is same as input voltage.

$$\therefore \quad V_o = V_{in} \tag{80}$$

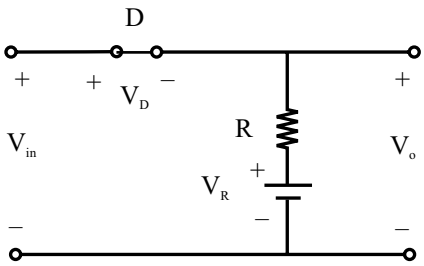


Fig.36 Equivalent circuit of negative level clipper with positive reference voltage and $V_D > 0$

Waveforms:

The waveforms of output signal for a sinusoidal input signal is shown in Fig.37. It can be observed from the waveform that when input signal is less the reference voltage, V_R, the output signal is clipped at voltage level V_R and when input signal becomes more than the reference voltage, the output signal is same as input voltage.

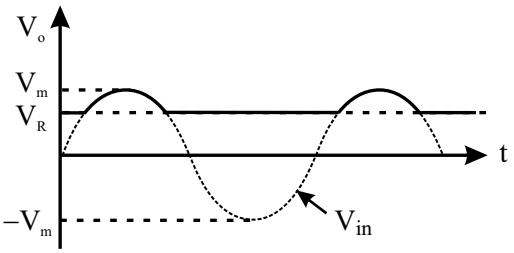


Fig.37 Waveform of input and output signals of negative level clipper with positive reference voltage

Transfer characteristics:

Fig. 38 represents the transfer characteristics of the of a negative level clipper circuit with positive reference voltage.

When $V_{in} \leq V_R$; $V_o = V_R$ (81)

When $V_{in} \geq V_R$; $V_o = V_{in}$ (82)

Thus the output clipped at level V_R for $V_{in} \leq V_R$ and it is a straight line of unity slope for the range $V_{in} \geq V_R$.

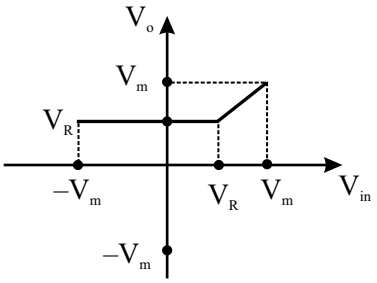


Fig.38 Transfer characteristics of negative level clipper with positive reference

Circuit 4: Series Connected Diode Negative Level Clipper with Negative Reference

A negative level clipper with negative reference voltage with series connected diode Fig.39.

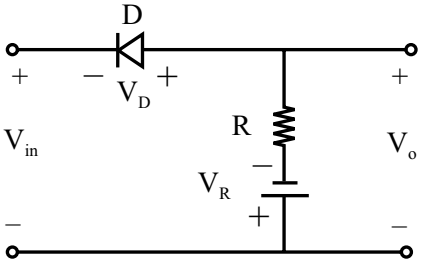


Fig.39 Series connected diode negative level clipper circuit with negative reference voltage

Case-1 : When diode D is OFF

The equivalent circuit with diode D in OFF condition becomes as shown in Fig. 40. The KVL on input side of the circuit gives,

$$V_{in} + V_D + V_R = 0 \quad (83)$$

The voltage drop across R is zero because the diode is open.

$$\Rightarrow \quad V_D = -V_{in} - V_R \quad (84)$$

The diode D is off if, $V_D < 0$ (85)

$$\Rightarrow \quad -V_{in} - V_R < 0 \quad (86)$$

$$\Rightarrow \quad V_{in} > -V_R \quad (87)$$

Under open circuited condition of the diode, the current through resistance R is zero, so voltage drop across R is zero and the output voltage becomes same as reference voltage.

$$\therefore \quad V_o = -V_R \quad (88)$$

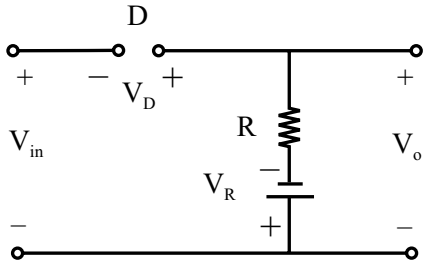


Fig.40 Equivalent circuit of negative level clipper with negative reference voltage and $V_D < 0$

Case-2 : When diode D is ON

The equivalent circuit with diode D in ON condition becomes as shown in Fig. 41. When diode is in OFF condition the voltage across the diode is given by equation (84).

The diode D turns on ON when,

$$V_D > 0 \quad (89)$$

$$\Rightarrow \quad -V_{in} - V_R > 0 \quad (90)$$

$$\Rightarrow \quad V_{in} < -V_R \quad (91)$$

Under short circuited condition of the diode, the battery is directly connected across the output terminals. Then the output voltage,

$$\therefore \quad V_o = V_{in} \quad (92)$$

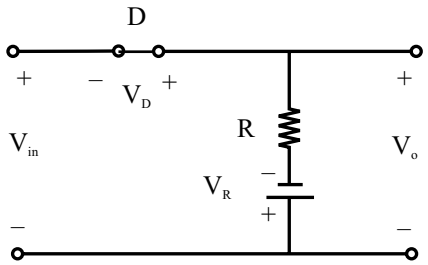


Fig.41 Equivalent circuit of negative level clipper With negative reference voltage and $V_D > 0$

Waveforms:

The waveforms of output signal for a sinusoidal input signal is shown in Fig.42. It is observed from the waveform that output voltage is clipped at level $-V_R$.

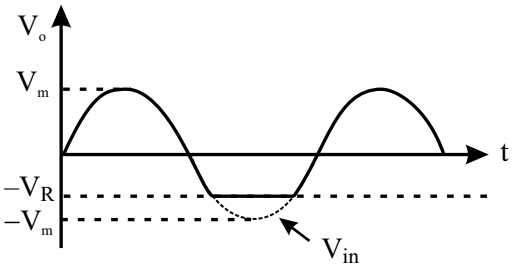


Fig.42 Waveform of input and output signals of negative level clipper with negative reference voltage

Transfer characteristics:

Fig. 43 represents the transfer characteristics of the of a negative level clipper circuit with negative reference voltage.

When $V_{in} \leq -V_R$; $V_o = -V_R$

When $V_{in} \geq -V_R$; $V_o = V_{in}$

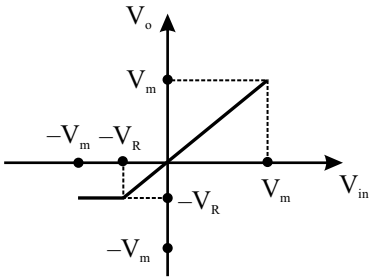


Fig.43 Transfer characteristics of negative level clipper with negative reference

Example 4

Consider the circuit shown in figure (a) If the diode used here has the V-I characteristic as in figure(b) then the output wave form v_0 is

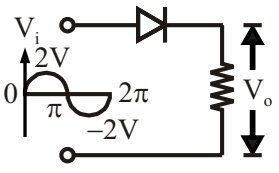


Fig. (a)

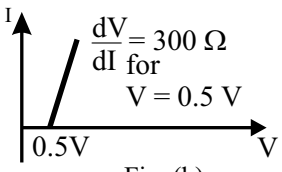
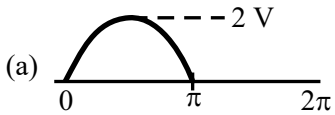
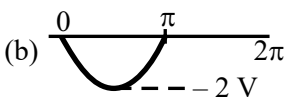
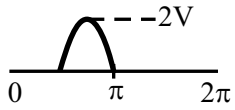
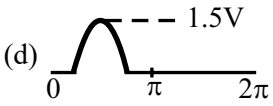


Fig. (b)



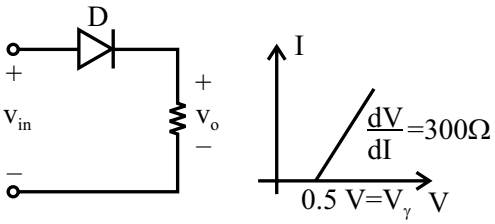


(c) 

(d) 

GATE(EC/1993/2M)

Solution : Ans.(d)



From the given circuit and characteristics of diode,

$V_{in} = 2 \sin \omega t$ and $V_\gamma = 0.5$ V

Case-I : $V_{in} < V_\gamma$; where $V_\gamma \rightarrow$ cut in voltage of diode

D $\rightarrow$ OFF

$V_o = 0$ V

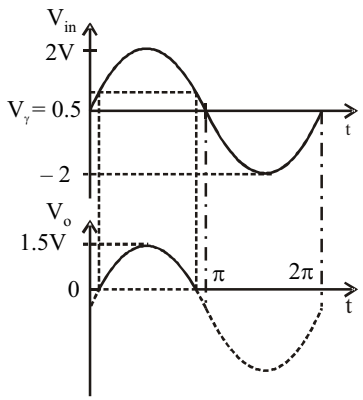
Case-II : $V_{in} > V_\gamma$

D $\rightarrow$ ON

$V_o = V_{in} - 0.5 = 2 \sin \omega t - 0.5$

Peak value of output voltage, $V_o = 2 - 0.5 = 1.5$ V

The waveforms of input and output signals can be drawn as shown below,



1.2.3 Two Level Clipper with Shunt Connected Diodes

A two level clipper consists of two diodes connected in shunt with the load as shown in Fig. 44. Two references sources are connected in series with the diodes which decide the clipping level of input voltage. The input signal is assumed to be sinusoidal. With the given connections of diodes D1 and D2 the circuit of Fig. 44 works as a clipper circuit if and only if $V_{R1} < V_{R2}$.

Circuit 1 : When both V_{R1} and V_{R2} are positive

A method of finding range of input voltage for which diode was ON or OFF was developed in single level clipper circuit. Same concept will be now used directly to explain working of two level clipper circuit.

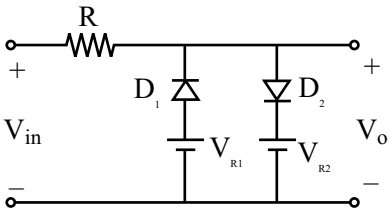


Fig.44 Two level clipper circuit with two shunt connected diodes

Case- I : When $V_{in} < V_{R1}$

Since, $V_{R1} < V_{R2}$, therefore, the input voltage is less than both V_{R1} and V_{R2}. Under this condition the Diode D_1 is forward biased and diode D_2 is reverse biased. So, the diode D_1 is ON and diode D_2 is OFF. The equivalent circuit becomes as under,

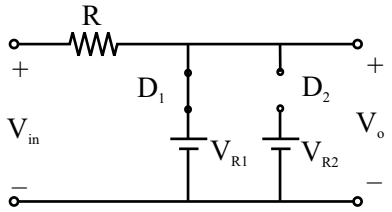


Fig.45 Equivalent circuit of two level clipper circuit when diode D_1 is ON and diode D_2 is OFF

Here the reference voltage source V_{R1} is directly connected across the output terminals so the output voltage,

$$V_o = V_{R1}$$

Case- II : $V_{R1} < V_{in} < V_{R2}$

Under this condition the both diode D_1 and diode D_2 are reverse biased. So, both diodes D_1 and diode D_2 are OFF. The equivalent circuit becomes as under,

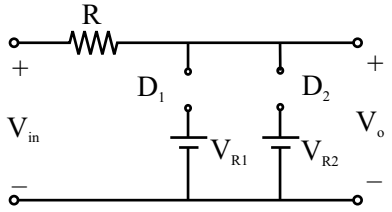


Fig.46 Equivalent circuit when diodes D_1 and D_2 are OFF

When both diodes are off the current in R is zero and hence there is no voltage drop across R and output voltage is same as input voltage.

$$V_o = V_{in}$$

Case- III : When $V_{in} > V_{R2}$

Since, $V_{R1} < V_{R2}$, therefore, the input voltage is more than both V_{R1} and V_{R2}. Under this condition

diode D_2 is forward biased and D_1 is reverse biased. So, the diode D_2 is ON and diode D_1 is OFF. The equivalent circuit becomes as under,

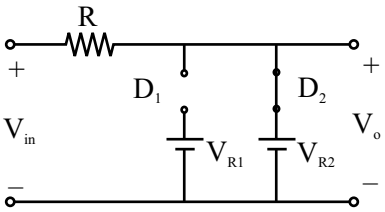


Fig.47 Equivalent circuit when diodes D_1 and D_2 are OFF

Here the reference voltage source V_{R2} is directly connected across the output terminals so the output voltage, $V_o = V_{R2}$

Waveforms :

The waveform of output and input voltages of two level clipper circuit with positive references voltages is shown in Fig. 48. It is observed from the waveform that output voltage is V_{R2} when input voltage becomes more than V_{R2} and it is V_{R1} when input voltage is less than V_{R1}. The output voltage is same as input voltage if input voltage is in the range, $V_{R1} < V_{in} < V_{R2}$.

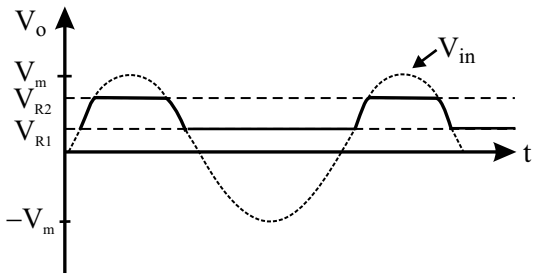


Fig.48 Waveform of two level clipper with both positive reference voltages.

Transfer characteristics :

Fig. 49 presents the transfer characteristics of a two level clipper circuit with positive reference voltages. It can be seen form the characteristics that output voltage a straight line at V_{R1} when input voltage is less than V_{R1} and output voltage is straight line at V_{R2} when input voltage is more than V_{R2}. The output voltage is $V_o = V_{in}$ for input voltage in the range $V_{R1} < V_{in} < V_{R2}$ which represents a straight line of unity slope between V_{R1} and V_{R2}.

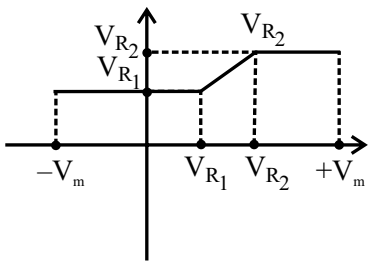


Fig.49 Transfer characteristics of two level clipper with both positive reference voltages.

Circuit 2 : When both V_{R1} is negative and V_{R2} are positive

Fig. 50 shows a two level clipper circuit with one positive and another negative reference voltage. It is assumed for proper operation of the circuit that $-V_{R1} < V_{R2}$.

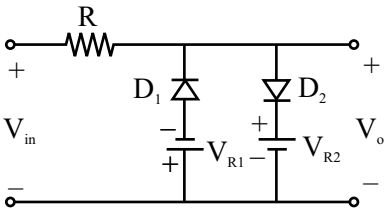


Fig.50 Two level clipper circuit with two shunt connected diodes

Case- I : When $V_{in} < -V_{R1}$

Since, $-V_{R1} < V_{R2}$, therefore, the input voltage is less than both $-V_{R1}$ and V_{R2}. Therefore, the diode D_1 is ON and diode D_2 is OFF. The equivalent circuit becomes as under,

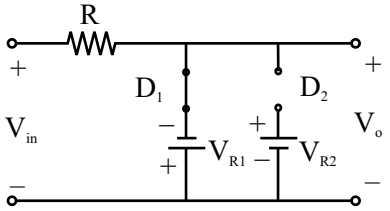


Fig.51 Equivalent circuit of two level clipper circuit when diode D_1 is ON and diode D_2 is OFF

Here the reference voltage source $-V_{R1}$ is directly connected across the output terminals so the output voltage,

$$V_o = -V_{R1}$$

Case- II : $-V_{R1} < V_{in} < V_{R2}$

Under this condition both diodes D_1 and diode D_2 are OFF. The equivalent circuit becomes as under,

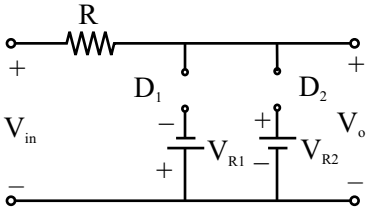


Fig.52 Equivalent circuit when diodes D_1 and D_2 are OFF

The output voltage is same as input voltage when both diodes are OFF,

$$V_o = V_{in}$$

Case- III : When $V_{in} > V_{R2}$

Since, $-V_{R1} < V_{R2}$, therefore, the input voltage is more than both $-V_{R1}$ and V_{R2}. Under this condition diode D_2 is ON and diode D_1 is OFF. The equivalent circuit becomes as under,

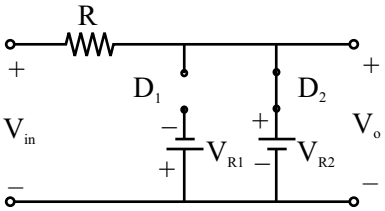


Fig.53 Equivalent circuit when diodes D_1 and D_2 are OFF

Here the reference voltage source V_{R2} is directly connected across the output terminals so the output voltage, $V_o = V_{R2}$

Waveforms :

The waveform of output and input voltages of two level clipper circuit with positive references voltages is shown in Fig. 54.

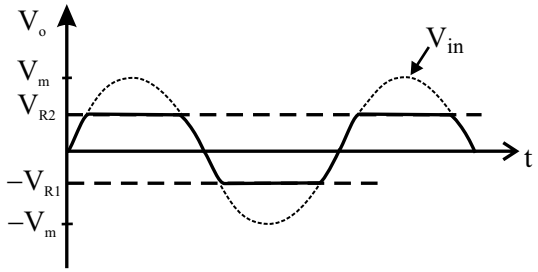


Fig.54 Waveform of two level clipper with positive and negative reference voltages.

Transfer characteristics :

Fig. 55 represents the transfer characteristics of a two level clipper circuit with positive reference voltage V_{R2} and negative reference $-V_{R1}$.

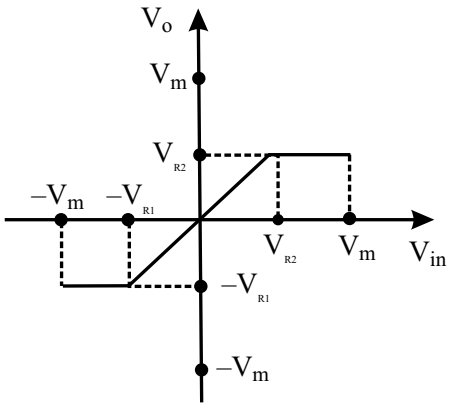


Fig.55 Transfer characteristics of two level clipper with both positive reference voltages.

Circuit 3 : When both V_{R1} and V_{R2} are negative

Fig. 56 shows a two level clipper circuit with both negative reference voltages. It is assumed for proper operation of the circuit that $-V_{R1} < -V_{R2}$.

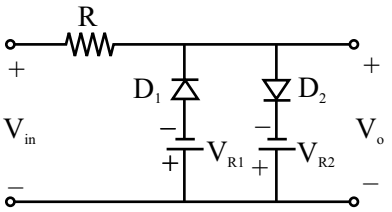


Fig.56 Two level clipper circuit with two shunt connected diodes

Case- I : When $V_{in} < -V_{R1}$

Since, $-V_{R1} < -V_{R2}$, therefore, the input voltage is less than both $-V_{R1}$ and $-V_{R2}$. Therefore, the diode D_1 is ON and diode D_2 is OFF. The equivalent circuit becomes as under,

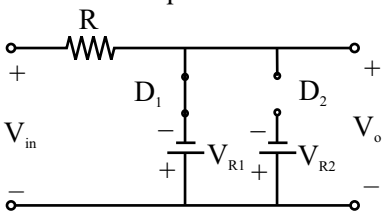


Fig.57 Equivalent circuit of two level clipper circuit when diode D_1 is ON and diode D_2 is OFF

The voltage source $-V_{R1}$ is directly connected across the output terminals so the output voltage,

$$V_o = -V_{R1}$$

Case- II : $-V_{R1} < V_{in} < -V_{R2}$

Under this condition both diodes D_1 and diode D_2 are OFF. The equivalent circuit becomes as shown under,

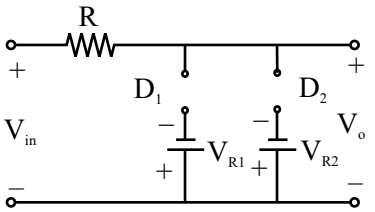


Fig.58 Equivalent circuit when diodes D_1 and D_2 are OFF

The output voltage is same as input voltage when both diodes are OFF,

$$V_o = V_{in}$$

Case- III : When $V_{in} > -V_{R2}$

Under this condition diode D_2 is ON and diode D_1 is OFF. The equivalent circuit becomes as shown under,

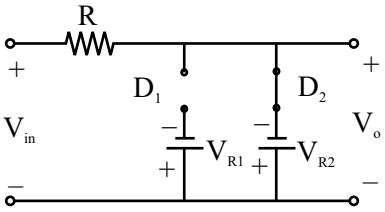


Fig.59 Equivalent circuit when diodes D_1 and D_2 are OFF

The reference voltage source $-V_{R2}$ is directly connected across the output terminals so the output voltage,

$$V_o = -V_{R2}$$

Waveforms :

The waveform of output and input voltages of two level clipper circuit with negative references voltages is shown in Fig. 60.

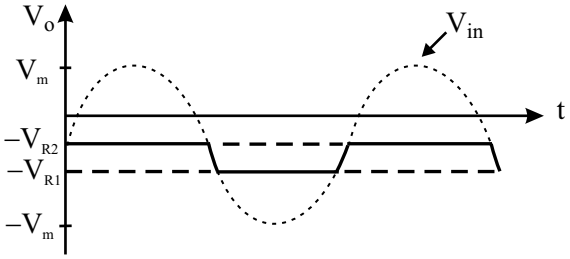


Fig.60 Waveform of two level clipper with positive and negative reference voltages.

Transfer characteristics :

Fig. 61 represents the transfer characteristics of a two level clipper circuit with negative references voltages.

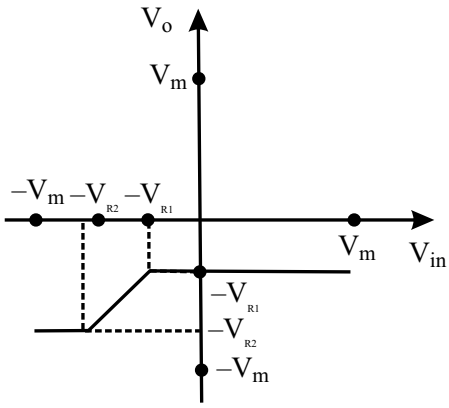
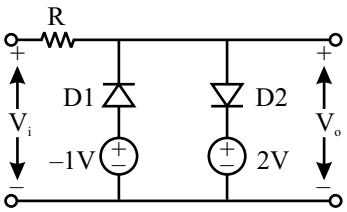


Fig.61 Transfer characteristics of two level clipper with both positive reference voltages.

Example 5

Two silicon diodes, with a forward voltage drop of 0.7 V, are used in the circuit shown in the figure. The range of input voltage V_i for which the voltage $V_o = V_i$, is



(a) $-0.3\ V < V_i < 1.3\ V$

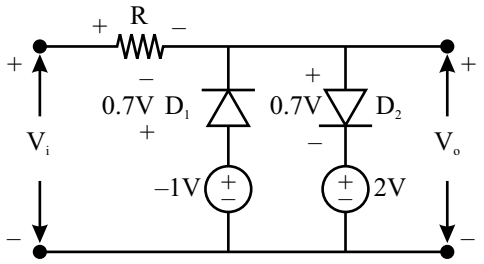
(b) $-0.3\ V < V_i < 2V$

(c) $-1.0\ V < V_i < 2.0\ V$

(d) $-1.7\ V < V_i < 2.7\ V$

GATE(EC-IV/2014/1M)

Solution : Ans. (d)



The output voltage of the given circuit will be same as input voltage when both diodes are OFF.

Case - I : Here diode D_2 is off when

$$V_{D2} < 0.7V \qquad .....(i)$$

KVL in loop containing D_2,

$$V_i - V_R - V_{D2} - 2 = 0$$

When both diodes are off current in R is zero, so $V_R = 0$.

$$\therefore \quad V_i = V_{D2} + 2$$

$$V_{D2} = V_i - 2$$

Putting above relation in equation (i), we have

$$V_i - 2 < 0.7V$$

$$V_i < 2.7V$$

So D_2 is off when $V_i < 2.7$ V

Case - II :Diode D_1 is off when

$$V_{D1} < 0.7V \qquad .....(ii)$$

KVL is loop contain V_i and D_1

$$V_i + V_{D1} - (-1V) = 0$$

$$V_{D1} = -V_i - 1$$

Surfing above relation in equation (ii), we have,

$$-V_i - 1 < 0.7V$$

$$\Rightarrow \quad -V_i < 1.7V$$

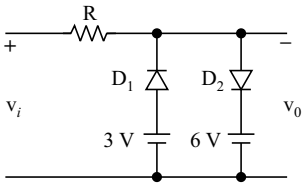
$\Rightarrow$ $V_i > -1.7V$

The diode D_2 is OFF when input voltage $V_i < (2 + 0.7)$ V and diode D_1 is OFF when input voltage $V_i > -1.7V$

$\therefore$ Range of input voltage for which $V_o = V_i$ is $-1.7V < V_i < 2.7$ V

Example 6

In the circuit shown in figure v_i is 4 V. Assuming the diodes to be ideal, v_0 is

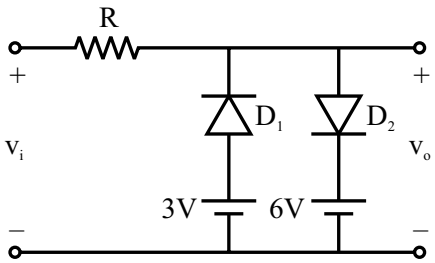


(a) 3V (b) 4V

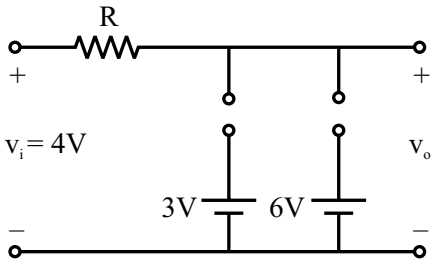
(c) 4.5 V (d) 6 V

GATE(IN/1999/2M)

Solution : Ans.(b)



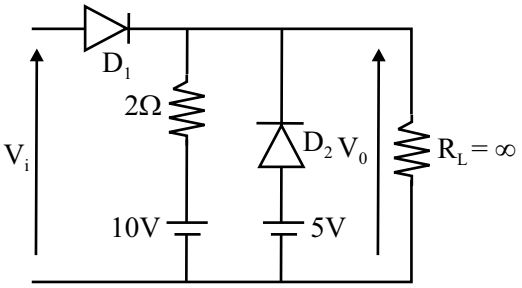
In above circuit diode D_1 is OFF when $v_i = 3V$ and diode D_2 OFF when $v_i < 6V$. Here $v_i = 4V$ so both D_1 and D_2 are OFF. Then equivalent circuit becomes as under,



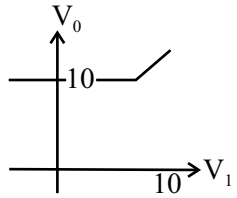
Output voltage of above circuit, $v_o = v_i = 4V$

Example 7

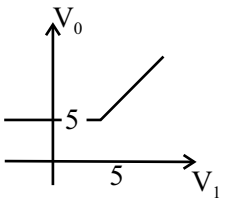
Assuming the diodes D_1 and D_2 of the circuit shown in figure to be ideal ones, the transfer characteristics of the circuit will be



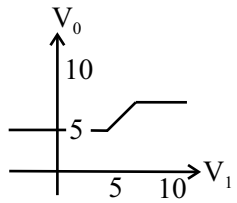
(a)



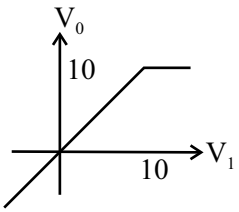
(b)



(c)

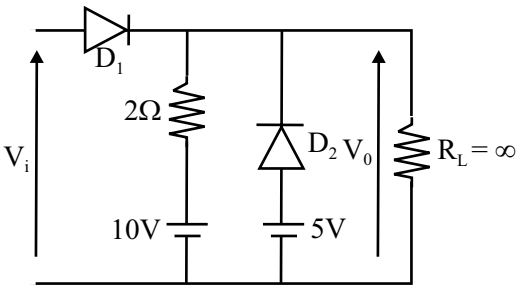


(d)



GATE(EE/2006/2 M)

Solution : Ans.(a)



Case-I $v_{in} < 10V$

$D_1 \rightarrow$ OFF, $D_2 \rightarrow$ OFF

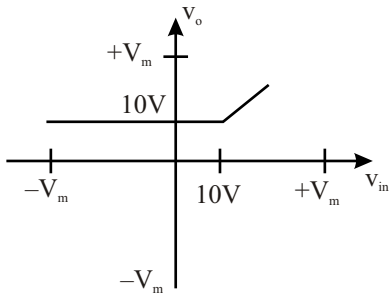
$v_o = 10V$

Case-II $v_{in} > 10V$

$D_1 \rightarrow$ ON, $D_2 \rightarrow$ OFF

$v_o = v_{in}$

Transfer characteristics,



1.2.4 Clipping Circuits Using Zener Diodes

A two level clipper circuit can also be implemented using two Zener diodes connected back to back in shunt with the load as shown in Fig. 62. Let V_{D1} and V_{D2} are forward biased voltage drops and V_{Z1} and V_{Z2} are breakdown voltages of diodes Z_1 and Z_2, respectively.

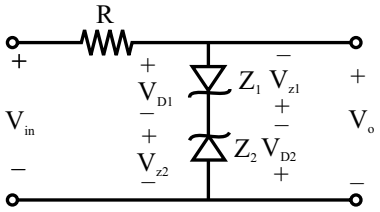


Fig.62 Two level clipper using two diodes connected back to back in parallel with load.

Case- I : When $V_{in} > (V_{D1} + V_{Z2})$

When input voltage is greater than $(V_{D1} + V_{Z2})$, the diode Z_1 is forward biased and diode Z_2 is reverse biased and works in breakdown. Therefore, both diodes Z_1& Z_2 are ON with Z_1 in forward biased mode and Z_2 in reverse breakdown mode. Under this biasing condition the voltage across diode Z_1 is V_{D1} and voltage across diode Z_2 is V_{Z2}. The equivalent circuit becomes as under,

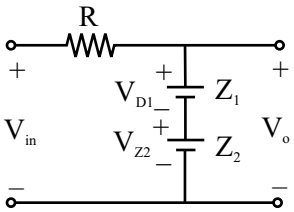


Fig.63 Equivalent circuit when input voltage $V_{in} > (V_{D1} + V_{Z2})$

The output voltage of circuit under such biasing can be given as under,

$$V_o = V_{D1} + V_{Z2} \tag{93}$$

Case- II : when $-(V_{D2} + V_{Z1}) < V_{in} < (V_{D1} + V_{Z2})$

For $0 < V_{in} < (V_{D1} + V_{Z2})$ the diode Z_1 is forward biased and diode Z_2 is reverse biased but not in breakdown region so, the diode Z_2 is OFF. For $-(V_{D2} + V_{Z1}) < V_{in} < 0$ the diode Z_2 is forward biased and diode Z_1 is reverse biased but not in breakdown region so, the diode Z_1 is OFF. Therefore, the

shunt branch consisting of Zener diodes is open circuited when $-(V_{D2} + V_{Z1}) < V_{in} < (V_{D1} + V_{Z2})$. The voltage is same as input voltage when either of the diodes is OFF.

$$\therefore \quad V_o = V_{in} \tag{94}$$

Case- III : When $V_{in} < -(V_{D2} + V_{Z1})$

When input voltage is less than $-(V_{D2} + V_{Z1})$, the diode Z_2 is forward biased and diode Z_1 is reverse biased and works in breakdown. Therefore, both diodes Z_1& Z_2 are ON, with Z_2 in forward biased mode and Z_1 in reverse breakdown mode. Under this biasing condition, the voltage across diode Z_1 is V_{Z1} and voltage across diode Z_2 is V_{D2}. The equivalent circuit becomes as under,

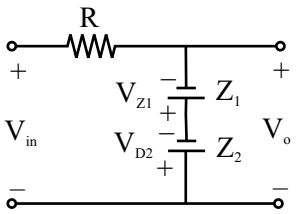


Fig.64 Equivalent circuit when input voltage $V_{in} < -(V_{D2} + V_{Z1})$

The output voltage of circuit under such biasing can be given as under,

$$V_o = -(V_{D2} + V_{Z1}) \tag{95}$$

Waveforms :

The waveform of output and input voltages of two level clipper circuit using Zener diodes is shown in Fig. 65.

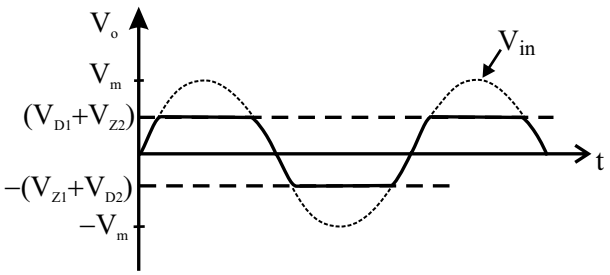


Fig.65 Waveform of two level clipper using shunt connected Zener diodes.

Transfer characteristics :

Fig. 66 represents the transfer characteristics of a two level clipper using two diodes connected back to back in parallel with load.

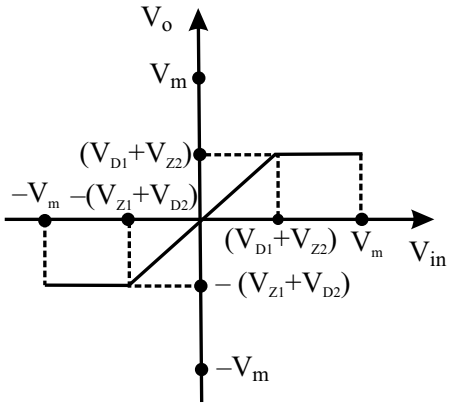
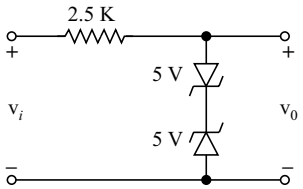


Fig.66 Transfer characteristics of two level clipper using shunt connected Zener diodes.

Example 8

For a sinusoidal input of 50 V amplitude, the circuit shown in Figure can be used as

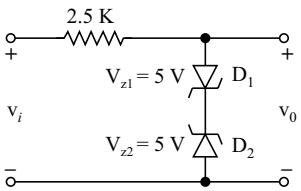


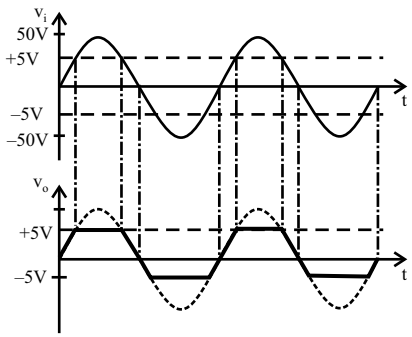
(a) Regulated dc power supply (b) Square wave generator

(c) Half wave rectifier (d) Full wave rectifier

GATE(IN/2000/2M)

Solution : Ans.(b)





Case-I : when $v_i > 5V$

$D_1 \rightarrow$ forward biased

$D_2 \rightarrow$ reverse biased (breakdown)

$\therefore \quad v_o = V_{z2} = 5V$

Case-II : When $v_i < -5V$

$D_1 \rightarrow$ Reverse breakdown

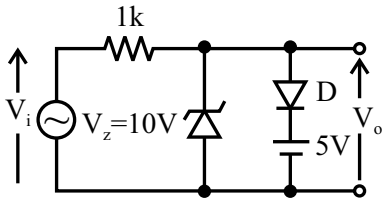
$D_2 \rightarrow$ Forward biased

$\therefore \quad v_o = V_{z1} = -5V$

So output signal is a square wave.

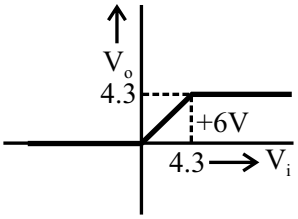
Example 9

A clipper circuit is shown below.

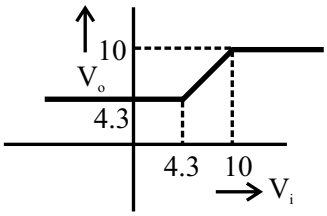


Assuming forward bias voltage drops of the diodes to be 0.7 V, the input-output transfer characteristics of the circuit is

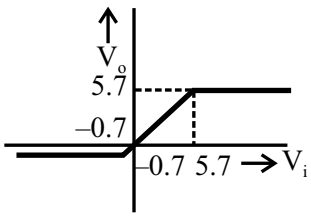
(a)



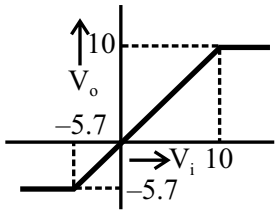
(b)



(c)

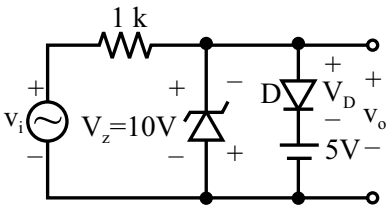


(d)



GATE(EE/2011|2 M)

Solution : Ans.(c)



Given, $V_D = 0.7$ V

Let, $v_i = V_m \sin \omega t$

& $5.7 \text{ V} < V_m < 10 \text{ V}$

Case-I : *Positive half cycle*

when $v_i > 5.7$, D is ON

and $v_o = 5.7$ V

when $v_i < 5.7$, D is OFF

and $v_o = v_i$

Case-II : *Negative half cycle*

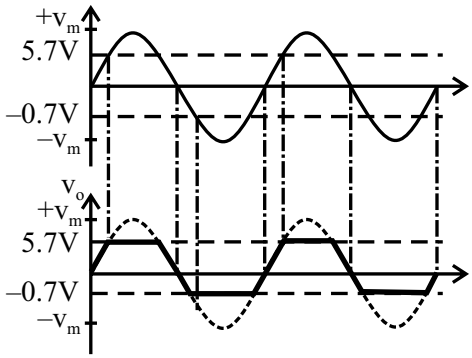
when, $v_i > -0.7$ V ; Zener diode is off

$\therefore$ $v_o = v_i$

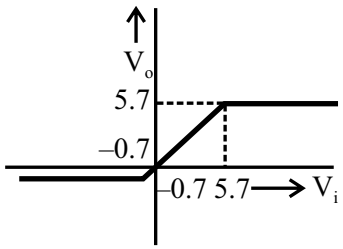
when $v_i < -0.7$ V ; Zener diode is forward biased and it is on with 0.7 V drop across diode.

$\therefore$ $v_o = -0.7$ V

Waveforms :

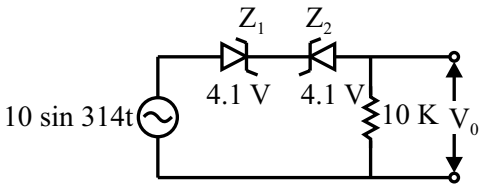


Transfer characteristics:

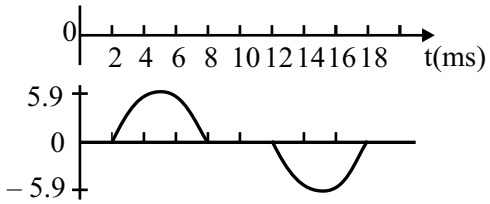


Example 10

The wave shape of V_0 in Figure will be

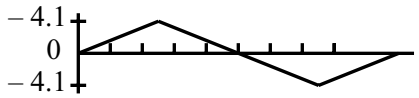


(a)

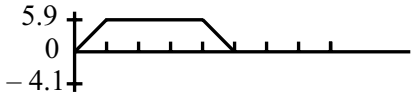


(b)

(c)

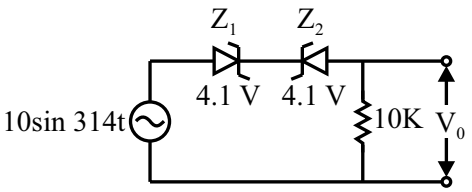


(d)



GATE(EC/1993/1M)

Solution : Ans.(a)



Let diodes are ideal with zero forward voltage drop,

$$V_{D1} = V_{D2} = 0$$

Case-I : Positive half cycle

when, $V_{in} > (V_{Z2} + V_{D1})$ or $v_{in} > 4.1$ V

$Z_1 \rightarrow$ ON (forward biased)

$Z_2 \rightarrow$ ON (zener break down)

So, $v_o = 10 \sin 314t - V_{Z2}$; $0 < t < T/2$

$v_o = v_{in} - 4.1 = 10 \sin 314t - 4.1$

Peak output voltage during positive half cycle

$$v_{o,peak} = 10 - 4.1 = 5.9 \text{ V}$$

when, $v_{in} < (V_Z + V_D)$, $v_{in} < 4.1$ V

$Z_2 \rightarrow$ OFF(reverse biased)

$Z_1 \rightarrow$ OFF (Because series connected diode Z_2 is OFF)

So, $V_o = 0$ V

Case II : During negative half cycle

when, $v_{in} < -(V_{Z2} + V_{D1})$ or $v_{in} < -4.1$ V

$Z_1 \rightarrow$ ON (zener break down)

$Z_2 \rightarrow$ ON (forward biased)

So, $v_o = v_{in} - 4.1 = -10 \sin 314t + V_{Z1}$; $T/2 < t < T$

$v_o = 10 \sin 314t + 4.1$

Peak output voltage during negative half cycle

$$v_{o,peak} = -10 + 4.1 = -5.9 \text{ V}$$

when, $v_{in} > -(V_{Z2} + V_D)$, $v_{in} > -4.1$ V

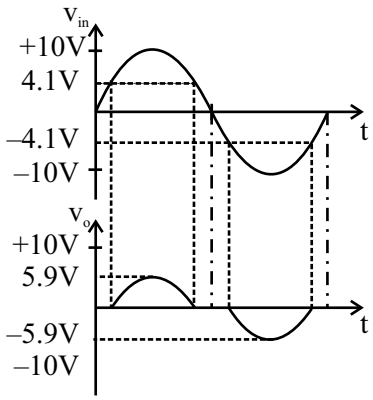
$Z_1 \rightarrow$ OFF(reverse biased)

$Z_2 \rightarrow$ OFF (Because series connected diode Z_1 is OFF)

So, $V_o = 0$ V

During positive half of input voltage the diode Z_1 is forward biased and Z_2 is reverse biased.

Waveforms of input and output signals is as shown below,



1.3 Clamper Circuits

The clamper circuits are used to shift the level of the signals vertically. There are two types of clamper circuits called negative and positive level clamper. The clamper circuits consists of series capacitor and a shunt connected diode. The time constant of circuit is kept very large as compared to time period of the signal. The clamper circuits can be with or without biasing voltage to have variable level of clamping of the signals. The negative and positive level clamper circuits are discussed in the following sections.

1.3.1 Negative Level Clamper Circuits

Circuit 1 : Negative Level Clamper Without Biasing Voltage

Fig. 67 shows the negative level clamper circuit without any biasing voltage. The input signal is a sinusoidal voltage. For better under standing of the operation of the circuit is analyzed by considering very first positive half cycle of the input waveform during which the diode D is forward biased. When diode D is forward biased the capacitor C is charged to peak (V_m) of input voltage with polarities as shown in the Fig 67. Once capacitor is charged to peak value of input voltage in first positive half cycle of the input voltage then the diode is reverse biased in negative half cycles and all the positive half cycles after first positive half cycle. The value of R is selected such that time constant RC is very large as compared to time period of the input signal. Therefore, capacitor does not discharge once it is charged.

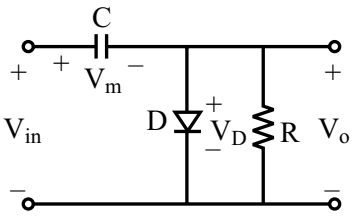


Fig.67 Negative level clamper circuit without biasing voltage

The output voltage can be written by applying KVL in outer loop of the circuit as under,

$$V_{in} - V_m - V_o = 0 \quad (96)$$

$$\Rightarrow \quad V_o = V_{in} - V_m \quad (97)$$

For sinusoidal input, $V_{in} = V_m \sin \omega t$ (98)

$$\Rightarrow \quad V_o = V_m \sin \omega t - V_m \quad (99)$$

It is seen from above equation that output voltage is shifted by $-V_m$ as compared to the input voltage of the circuit.

The waveforms of input and output signals of negative level clamper without biasing voltage is shown in Fig. 68. It is seen from waveform of output signal that the output signal is shifted vertically by $-V_m$ as compared to the input signal.

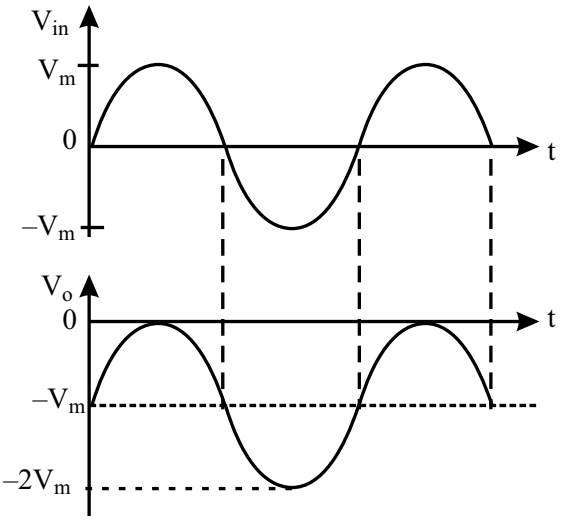


Fig.68 The waveforms of input and output signals of negative level clamper circuit without biasing voltage

Circuit 2 : Negative Level Clamper With Positive Biasing Voltage

Fig. 69 shows the negative level clamper circuit with positive biasing voltage. The operation of the circuit is similar to negative level clamper without biasing voltage. The diode D is forward biased

during first positive half cycle and the capacitor C is charged to voltage, $(V_m - V_R)$ with the polarities as shown in the Fig 69. Once capacitor is charged in first positive half cycle of the input voltage then the diode is reverse biased in negative half cycles and all the positive half cycles after first positive half cycle. The capacitor does not discharge once it is charged.

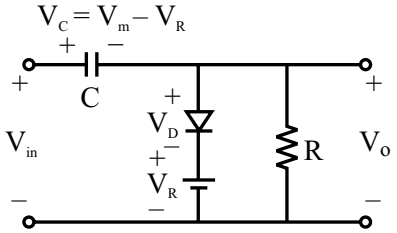


Fig.69 Negative level clamper circuit with positive biasing voltage

The output voltage can be written by applying KVL in outer loop of the circuit as under,

$$V_{in} - V_C - V_o = 0 \quad (100)$$

$$\Rightarrow \quad V_o = V_{in} - V_C \quad (101)$$

The voltage across charged capacitor ,

$$V_C = V_m - V_R \quad (102)$$

$$\Rightarrow \quad V_o = V_{in} - (V_m - V_R) \quad (103)$$

For sinusoidal input, $V_{in} = V_m \sin \omega t \quad (104)$

$$\Rightarrow \quad V_o = V_m \sin \omega t - (V_m - V_R) \quad (105)$$

It is seen from above equation that output voltage is shifted by $-(V_m - V_R)$ as compared to the input voltage of the circuit.

The waveforms of input and output signals of negative level clamper with positive biasing voltage is shown in Fig. 70. It is seen from waveform of output signal that the output signal is shifted vertically by $-(V_m - V_R)$ as compared to the input signal.

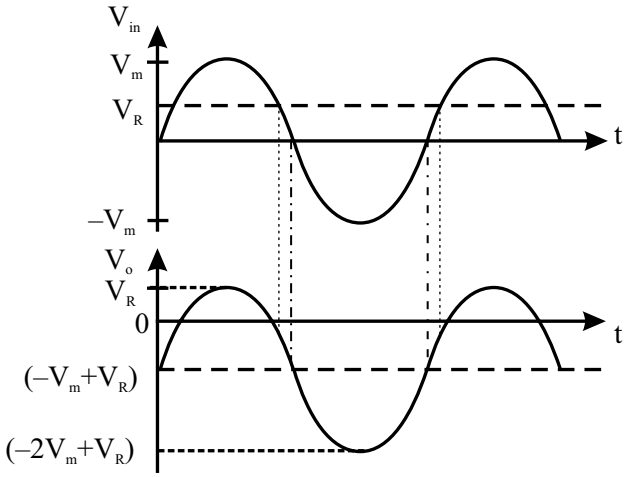


Fig.70 The waveforms of input and output signals of negative

level clamper circuit with positive biasing voltage

Circuit 3 : Negative Level Clamper With Negative Biasing Voltage

Fig. 71 shows the negative level clamper circuit with negative biasing voltage. The operation of the circuit is similar to negative level clamper with positive biasing voltage. The capacitor C is charged to voltage, $(V_m + V_R)$ during first positive half cycle with the polarities as shown in the Fig 71. Once capacitor is charged in first positive half cycle of the input voltage then the diode is reverse biased in negative half cycles and all the positive half cycles after first positive half cycle. The capacitor does not discharge once it is charged.

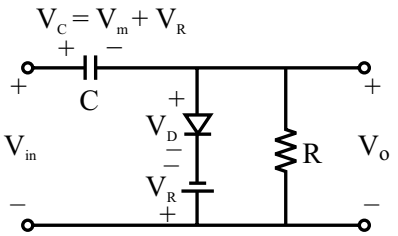


Fig.71 Negative level clamper circuit with negative biasing voltage

The output voltage can be written by applying KVL in outer loop of the circuit as under,

$$V_{in} - V_C - V_o = 0 \quad (106)$$

$$\Rightarrow \quad V_o = V_{in} - V_C \quad (107)$$

The voltage across charged capacitor ,

$$V_C = V_m + V_R \quad (108)$$

$$\Rightarrow \quad V_o = V_{in} - (V_m + V_R) \quad (109)$$

For sinusoidal input, $V_{in} = V_m \sin \omega t \quad (110)$

$$\Rightarrow \quad V_o = V_m \sin \omega t - (V_m + V_R) \quad (111)$$

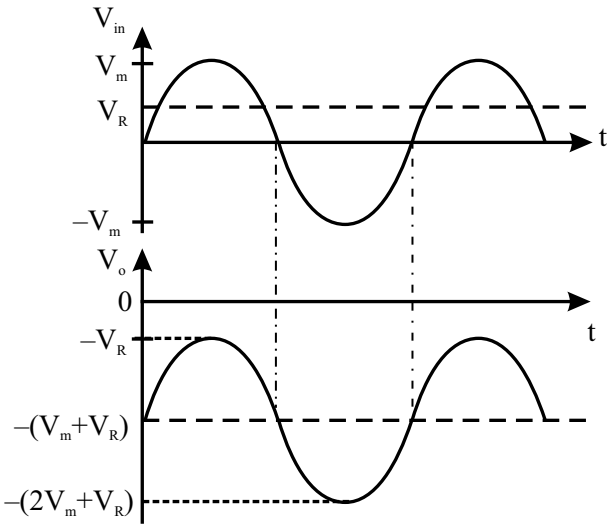


Fig.72 The waveforms of input and output signals of negative

level clamper circuit with negative biasing voltage

It is seen from above equation that output voltage is shifted by $-(V_m + V_R)$ as compared to the input voltage of the circuit. The waveforms of input and output signals of negative level clamper with negative biasing voltage is shown in Fig. 72. It is seen from waveform of output signal that the output signal is shifted vertically by $-(V_m + V_R)$ as compared to the input signal.

1.3.2 Positive Level Clamper Circuits

Circuit 1 : Positive Level Clamper Without Biasing Voltage

Fig. 73 shows the positive level clamper circuit without any biasing voltage. The circuit is analyzed by considering very first negative half cycle of the input waveform during which the diode D is forward biased. When diode D is forward biased the capacitor C is charged to peak (V_m) of input voltage with polarities as shown in the figure. Once capacitor is charged to peak value of input voltage in first negative half cycle then the diode is reverse biased in remaining positive half cycles and negative half cycles. The time constant RC is kept very large as compared to time period of the input signal. Therefore, capacitor does not discharge once it is charged.

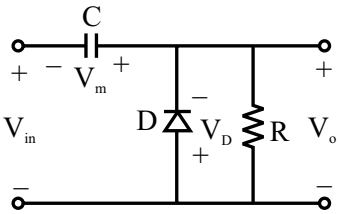


Fig.73 Positive level clamper circuit without biasing voltage

The output voltage can be written by applying KVL in outer loop of the circuit as under,

$$V_{in} + V_m - V_o = 0 \quad (112)$$

$$\Rightarrow \quad V_o = V_{in} + V_m \quad (113)$$

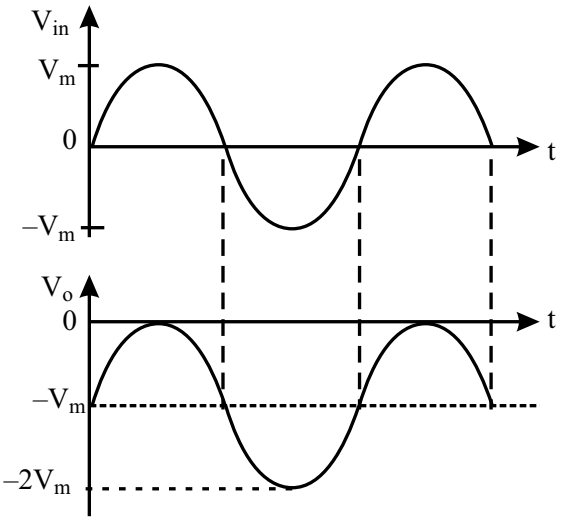


Fig.74 The waveforms of input and output signals of positive level clamper circuit without biasing voltage

For sinusoidal input, $V_{in} = V_m \sin \omega t$ (114)

$\Rightarrow$ $V_o = V_m \sin \omega t + V_m$ (115)

It is seen from above equation that output voltage is shifted by $+ V_m$ as compared to the input voltage of the circuit.

The waveforms of input and output signals of positive level clamper without biasing voltage is shown in Fig. 74.

It is seen from waveform of output signal that the output signal is shifted vertically by $+ V_m$ as compared to the input signal.

Circuit 2 : Positive Level Clamper With Positive Biasing Voltage

Fig. 75 shows the positive level clamper circuit with positive biasing voltage. The operation of the circuit is similar to positive level clamper without biasing voltage. The diode D is forward biased during first negative half cycle and the capacitor C is charged to voltage, $(V_m + V_R)$ with the polarities as shown in the figure. Once capacitor is charged the diode is reverse biased in negative half and the positive half cycles. The capacitor does not discharge once it is charged due to large time constant of the circuit.

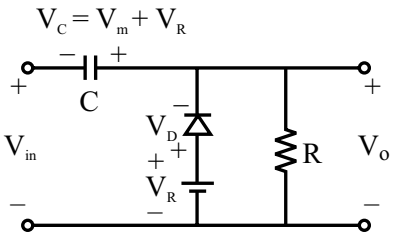


Fig.75 Positive level clamper circuit with positive biasing voltage

The output voltage can be written by applying KVL in outer loop of the circuit as under,

$V_{in} + V_C - V_o = 0$ (116)

$\Rightarrow$ $V_o = V_{in} + V_C$ (117)

The voltage across charged capacitor ,

$V_C = V_m + V_R$ (118)

$\Rightarrow$ $V_o = V_{in} + (V_m + V_R)$ (119)

For sinusoidal input, $V_{in} = V_m \sin \omega t$ (120)

$\Rightarrow$ $V_o = V_m \sin \omega t + (V_m + V_R)$ (121)

It is seen from above equation that output voltage is shifted by $(V_m + V_R)$ as compared to the input voltage of the circuit.

The waveforms of input and output signals of negative level clamper with positive biasing voltage is shown in Fig. 76. It is seen from waveform of output signal that the output signal is shifted vertically by $(V_m + V_R)$ as compared to the input signal.

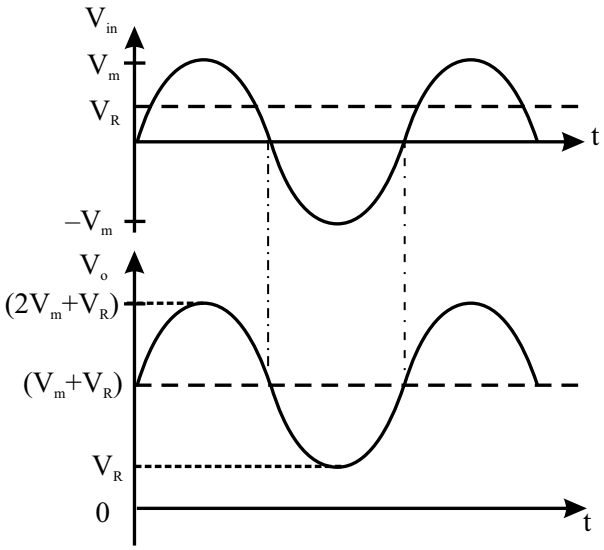


Fig.76 The waveforms of input and output signals of positive level clamper circuit with positive biasing voltage

Circuit 3 : Positive Level Clamper With Negative Biasing Voltage

Fig. 77 shows the positive level clamper circuit with negative biasing voltage. The capacitor C is charged to voltage, $(V_m - V_R)$ during first positive half cycle. Once capacitor is charged it does not discharge due to large time constant of the circuit.

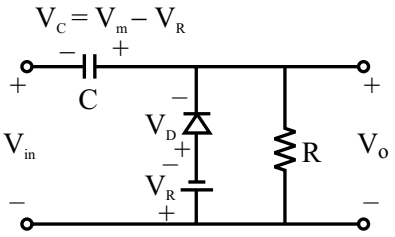


Fig.77 Positive level clamper circuit with negative biasing voltage

The output voltage can be written by applying KVL in outer loop of the circuit as under,

$$V_{in} + V_C - V_o = 0 \quad (122)$$

$$\Rightarrow \quad V_o = V_{in} + V_C \quad (123)$$

The voltage across charged capacitor ,

$$V_C = V_m - V_R \quad (124)$$

$$\Rightarrow \quad V_o = V_{in} + (V_m - V_R) \quad (125)$$

For sinusoidal input, $V_{in} = V_m \sin \omega t \quad (126)$

$$\Rightarrow \quad V_o = V_m \sin \omega t + (V_m - V_R) \qquad (127)$$

It is seen from above equation that output voltage is shifted by + $(V_m - V_R)$ as compared to the input voltage of the circuit.

The waveforms of input and output signals of positive level clamper with negative biasing voltage is shown in Fig. 78. It is seen from waveform of output signal that the output signal is shifted vertically by $+(V_m - V_R)$ as compared to the input signal.

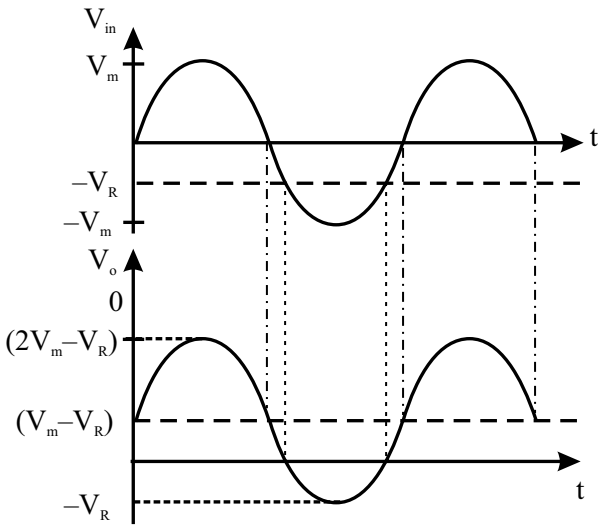
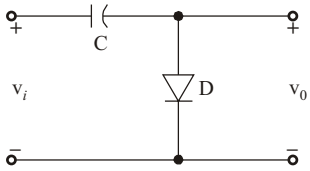


Fig.78 The waveforms of input and output signals of positive level clamper circuit with negative biasing voltage

Note : *In clamping circuits the polarity of the voltage across capacitor in decided by the half cycle of input signal during which diode is forward biased and magnitude (not polarity) of voltage across capacitor is decided by the difference between peak of input voltage and reference voltage V_R.*

Example 11

The input voltage, v_i is $4 + 3 \sin \omega t$. Assuming all elements to be ideal, the average of the output voltage v_0 in figure is

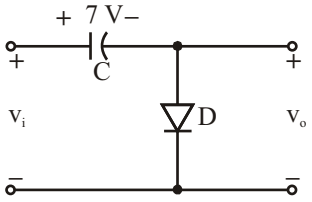


(a) –3 V (b) +3 V

(c) –7 V (d) +7 V

GATE(IN/1999/2M)

Solution : Ans.(a)



Given, $v_{in} = 4 + 3 \sin \omega t$

The diode is forward biased during positive half cycle. During first positive half cycle the capacitor gets charged to 7 V. Then onward the diode remains OFF and the output of circuit is,

$$v_o = -7 + v_{in}$$

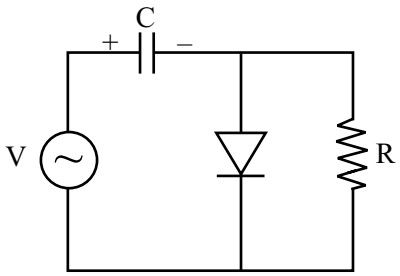
$$\Rightarrow \quad v_o = -7 + 4 + 3 \sin \omega t$$

$$= -3 + 3 \sin \omega t$$

The average value of sinusoidal component of output voltage is zero. So the average value of output voltage is –3V

Example 12

If the circuit shown has to function as a clamping circuit, then which one of the following conditions should be satisfied for the sinusoidal signal of period T?

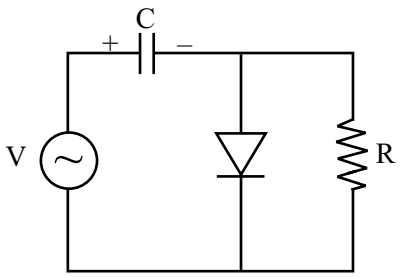


(a) RC << T (b) RC = 0.35 T

(c) RC ≈ T (d) RC >> T

GATE(EC-II/2015/1M)

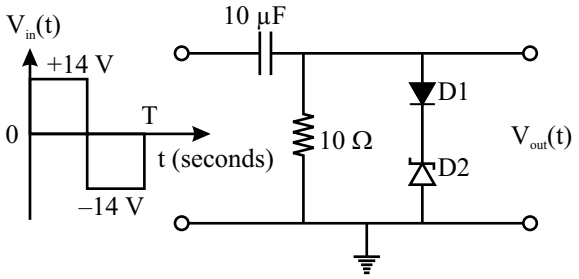
Solution : Ans. (d)



For above circuit to behave as a clamping circuit the capacitor should not discharged once it is charged in first cycle of input voltage waveform. This is possible only when RC >> T.

Example 13

In the figure, D1 is a real silicon pn junction diode with a drop of 0.7V under forward bias condition and D2 is a Zener diode with breakdown voltage of –6.8 V. The input $V_{in}(t)$ is a periodic square wave of period T, whose one period is shown in the figure.



Assuming $10\tau << T$, where τ is the time constant of the circuit, the maximum and minimum values of the output waveform are respectively,

(a) 7.5 V and –20.5 V

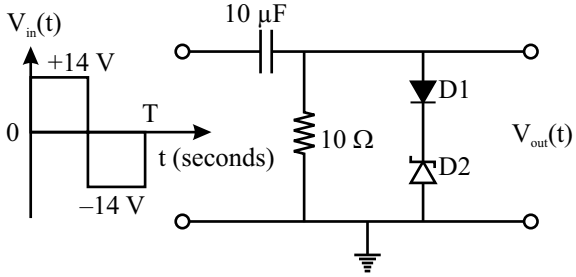
(b) 6.1 V and –21.9 V

(c) 7.5 V and – 21.2 V

(d) 6.1 V and –22.6 V

GATE(EC-II/2017/1M)

Solution : Ans. (a)



During positive half cycle of input voltage the diode D_1 is forward biased and diode D_2 is reverse biased. Since input voltage during positive half cycle is more than sum of forward voltage drop of D_1 and reverse breakdown voltage of D_2 so the output voltage is clipped at

$$V_{out} = V_{D_1} + V_z = 0.7 + 6.8$$

$$= 7.5V$$

The capacitor gets charged to a voltage V_c during positive half cycle which is given by

$$V_c = 14 - 7.5 = 6.5V$$

The left plate of capacitor becomes positive and right plate becomes negative. During negative half cycle the diode D_1 is reverse biased and behaves like an open circuit. Then output voltage during negative half cycle will be,

$$V_{out} = -6.5 - 14 = -20.5\ V$$

Therefore, the maximum and minimum values of the output waveform are 7.5 V and –20.5 V, respectively.

1.4 Voltage Doubler Circuit

The voltage double circuit can be half wave or full wave voltage double. Both half wave and full wave voltage doubler circuits are discussed in the following sections.

A. Half wave voltage doubler

The circuit shown in Fig. 79 is called a half wave voltage doubler circuit. The input signal of the circuit is assumed to be a sinusoidal signal. During first positive half cycle of input voltage the diode D_1 is forward biased and capacitor C_1 gets charged to V_m with polarity as shown in the figure. Once the capacitor C_1 is charged to peak of input voltage it keeps the diode D_1 under reverse biased condition. During first negative half cycle of input voltage, the diode D_2 is forward biased and capacitor C_2 is charged to a voltage level equal to sum of peak of input voltage and voltage of capacitor C_1. Since, capacitor C_1 is already charged to peak of input voltage (V_m) so the capacitor C_2 is charged to a total voltage of $2V_m$ with the polarities as shown in the figure. Thus the output voltage is double of peak value of input voltage and circuit performs as doubling operation.

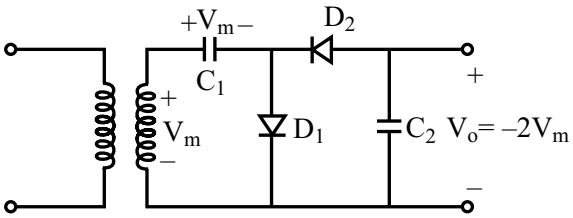


Fig. 79 Half wave voltage doubler circuit.

B. Full wave voltage doubler

Fig.80 illustrates a full wave voltage doubler circuit. During positive half of supply voltage the diode D_1 is forward biased and D_2 is reverse biased so the capacitor C_1 is charged to peak of input voltage, V_m. with upper plate positive and lower plate negative. During negative half of supply voltage the diode D_1 is reverse biased and diode D_2 is forward biased so the capacitor C_2 gets charged to peak of supply voltage with polarities as shown in the figure. The output voltage is sum of voltages across the capacitors. As both capacitors are charged to peak of supply voltage with additive polarities therefore, the output voltage is double of peak of input voltage of the circuit.

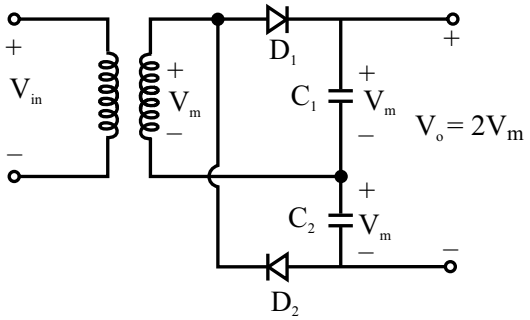
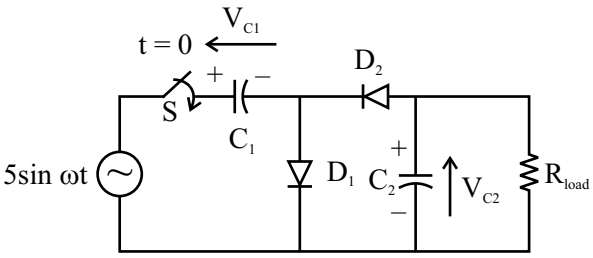


Fig.80 Full wave voltage doubler circuit

Example 14

In the voltage doubler circuit shown in the figure, the switch 'S' is closed at t = 0. Assuming diodes D_1 and D_2 to be ideal, load resistance to be infinite and initial capacitor voltages to be zero, the

steady state voltage across capacitors C_1 and C_2 will be



(a) $V_{C1} = 10$ V, $V_{C2} = 5$ V

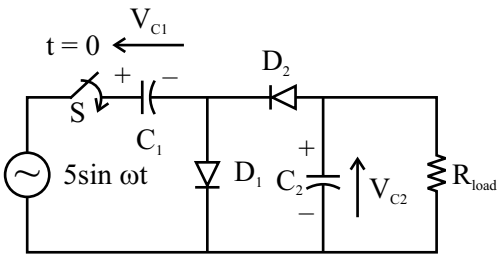
(b) $V_{C1} = 10$ V, $V_{C2} = -5$ V

(c) $V_{C1} = 5$ V, $V_{C2} = 10$ V

(d) $V_{C1} = 5$ V, $V_{C2} = -10$ V

GATE(EE/2008/2 M)

Solution : Ans.(d)



During negative very first negative half cycle, the diode D_1 is forward biased and capacitor C_1 gets charged to peak of input voltage such that

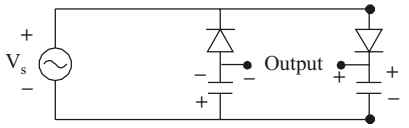
$$V_{C1} = 5 \text{ V}$$

and during positive half cycle just after the first negative half cycle, the diode D_1 is reverse biased and diode D_2 is forward biased and capacitor C_2 gets charged to V_{C1} plus peak of input voltage. So,

$$V_{C2} = -(V_{C1} + 5 \text{ V}) = -10 \text{ V}.$$

Example 15

The circuit shown in Figure is best described as a



(a) bridge rectifier

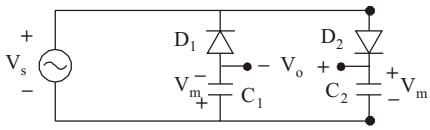
(b) ring modulator

(c) frequency discriminatory

(d) voltage doubler

GATE(EC/2003/1M)

Solution : Ans.(d)

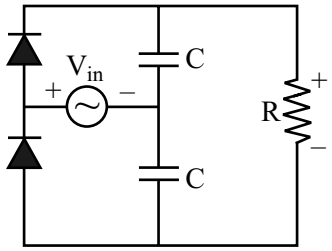


During positive half cycle of input the D_2 is ON and D_1 is OFF so C_2 gets charged to positive peak

of V_s and during negative half cycle of input D_1 is ON and D_2 is OFF so C_1 gets charged to negative peak of V_s . So, output voltage $V_o = 2V_m$. Since output voltage is double of peak of input voltage so circuit behaves like a voltage doubler.

Example 16

In the following circuit, the input voltage V_{in} is 100 sin (100 πt). For 100πRC = 50, the average voltage across R (in volts) under steady-state is nearest to

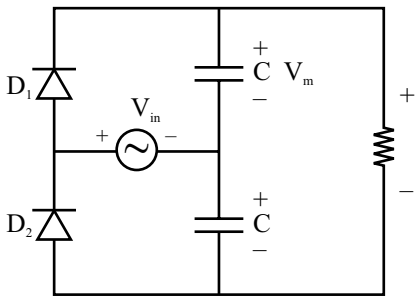


(a) 100 (b) 31.8

(c) 200 (d) 63.6

GATE(EE-II/2015/1M)

Solution : Ans. (c)



Given circuit is a voltage doubler circuit. The time constant of the circuit RC/2 should be very large as compared to time period of input voltage V_{in} for the circuit to work as voltage doubler.

Given, $V_{in} = 100 \sin 100\pi t$

Frequency of input signal,

$$\omega = \frac{2\pi}{T} = 100\pi$$

$$\Rightarrow \quad T = \frac{1}{50} = 0.02s$$

Also, $100\,\pi RC = 50$

$$RC = 0.159\ s$$

$\therefore$ Time contents of the circuit. RC/2 $= 0.0795s$

As time constant of circuit RC/2 > T so given circuit works like a voltage doubler. The operation of the circuit as a voltage doubler can be explained as follows

Case-I : During the half cycle

During first positive half cycle of the input voltage, the diode D_1 is forward biased and diode D_2 is reverse biased and capacitor C_1 gets charge to peak of supply voltage with upper plate positively charged. After first positive half cycle the does not charge due to large time constant and capacitor voltage becomes more than the supply voltage and diode D_1 is also reverse biased.

Case-II : During negative half cycle

During first negative half cycle, the diode D_1 is reverse biased and D_2 is forward biased and capacitor C_2 gets charged to peak of supply voltage with upper end positive and lower end negative. After peak of negative half cycle the capacitor voltage becomes more than the supply voltage and diode D_2 is also reverse biased.

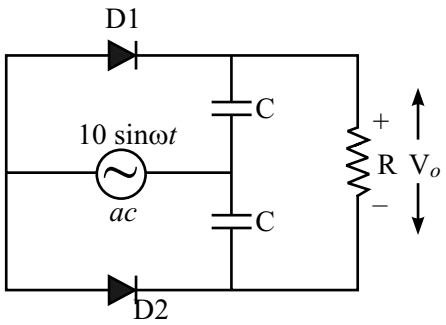
The overall voltage across the resistance R becomes as under,

$$V_R = V_{C1} + V_{C2} = V_m + V_m$$

$$\Rightarrow \quad V_R = 2V_m = 2 \times 100 = 200 \text{ V}$$

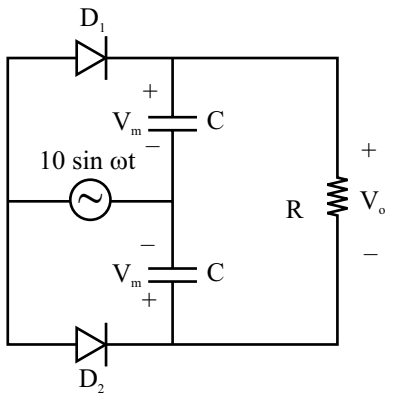
Example 17

The diodes D_1 and D_2 in the figure are ideal and the capacitors are identical. The product RC is very large compared to the time period of the ac voltage. Assuming that the diodes do not breakdown in the reverse bias, the output voltage V_o (in volt) at the steady state is .....



GATE(EC-III/2016/1M)

Solution : 0.0



Given, RC >> time period of input voltage.

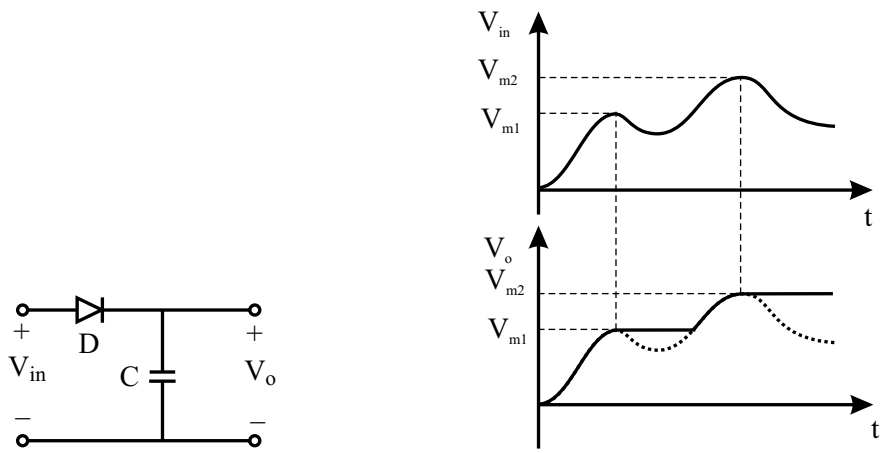
During first positive half cycle of input voltage, the diode both diodes D_1 and D_2 are forward biased. The upper capacitor C is charged to peak of input voltage i.e. 10 V with upper plate positive and lower plate negative and the lower capacitor C is charged to peak of input voltage i.e. 10 V with lower plate positive and upper plate negative . During negative half cycle of input voltage, both diodes are reverse biased. However, the capacitors do not discharge through R during negative half cycle due to large time constant RC as compared to time period of input signal. Thus capacitors remain charged with same polarities as during the positive half cycle. Thus after very first cycle of input voltage the both capacitors remain charged with peak of input voltage but with opposite polarities.

The output voltage across 'R' can be given as,

$$V_o = V_m - V_m = 10 - 10 = 0$$

1.5 Peak Detector Circuit

A peak detector circuit consists of a series connected diode and shunt connected capacitor. Fig. 81(a) shows the positive peak detector circuit using a diode. Let input applied to the peak detector circuit has two peaks as shown in Fig. 81(b). The diode D is forward biased for the part oa of input signal and output voltage same as input voltage for this part. For part ab of input waveform the diode is reverse biased and capacitor is charged to first peak of input voltage, V_{m1}. For part bc of input voltage the diode is again forward biased and output voltage follows the input voltage. At point capacitor is charged to second peak ,V_{m2}, of input voltage and diode D is reverse biased for remaining part cd of input voltage. Therefore, output voltage is equal to last peak value of input voltage. A negative peak detector circuit can also be implemented by simply reversing the connections of the diode D.



(a) Peak detector circuit (b) Input and output voltage waveforms.

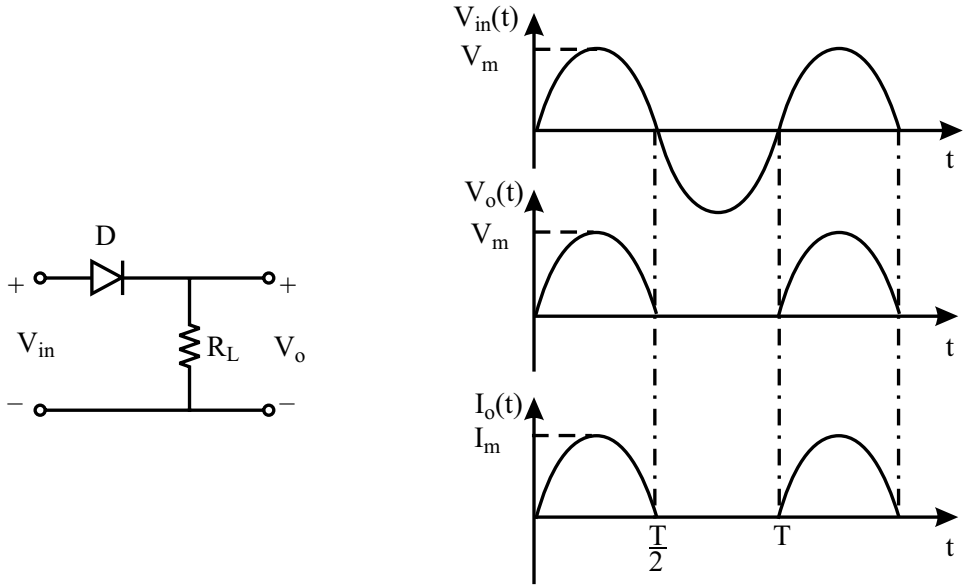
Fig.81 Positive peak detector circuit and its input and output signals.

1.6 Rectifiers

Rectifier circuits are used to convert an AC signal to a DC signal. The rectifiers are of two types called half wave and full wave rectifiers.

1.6.1 Half wave Rectifier

A half wave rectifier consists of a diode in series with a load as shown in Fig. 82(a). The diode is forward biased during positive half of input voltage and reverse biased during negative half of input voltage.



(a) Half wave rectifier **(b) Input voltage, output voltage and output current**

Fig.82 Positive peak detector circuit and its input and output signals.

So, output voltage is same as input voltage during positive half cycle and it is zero during negative half cycle of input voltage. Fig. 82(b) shows the waveforms of input voltage, output voltage and output current of the half wave rectifier.

I. Average Output Current

The average value of periodic output current of the signal can be given by,

$$I_{av} = \frac{1}{T}\int_0^T i_o(t)\,dt \tag{128}$$

From the waveform of output current,

$$\begin{aligned} i_o(t) &= I_m \sin \omega t \quad ; \quad 0 < t < T/2 \\ &= 0 \quad ; \quad T/2 < t < T \end{aligned}$$

$$\Rightarrow \quad I_{av} = \frac{1}{T}\int_0^{\frac{T}{2}} I_m \sin \omega t\, dt = \frac{I_m}{T}\left[\frac{-\cos \omega t}{\omega}\right]_0^{\frac{T}{2}} \tag{129}$$

$$\Rightarrow \quad I_{av} = \frac{I_m}{2\pi}[-\cos\pi + \cos 0] = \frac{I_m}{\pi} \tag{130}$$

II. Root Mean Square (RMS) or Effective Value of Output Current

The RMS value of the period current is given by,

$$I_{rms} = \left[\frac{1}{T}\int_0^{T/2} i_0^2(t)\,dt\right]^{\frac{1}{2}} \tag{131}$$

$$\Rightarrow \quad I_{rms} = \left[\frac{1}{T}\int_0^{\frac{T}{2}} I_m^2 \sin^2 \omega t\,dt\right]^{\frac{1}{2}} = \left[\frac{I_m^2}{2T}\int_0^{\frac{T}{2}}(1-\cos 2\omega t\,dt)\right]^{\frac{1}{2}} \tag{132}$$

$$\Rightarrow \quad I_{rms} = \left[\frac{I_m^2}{2T}\left[t - \frac{\cos 2\omega t}{2\omega}\right]_0^{T/2}\right]^{\frac{1}{2}} = \frac{I_m}{2} \tag{133}$$

The peak value of current can be given in terms of peak value of voltage as under,

For ideal diode, $$I_m = \frac{V_m}{R_L} \tag{134}$$

For non ideal diode, $$I_m = \frac{V_m}{R_L + R_f} \tag{135}$$

Where, R_f is forward resistance of the diode and R_L is load resistance. The value of R_f is zero for an ideal diode.

III. Average Output Voltage

The average or DC value of output voltage of the rectifier is obtained similar to current of the rectifier as under,

$$V_{av} = \frac{1}{T}\int_0^T V_o(t)\,dt \tag{136}$$

From the waveform of output current,

$$\begin{aligned} v_o(t) &= V_m \sin \omega t \quad ; \quad 0 < t < T/2 \\ &= 0 \quad ; \quad T/2 < t < T \end{aligned}$$

$$\Rightarrow \quad V_{av} = \frac{1}{T}\int_0^{\frac{T}{2}} V_m \sin\omega t\,dt = \frac{V_m}{\pi} \tag{137}$$

IV. Root Mean Square (RMS) or Effective Value of Output Voltage

The output voltage of the rectifier can be given as under,

$$V_{rms} = \left[\frac{1}{T}\int_0^T v_0^2(t)\,dt\right]^{\frac{1}{2}} \tag{138}$$

$$\Rightarrow \quad V_{rms} = \left[\frac{1}{T}\int_0^{T/2} V_m^2 \sin^2 \omega t\, dt\right]^{\frac{1}{2}} \tag{139}$$

$$\Rightarrow \quad V_{rms} = \left[\frac{V_m^2}{2T}\int_0^{T/2} (1-\cos 2\omega t)\,dt\right]^{\frac{1}{2}} \tag{140}$$

$$\Rightarrow \quad V_{rms} = \left[\frac{V_m^2}{2T}\left[t - \frac{\cos 2\omega t}{2\omega}\right]_0^{T/2}\right]^{\frac{1}{2}} = \frac{V_m}{2} \tag{141}$$

V. Average Output Voltage For Non-ideal Diode

If diode is non-ideal with a forward resistance , R_f.. The equivalent circuit of half wave rectifier with non-ideal diode can be drawn as shown in the figure below,

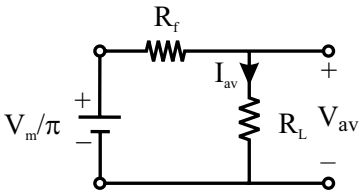


Fig.83 Equivalent circuit of half wave rectifier with non-ideal diode

The average output voltage of the rectifier can be given by,

$$V_{av} = \frac{V_m}{\pi} - I_{av}\, R_f \tag{142}$$

The average current for a rectifier with non-ideal diode can be given as under,

$$I_{av} = \frac{I_m}{\pi} = \frac{\frac{V_m}{R_L + R_f}}{\pi} = \frac{V_m}{\pi(R_L + R_f)} \tag{143}$$

$$\Rightarrow \quad V_{av} = \frac{V_m}{\pi} - \frac{V_m}{\pi(R_L + R_f)}.R_f \tag{144}$$

$$\Rightarrow \quad V_{av} = \frac{V_m}{\pi}\left[\frac{R_L}{R_f + R_L}\right] \tag{145}$$

Example 18

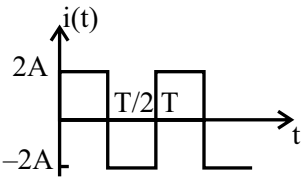
The RMS value of a half-wave rectified symmetrical square wave current of 2 A is

(a) $\sqrt{2}$A (b) 1 A

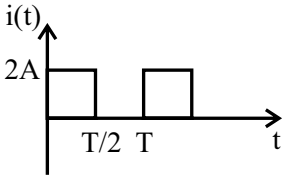
(c) $1/\sqrt{2}$A (d) $\sqrt{3}$A

GATE(EE/1999/1 M)

Solution : ***Ans.(a)***



When square wave shown above is given to a half wave rectifier the output of rectifier is pulse wave as shown below



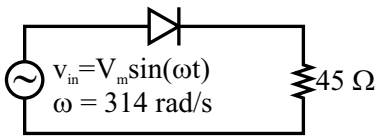
R.M.S. value of current wave form,

$$I_{rms} = \left[\frac{1}{T}\int_0^T i_L^2(t)dt\right]^{1/2} = \left[\frac{1}{T}\int_0^{T/2}(2)^2 dt\right]^{1/2}$$

$$\Rightarrow \quad I_{rms} = \left[\frac{4}{T}\times\frac{T}{2}\right]^{1/2} = \sqrt{2}\text{A}$$

Example 19

The forward resistance of the diode shown in figure is 5Ω and the remaining parameters are same as those of ideal diode. The dc component of the source current is

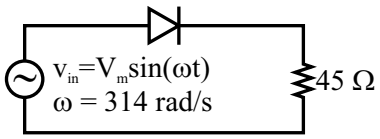


(a) $\frac{V_m}{50\pi}$ (b) $\frac{V_m}{50\pi\sqrt{2}}$

(c) $\frac{V_m}{100\pi\sqrt{2}}$ (d) $\frac{2V_m}{50\pi}$

GATE(EE/2002/1 M)

Solution : ***Ans.(a)***



The average output voltage of half wave rectifier shown above will be,

$$V_{dc} = \frac{V_m}{\pi}$$

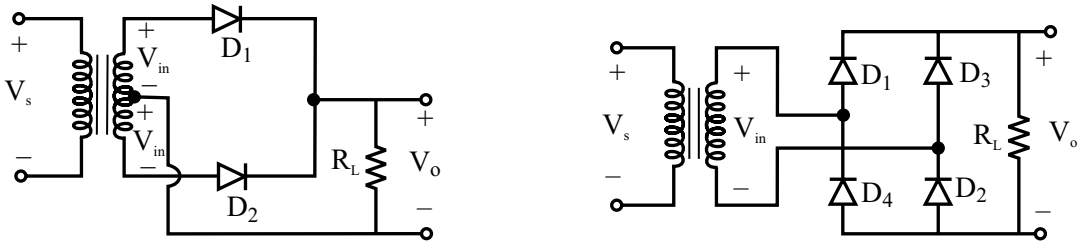
DC component of load current is same as dc load current,

So, DC component of source current is given by,

$$I_{dc} = \frac{V_{dc}}{r+R} = \frac{V_{dc}}{5+45} = \frac{V_m}{\pi\, 50} = \frac{V_m}{50\,\pi}$$

1.6.2 Full wave Rectifier

The full wave rectifiers are of two types called centre tap type and bridge type. The centre tap rectifier makes used of transformer with centre tap and two diodes where as bridge type rectifier makes use of bridge circuit consisting of four diodes with one diode connected in each arm of the bridge. Fig. 84 shows the centre tap type and bridge type full wave rectifiers.



(a) Centre tap type **(b) Bridge type**

Fig.84 Centre tap and Bridge type full wave rectifiers

The waveforms of input voltage, output current and output voltage are similar for both centre tap and bridge type rectifiers. The main difference is centre tap has one diode in path of current and bridge type has two diodes. The maximum or peak inverse voltage is V_m for centre tap and $2V_m$ for bridge type of rectifier. Fig.85 shows the waveforms input voltage, output current and output voltage of full wave rectifiers.

I. Average Output Current

The output current is period with time period of T/2. The average value of output current can be given by,

$$I_{av} = \frac{2}{T}\int_0^{T/2} i_o(t)\, dt \qquad (146)$$

From the waveform, $i_o(t) = I_m \sin \omega t \quad ; \quad 0 < t < T/2$

$$\Rightarrow \quad I_{av} = \frac{2}{T}\int_0^{\frac{T}{2}} I_m \sin \omega t\, dt = \frac{2I_m}{T}\left[\frac{-\cos \omega t}{\omega}\right]_0^{\frac{T}{2}} \qquad (147)$$

$$\Rightarrow \quad I_{av} = \frac{I_m}{\pi}[-\cos\pi + \cos 0] = \frac{2I_m}{\pi} \tag{148}$$

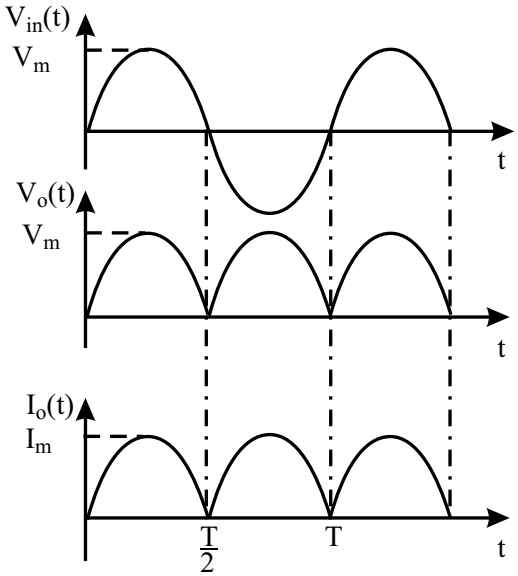


Fig. 85 Waveforms of input voltage, output voltage and output current of full wave rectifiers.

II. Root Mean Square (RMS) or Effective Value of Output Current

The RMS value of the output current is given by,

$$I_{rms} = \left[\frac{2}{T}\int_0^{T/2} i_0^2(t)\,dt\right]^{\frac{1}{2}} \tag{149}$$

$$\Rightarrow \quad I_{rms} = \left[\frac{2}{T}\int_0^{\frac{T}{2}} I_m^2 \sin^2 \omega t\,dt\right]^{\frac{1}{2}} = \left[\frac{I_m^2}{T}\int_0^{\frac{T}{2}} (1-\cos 2\omega t\,dt)\right]^{\frac{1}{2}} \tag{150}$$

$$\Rightarrow \quad I_{rms} = \left[\frac{I_m^2}{T}\left[t - \frac{\cos 2\omega t}{2\omega}\right]_0^{T/2}\right]^{\frac{1}{2}} = \frac{I_m}{\sqrt{2}} \tag{151}$$

The peak value of current can be given as,

For ideal diode, $I_m = \frac{V_m}{R_L}$; for both centre tap and bridge type (152)

For non ideal diode, $I_m = \frac{V_m}{R_L + R_f}$; For centre tap type (153)

$= \frac{V_m}{R_L + 2R_f}$; For bridge type (154)

III. Average Output Voltage

The average of output voltage of the rectifier is obtained as under,

$$V_{av} = \frac{2}{T}\int_0^{T/2} V_o(t)\,dt \tag{155}$$

From the waveform of output current,

$$v_o(t) = V_m \sin \omega t \quad ; \quad 0 < t < T/2$$

$$\Rightarrow \quad V_{av} = \frac{2}{T}\int_0^{\frac{T}{2}} V_m \sin \omega t\,dt = \frac{2V_m}{\pi} \tag{156}$$

IV. Root Mean Square (RMS) Value of Output Voltage

The output voltage of the rectifier can be given as under,

$$V_{rms} = \left[\frac{2}{T}\int_0^{T/2} v_0^2(t)\,dt\right]^{\frac{1}{2}} \tag{157}$$

$$\Rightarrow \quad V_{rms} = \left[\frac{2}{T}\int_0^{T/2} V_m^2 \sin^2 \omega t\,dt\right]^{\frac{1}{2}} \tag{158}$$

$$\Rightarrow \quad V_{rms} = \left[\frac{V_m^2}{T}\int_0^{T/2} (1-\cos 2\omega t)\,dt\right]^{\frac{1}{2}} \tag{159}$$

$$\Rightarrow \quad V_{rms} = \left[\frac{V_m^2}{T}\left[t - \frac{\cos 2\omega t}{2\omega}\right]_0^{T/2}\right]^{\frac{1}{2}} = \frac{V_m}{\sqrt{2}} \tag{160}$$

V. Average Output Voltage For Non-ideal Diode

The equivalent circuit of bridge type full wave rectifier with non-ideal diode can be drawn as shown in the figure below,

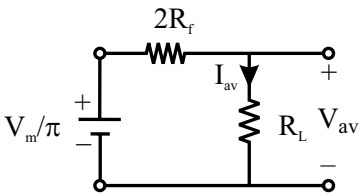


Fig.86 Equivalent circuit of bridge type full wave rectifier with non-ideal diode

There are two diodes in the path of current therefore, a resistance $2R_f$ is connected in series with the DC source in the equivalent circuit of the rectifier.

The average output voltage of the rectifier can be given by,

$$V_{av} = \frac{2V_m}{\pi} - I_{av}(2R_f) \tag{161}$$

The average current for a rectifier with non-ideal diode can be given as under,

$$I_{av} = \frac{2I_m}{\pi} = \frac{2 \times \frac{V_m}{R_L + 2R_f}}{\pi} = \frac{2V_m}{\pi(R_L + 2R_f)} \quad (162)$$

$$\Rightarrow \quad V_{av} = \frac{2V_m}{\pi} - \frac{2V_m}{\pi(R_L + 2R_f)} . 2R_f \quad (163)$$

$$\Rightarrow \quad V_{av} = \frac{2V_m}{\pi} \left[\frac{R_L}{2R_f + R_L} \right] \quad (164)$$

For centre tap type full wave rectifier there is one diode in series with the load so the resistance $2R_f$ in series of DC source in equivalent circuit is replaced by R_f and the average output voltage becomes as under,

$$\Rightarrow \quad V_{av} = \frac{2V_m}{\pi} \left[\frac{R_L}{R_f + R_L} \right] \quad (165)$$

1.6.3 Performance Parameters of Rectifiers

I. Peak Inverse Voltage (PIV) :

Peak inverse voltage of rectifier is maximum reverse voltage which appears across the diode under reverse bias condition. Mathematically it is given by,

$$\begin{aligned} PIV &= V_m \quad ; \text{For half wave rectifier} \\ &= V_m \quad ; \text{For full wave bridge type} \\ &= 2V_m \quad ; \text{For full wave centre tap type} \end{aligned}$$

II. Voltage Regulation :

Voltage regulation of the rectifier is defined as percentage voltage drop in output voltage from no load to full load. Mathematically it is given as,

$$V.R. = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 \quad (166)$$

The output voltage of rectifier reduces with increase in load current due to forward resistance of the diode. The variation in voltage with load current is drawn in Fig. 87

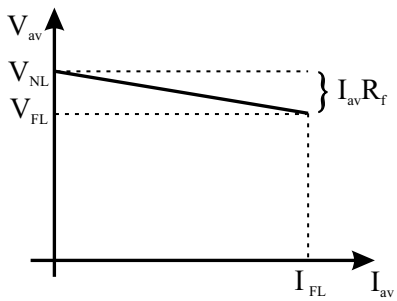


Fig.87 Variation in output voltage with load current in rectifiers with non-ideal diodes.

For half wave rectifier :

No load voltage, $$V_{NL} = \frac{V_m}{\pi} \quad (167)$$

Full load voltage, $$V_{FL} = \frac{V_m}{\pi} - I_{av} R_f = \frac{V_m}{\pi}\left[\frac{R_L}{R_f + R_L}\right] \quad (168)$$

$$\therefore \quad V.R. = \frac{\frac{V_m}{\pi} - \frac{V_m}{\pi}\left[\frac{R_L}{R_f + R_L}\right]}{\frac{V_m}{\pi}\left[\frac{R_L}{R_f + R_L}\right]} \times 100 = \frac{R_f}{R_L} \times 100 \quad (169)$$

For full wave bridge type rectifier :

No load voltage, $$V_{NL} = \frac{2V_m}{\pi} \quad (170)$$

Full load voltage, $$V_{FL} = \frac{2V_m}{\pi} - I_{av}(2R_f) = \frac{2V_m}{\pi}\left[\frac{R_L}{2R_f + R_L}\right] \quad (171)$$

$$\therefore \quad V.R. = \frac{\frac{2V_m}{\pi} - \frac{2V_m}{\pi}\left[\frac{R_L}{2R_f + R_L}\right]}{\frac{2V_m}{\pi}\left[\frac{R_L}{2R_f + R_L}\right]} \times 100 = \frac{2R_f}{R_L} \times 100 \quad (172)$$

For full wave centre tap type rectifier :

In centre tap type rectifier there is only one diode in path of current so resistance $2R_f$ is replaced by R_f.

$$V.R. = \frac{R_f}{R_L} \times 100 \quad (173)$$

Note : i. For ideal diode $R_f = 0$ so ideally V.R. = 0 for all types of rectifiers.

ii. Voltage regulation of full wave bridge rectifier is double in the case of half wave rectifier and centre tape full wave rectifier. So voltage regulation of full wave bridge rectifier is poorer than half wave and centre tape rectifier.

III. Form Factor

Form factor is defined as the ratio of rms value of output voltage to its average value. Mathematically, it is given by,

$$\text{Form factor, FF} = \frac{V_{rms}}{V_{av}} \quad (174)$$

For half wave rectifier :

$$FF = \frac{\frac{V_m}{2}}{\frac{V_m}{\pi}} = \frac{\pi}{2} = 1.57 \quad (175)$$

For full wave rectifiers:

$$FF = \frac{V_{o\,rms}}{V_{o\,av}} = \frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{\pi}} = \frac{\pi}{2\sqrt{2}} = 1.11 \quad (176)$$

IV. Ripple Factor

Ripple factor is defined as the ratio of rms value of ac ripple in output to average value of the output voltage. Mathematically it is given as ,

Ripple factor, $$RF = \frac{V_{o\,ac\,rms}}{V_{av}} \quad (177)$$

Where $V_{o\,ac\,rms}$ is rms value of ac ripple component in the output voltage.

The rms value of ac ripple component in output voltage can be given as

$$V_{o\,ac\,rms} = \sqrt{V_{rms}^2 - V_{av}^2} \quad (178)$$

$$\Rightarrow \quad RF = \frac{\sqrt{V_{rms}^2 - V_{av}^2}}{V_{av}} = \sqrt{\frac{V_{rms}^2}{V_{av}^2} - 1} = \sqrt{(FF)^2 - 1} \quad (179)$$

For half wave rectifier:

$$R.F. = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21 \quad (180)$$

For full wave rectifiers:

$$R.F. = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.48 \quad (181)$$

IV. Rectifier Efficiency

Rectifier efficiency is defined by the ratio of output dc power to the input ac power of the rectifier.

$$\eta = \frac{\text{Output dc Power}}{\text{Input ac Power}} = \frac{P_{o\,dc}}{P_{i\,ac}} \quad (182)$$

For half wave rectifier:

The dc output power of rectifier can be given by,

$$P_{o,dc} = I_{av}^2 R_L \quad (183)$$

The ac input power of rectifier is given by,

$$P_{i\,ac} = I_{in\,rms}^2 (R_L + R_f) \quad (184)$$

The rms value of input current is same as rms value of output current of the rectifier. Therefore, ac input power can be given as,

$$\Rightarrow \quad P_{i\,ac} = I_{rms}^2 . R_f + I_{rms}^2 R_L \quad (185)$$

$$\therefore \quad \eta = \frac{I_{av}^2 R_L}{I_{rms}^2 R_f + I_{rms}^2 R_L} \times 100 \quad (186)$$

$$\Rightarrow \quad \eta = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{2}\right)^2 R_f + \left(\frac{I_m}{2}\right)^2 R_L} \times 100 \quad (187)$$

$$\boxed{\eta = \frac{4}{\pi^2} \cdot \frac{R_L}{R_f + R_L} \times 100} \quad (188)$$

If diode is ideal, $R_f = 0$

$$\therefore \quad \boxed{\eta = \eta_{max} = \frac{4}{\pi^2} \times 100 = 40.5\%} \quad (189)$$

If source resistance is also taken into consideration then R_f is replaced by $R_s + R_f$

$$\boxed{\eta = \frac{4}{\pi^2} \cdot \frac{R_L}{R_f + R_L + R_s} \times 100} \quad (190)$$

For ideal diode, $$\eta = \frac{4}{\pi^2} \cdot \frac{R_L}{R_L + R_s} \times 100 \quad (191)$$

For full wave bridge type rectifier:

The ac input power of rectifier is given by,

$$P_{i\,ac} = I_{rms}^2 . (2R_f) + I_{rms}^2 R_L \quad (192)$$

$$\therefore \quad \eta = \frac{I_{av}^2 R_L}{I_{rms}^2 (2R_f) + I_{rms}^2 R_L} \times 100 \quad (193)$$

$$\Rightarrow \quad \eta = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m}{\sqrt{2}}\right)^2 (2R_f) + \left(\frac{I_m}{\sqrt{2}}\right)^2 R_L} \times 100 \tag{194}$$

$$\Rightarrow \quad \boxed{\eta = \frac{8}{\pi^2} \times \frac{R_L}{R_L + 2R_f} \times 100} \tag{195}$$

If source resistance is also taken into account,

$$\boxed{\eta = \frac{8}{\pi^2} \cdot \frac{R_L}{2R_f + R_L + R_s} \times 100} \tag{196}$$

For centre tap type rectifier, resistance $2R_f$ is replaced by R_f. Then the rectifier efficiency for centre tap type rectifier will be,

$$\boxed{\eta = \frac{8}{\pi^2} \cdot \frac{R_L}{R_f + R_L + R_s} \times 100} \tag{197}$$

Note : Maximum efficiency of full wave rectifier is twice the maximum efficiency of half wave rectifier.

(v) Transformer Utilization Factor (TUF)

It is defined by the ratio of power delivered to the load and volt-ampere delivered by secondary side of transformer. Mathematically,

$$\text{TUF} = \frac{I_{av}^2 R_L}{V_{in\,rms} \cdot I_{in\,rms}} \tag{198}$$

As the rms value of input current is same as rms value of output current of the rectifier, therefore, TUF can be given as,

$$\Rightarrow \quad \text{TUF} = \frac{I_{av}^2 R_L}{V_{in\,rms} \cdot I_{rms}} \tag{199}$$

For Half Wave Rectifier:

$$\text{TUF} = \frac{\left[\frac{V_m}{\pi(R_f + R_L)}\right]^2 \times R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2}} = \frac{\frac{V_m^2}{\pi^2}\left[\frac{1}{R_f + R_L}\right]^2 . R_L}{\frac{V_m}{\sqrt{2}} \times \frac{V_m}{2(R_f + R_L)}} \tag{200}$$

$$\Rightarrow \quad \text{TUF} = \frac{2\sqrt{2}}{\pi^2} \cdot \frac{R_L}{R_f + R_L} \tag{201}$$

For ideal diode, $R_f = 0$

$$\therefore \quad \boxed{TUF_{max} = \frac{2\sqrt{2}}{\pi^2} = 0.286} \tag{202}$$

For Full Wave Bridge rectifier:

$$TUF = \frac{\left(\frac{2V_m}{\pi} \times \frac{1}{2R_F + R_L}\right)^2 \times R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{1}{\sqrt{2}} \times \frac{V_m}{2R_F + R_L}} = \frac{8}{\pi^2} \times \frac{R_L}{R_L + 2R_f} \tag{203}$$

$$\Rightarrow \quad TUF = \frac{8}{\pi^2} \times \frac{R_L}{R_L + 2R_f} \tag{204}$$

For Full Wave Centre Tap type rectifier:

Replace $2R_f$ by R_f in above equation for centre tap type rectifier as under,

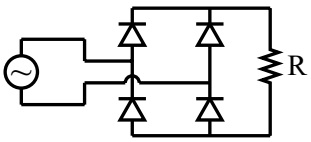
$$\Rightarrow \quad TUF = \frac{8}{\pi^2} \times \frac{R_L}{R_L + R_f} \tag{204a}$$

For ideal diode, $R_f = 0$

$$\therefore \quad TUF_{max} = \frac{8}{\pi^2} = 0.812 \quad \text{(for both centre tap \& bridge type)} \tag{205}$$

Example 20

In the single phase diode bridge rectifier shown in figure, the load resistor is R = 50 Ω. The source voltage is v = 200 sin ωt, where, ω = 2π × 50 radians per second. The power dissipated in the load resistor R is



(a) $\frac{3200}{\pi}$ W

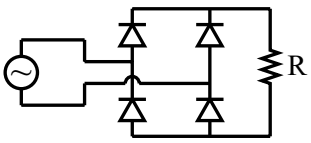
(b) $\frac{400}{\pi}$ W

(c) 400 W

(d) 800 W

GATE(EE/2002/2 M)

Solution : Ans.(c)



The power dissipated in load resistance depends on rms value of load current. The rms value of load current for full wave rectifier shown will be,

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{V_m}{\sqrt{2}\,R}$$

Given , source voltage, v = 200 sinωt

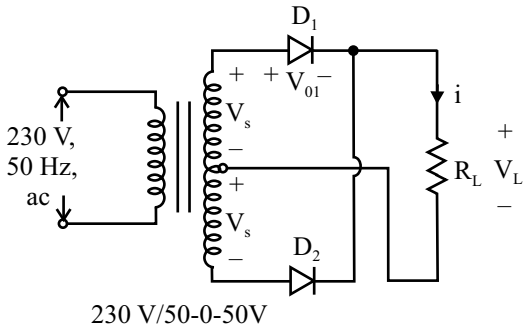
$$\therefore \quad I_{rms} = \frac{200}{\sqrt{2}\times 50} = 2\sqrt{2}$$

Power dissipated in R,

$$P = I^2R = \left(2\sqrt{2}\right)^2 \times 50 = 400W$$

Example 21

The circuit in figure shows a full-wave rectifier. The input voltage is 230 V (rms) single-phase ac. The peak reverse voltage across the diodes D_1 and D_2 is

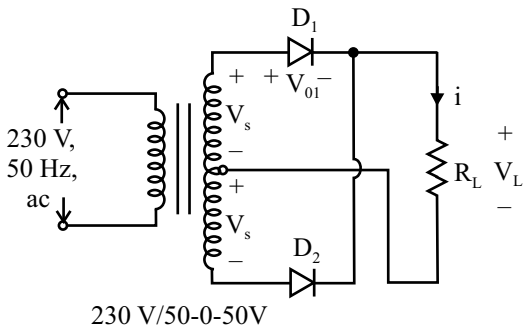


(a) $100\sqrt{2}V$ (b) 100 V

(c) $50\sqrt{2}\,V$ (d) 50 V

GATE(EE/2004/1 M)

Solution : Ans.(a)



Peak inverse voltage(PIV) of a centre tap full wave rectifier circuit shown above is given by,

$$PIV = 2V_m$$

Where, V_m is peak of secondary voltage of transformer. The rating of transformer is always given in terms of rms value. So, the peak voltage in each section of secondary winding of transformer is,

$$V_m = 50\sqrt{2}\,V$$

Then PIV of diode D1 and D2 will be,

$$PIV = 2V_m = 100\sqrt{2}V$$

Example 22

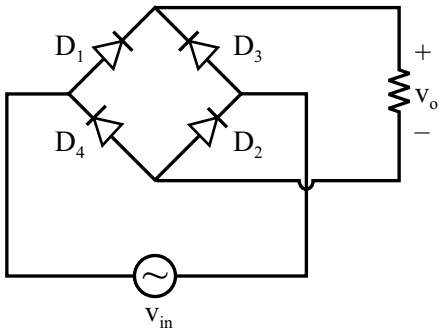
For an input, v (t) = 5 – 2 sin (100 πt) – cos (200πt), the output of a full-wave rectifier averager is

(a) 2 (b) 4

(c) 5 (d) 8

GATE(IN/2001/2M)

Solution : Ans.(c)



Given input of full wave rectifier,

$$v_{in}(t) = 5 - 2\sin(100\,\pi t) - \cos(200\pi t)$$

The dc component of $v_{in}(t)$ is more than peak value of ac components so the diodes D_1 and D_2 are continuously ON and output voltage is input signal itself.

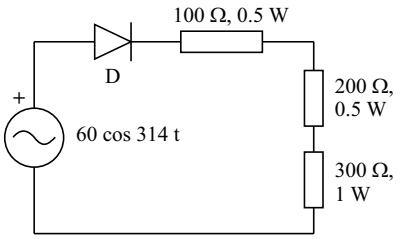
$$\therefore \quad v_o(t) = v_{in}(t) = 5 - 2\sin(100\,\pi t) - \cos(200\pi t)$$

The average value of ac components of output voltage is zero. Then the average output will be only dc component.

$$\therefore \quad V_{odc} = 5\ V$$

Example 23

For the circuit shown in figure, the diode D is ideal. The power dissipated by the 300 Ω resistor

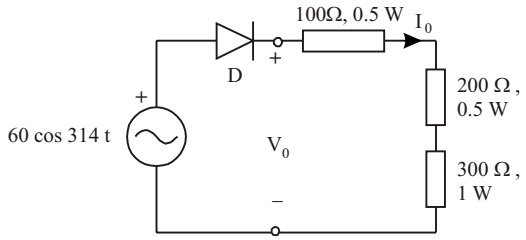


(a) 0.25 W (b) 0.50 W

(c) 0.75 W (d) 1.00 W

GATE(IN/2004/2M)

Solution : *Ans.(c)*



The given circuit is a half wave rectifier with rms output voltage of rectifier,

$$V_{o,rms} = \frac{V_m}{2} = \frac{60}{2} = 30V$$

Then rms value of current at output of rectifier,

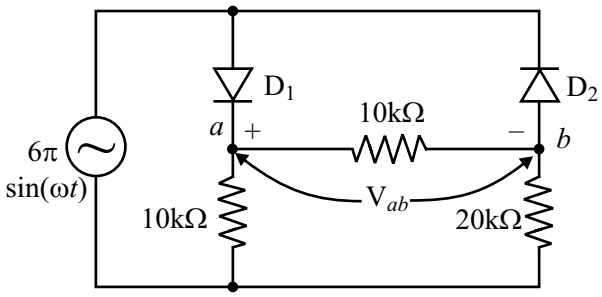
$$I_{o,rms} = \frac{V_{o,rms}}{R_{total}} = \frac{30}{100+200+300} = \frac{1}{20}$$

The power consumed by 300 Ω resistance,

$$P = I_{o,rms}^2 \times R = (0.05)^2 \times 300 = 0.75 \text{ W}$$

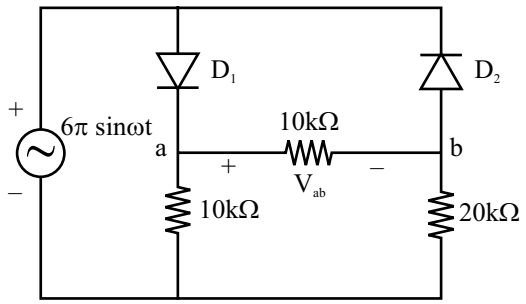
Example 24

In the circuit shown, assume that the diodes D_1 and D_2 are ideal. The average value of voltage V_{ab} (in Volts), across terminals '*a*' and '*b*' is .....



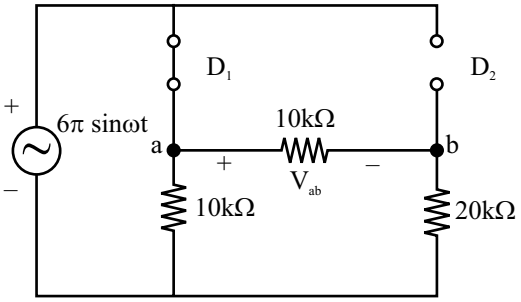
GATE(EC-III/2015/2M)

Solution : 4.85 to 5.15



Case-I : Positive half cycle of input voltage.

During positive half cycle of input voltage , the diode D_1 is ON and diode D_2 is OFF. The equivalent circuit for positive half cycle becomes as under

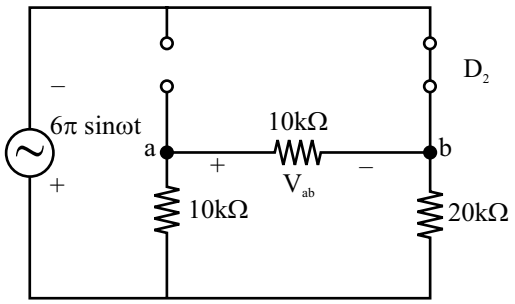


From above circuit,

$$V_{ab} = \frac{10}{10+20} \times 6\pi \sin \omega t = 2\pi \sin \omega t$$

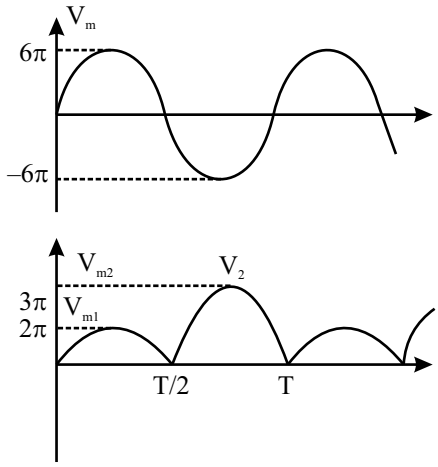
Case-II : Negative half cycle of input voltage. The diode D_1 is OFF and diode D_2 is ON during negative half cycle of input voltage.

The equivalent circuit during negative half cycle of input voltage is as under



$$V_{ab} = \frac{10}{10+10} \times 6\pi \sin \omega t = 3\pi \sin \omega t$$

The waveform of input voltage & V_{ab} can be drawn as under



It is observed from the waveforms that the output wave V_{ab} is sum of two half rectifier waves. So, the output voltage V_{ab} is sum of the two half rectified waves V_1 and V_2 as,

$$V_{av} = V_{av1} + V_{av2} = \frac{V_{m1}}{\pi} + \frac{V_{m2}}{\pi} = \frac{2\pi}{\pi} + \frac{3\pi}{\pi} = 5V$$

Example 25

In the Figures (a) and (b) shown below, the transformers are identical and ideal, except that the transformer in Figure (b) is centre-tapped. Assuming ideal diodes, the ratio of the root-mean-square (RMS) voltage across the resistor R in Figure (a) to that in Figure (b) is

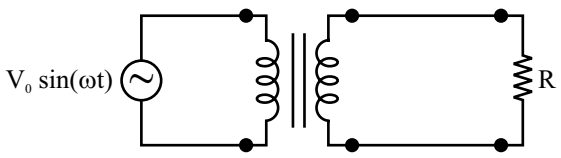


Fig.(a)

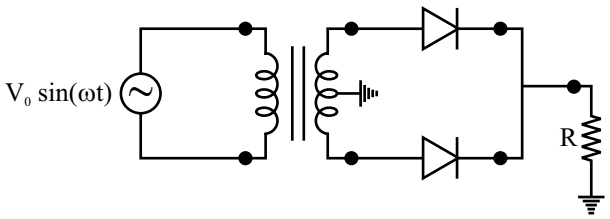


Fig.(b)

(a) $\sqrt{2}:1$

(b) 2:1

(c) $2\sqrt{2}:1$

(d) 4:1

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Solution : Ans.(b)

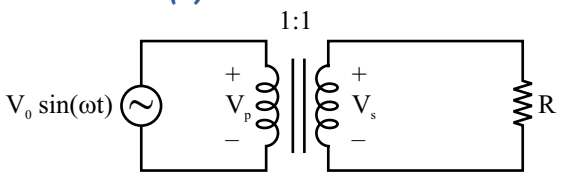


Fig.(a)

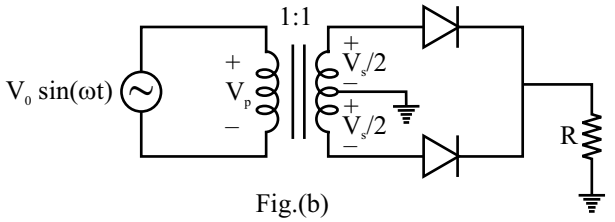


Fig.(b)

Let, transformation ratio of the transistor is 1 : 1.

The RMS value of voltage across 'R' in Fig.(a),

$$V_{RMS1} = \frac{V_o}{\sqrt{2}}$$

Circuit in Fig. 'b' is a centre-tap type full wave rectifier. The voltage across R in each half cycle is $\frac{V_s}{2}$.

$$\therefore \quad \frac{V_s}{2} = \frac{V_o}{2} \sin \omega t = V_m \sin \omega t$$

The RMS value of voltage across R is full wave rectifier is given by,

$$V_{RMS2} = \frac{V_m}{\sqrt{2}} = \frac{V_o}{2\sqrt{2}}$$

Ratio of RMS voltage across 'R' in Fig. 'a' to that of Fig.(b).

$$\frac{V_{RMS1}}{V_{RMS2}} = \frac{V_o/\sqrt{2}}{V_o/2\sqrt{2}} = \frac{2}{1}$$

1.6.4 Comparison of Centre tap and Bridge type rectifiers

(i) PIV of bridge type rectifier V_m where as it is $2V_m$ for centre tap type full wave rectifier.
(ii) Transformer Utilization factor (TUF) is better for bridge type rectifier as compare to centre tap type rectifier.
(iii) Size of transformer required for bridge type rectifier is smaller than centre tap or mid-point type rectifier.
(iv) Voltage regulation of centre tap type rectifier is better than bridge type rectifier.

1.6.5 Comparison between half wave and full wave bridge type rectifier

(i) Rectifier efficiency for full wave is double of that of half wave rectifier.
(ii) Full wave rectifier gives higher output voltage, higher power and higher TUF.
(iii) Ripple voltage of full wave rectifier is smaller than half wave rectifier.
(iv) Ripple frequency of full wave rectifier is twice the ripple frequency of half wave rectifier.
(v) In full wave rectifier the direction of current in secondary winding of transformer. Changes in every half cycle where as it is unidirectional in case of half wave rectifier. Due to unidirectional current in half wave rectifier there is problem of transformer core saturation. This problem is not present in full wave rectifier.
(vi) The voltage regulation of half wave rectifier is smaller than full wave bridge type rectifier. Therefore, voltage regulation of half wave rectifier is better than voltage regulation of full wave bridge type rectifier.

1.6.6 Rectifier Filters

The output from any of the rectifier circuit is not purely dc battery also has ac components called ripples along with it. Ripple content of output of full wave is less than half wave rectifier. A filter circuit converts pulsating

output of rectifier to a d.c. level. The commonly used filters are

i) Shunt capacitor filter
ii) Series inductor filter
iii) Choke input filter or L-section filter
iv) Capacitor input or π-filter
v) RC filter

1. Shunt Capacitor Filter

This filter is most simple has a capacitor load across output terminals of rectifier.

In shunt filter capacitor the diode current flows only for small duration when supply voltage is more than capacitor voltage. This current is short duration surging current. A small resistor called the surge limiting resistor is therefore always connected in series with the diode to limit this surge current.

A. Half wave rectifier with shunt capacitor filter

Half wave rectifier with shunt capacitor filter is shown in Fig. 88. The capacitor C is selected such that the time constant, RC, is much greater than the time period of the sinusoidal input signal.

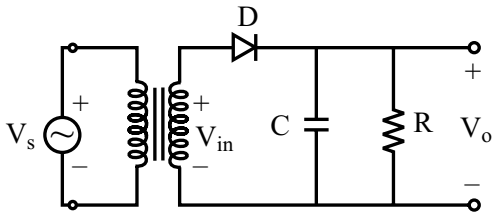


Fig.88 Half wave rectifier with shunt capacitor filter

The waveforms of input voltage and output voltage with and without shunt capacitor filter are shown in Fig. 89. It is observed that the output without capacitor filter is same as input during positive half cycle and zero during negative half cycle. When a capacitor of suitable value is connected in shunt with the load the output voltage is no more zero during negative half cycle.

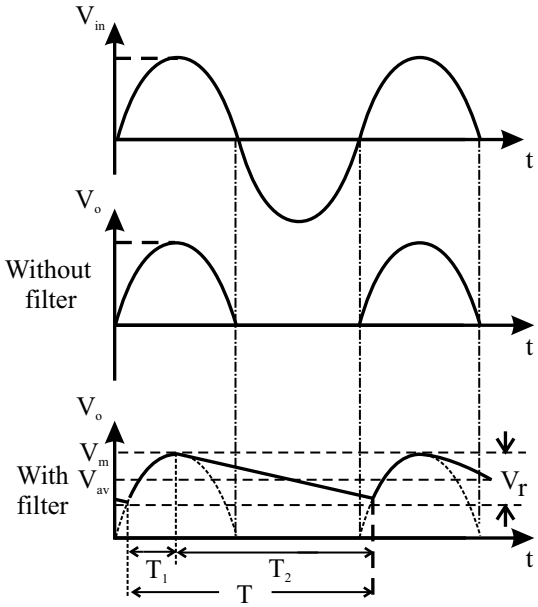


Fig.89 Waveforms of input voltage and output voltage of half wave rectifier with and without shunt filter

At steady state operation the diode is forward for period T_2 in positive half cycle and output voltage is same as input voltage. The capacitor gets charged to peak value,V_m, of input voltage during positive half cycle. After peak value, the input voltage falls below V_m where as capacitor is charged to V_m so the diode gets reverse biased and capacitor starts discharging through load resistance,R. The capacitor keeps on discharging for a period T_1 until the input voltage becomes more than the instantaneous value of capacitor voltage. The diode is again forward biased and capacitor is again charged to V_m. This cycle of charging and discharging of capacitor repeats in every cycle of input voltage and

the output voltage is, thus, non-zero during negative half cycle of input voltage and output voltage waveform is smoothened resulting in reduction in ripple in the output voltage.

Expression of Ripple Voltage :

The total charge taken by the capacitor during charging period is given by:

$$q_{T1} = CV_r \tag{206}$$

Where, V_r is the ripple voltage and T_1 is charging period

The charge removed during discharging period.

$$q_{T2} = I_{dc} T_2 \tag{207}$$

Where, I_{dc} is average capacitor current during discharging and T_2 is discharging period.

It is observed from the waveforms that output voltage is varying between two fixed levels. It will be possible only when the total charge stored by capacitor during charging period is equal to total charge removed during discharging period in steady state operation.

$$\therefore \quad q_{T1} = q_{T2}$$

$$\Rightarrow \quad CV_r = I_{dc} T_2$$

$$\Rightarrow \quad V_r = \frac{I_{dc}}{C} . T_2 \tag{208}$$

From waveform, $T_1 + T_2 = T$

If RC >> T then, $T_2 >> T_1$

$$\Rightarrow \quad T = T_1 + T_2 \approx T_2 \tag{209}$$

$$\Rightarrow \quad V_r = \frac{I_{dc}}{C} . T \tag{210}$$

$$\Rightarrow \quad \boxed{V_r = \frac{I_{dc}}{C f}} \tag{211}$$

Where f is frequency of input signal

Average output voltage of the rectifier with shunt filter can be given as,

$$V_{av} = V_m - \frac{V_r}{2} \tag{212}$$

$$\boxed{V_{av} = V_m - \frac{I_{dc}}{2 f C}} \tag{213}$$

The dc current through the capacitor during discharging period is given by,

$$\boxed{I_{dc} = \frac{I_m}{\pi}} \tag{214}$$

B. Full wave rectifier with shunt capacitor filter

Full wave rectifier with shunt capacitor filter is shown in Fig. 90. The capacitor C is selected such that the time constant,RC, is much greater than the time period of the input.

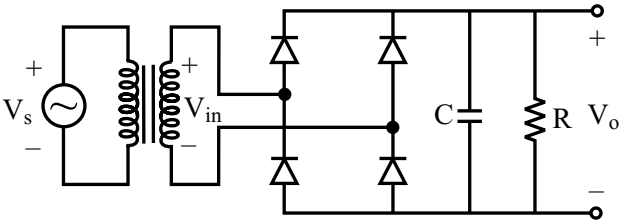


Fig. 90 Full wave rectifier with shunt capacitor filter

The waveforms of input voltage and output voltage with and without shunt capacitor filter are shown in Fig. 91. The output of full wave rectifier with a shunt capacitor filter is similar to that of half wave rectifier except that the output exists in full wave rectifier even during negative half cycle. In full wave rectifier the ripple frequency is 2f where as it is f in case half wave rectifier. The capacitor charges and discharges in every half cycle of input voltage.

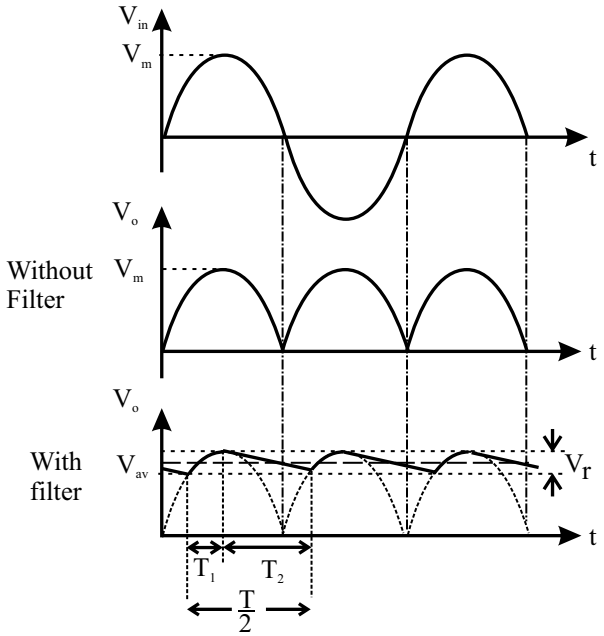


Fig.91 Waveforms of input voltage and output voltage of full wave rectifier with and without shunt filter

Expression of Ripple Voltage :

The total charge taken by the capacitor during charging period, T_1, is given by:

$$q_{T1} = CV_r \tag{215}$$

The charge removed during discharging period,

$$q_{T2} = I_{dc} T_2 \tag{216}$$

The total charge stored by capacitor during charging period is equal to total charge removed during discharging period in steady state operation.

$$\therefore \quad q_{T1} = q_{T2}$$

$$\Rightarrow \quad CV_r = I_{dc} T_2$$

$$\Rightarrow \quad V_r = \frac{I_{dc}}{C} . T_2 \tag{217}$$

From waveform, $T_1 + T_2 = T/2$

If RC >> T then, $T_2 >> T_1$

$$\Rightarrow \quad T/2 = T_1 + T_2 \approx T_2 \tag{218}$$

$$\Rightarrow \quad V_r = \frac{I_{dc}}{C} . \frac{T}{2} \tag{219}$$

$$\Rightarrow \quad \boxed{V_r = \frac{I_{dc}}{2Cf}} \tag{220}$$

Average output voltage with shunt filter can be given as,

$$V_{av} = V_m - \frac{V_r}{2} \tag{221}$$

$$\boxed{V_{av} = V_m - \frac{I_{dc}}{4fC}} \tag{222}$$

The dc current through the capacitor during discharging period is given by,

$$\boxed{I_{dc} = \frac{2I_m}{\pi}} \tag{223}$$

Note : *i. Ripple voltage in full wave rectifier is approximately half of ripple voltage of half wave rectifier.*

ii. The average output voltage of full wave rectifier is more than that of half wave rectifier.

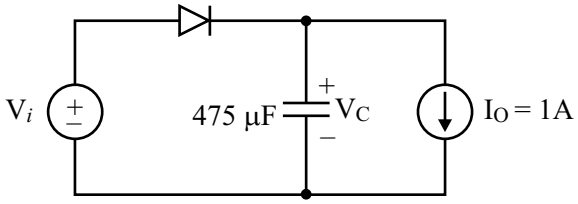
iii. Ripple frequency of half wave rectifier is same as frequency of input signal. Where as ripple frequency of full wave rectifier is twice the frequency of input signal.

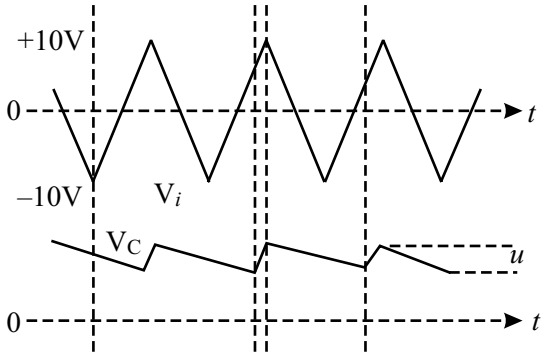
iv. The ripple factor of have wave rectifier with capacitor filter is given by, $RF = \frac{1}{2\sqrt{3}fRC}$

v. The ripple factor of full wave bridge rectifier with capacitor filter is given by, $RF = \frac{1}{4\sqrt{3}fRC}$

Example 26

The figure shows a half-wave rectifier with a 475 μF filter capacitor. The load draws a constant current I_0 = 1 A from the rectifier. The figure also shows the input voltage V_i, the output voltage V_C and the peak-to-peak voltage ripple *u* on V_C. The input voltage V_i is a triangle-wave with an amplitude of 10 V and a period of 1 ms.





The value of the ripple *u* (in volts) is .....

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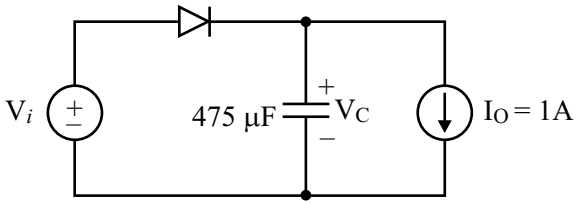
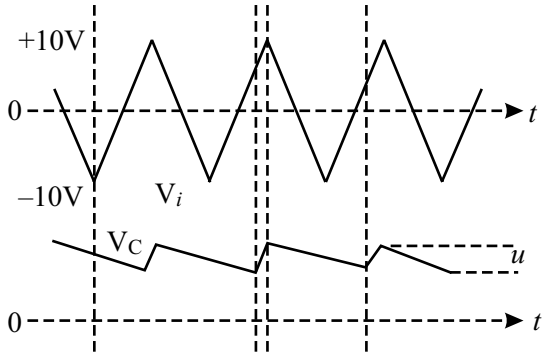
Solution : 1.9:2.2





The capacitor takes positive charge when diode is forward biased during positive half cycle of input voltage and capacitor discharges when diode is reverse biased. Let charging period is T_1 and discharging period is T_2. Charge taken by capacitor during charging period.

$$q_1 = Cu$$

Where u is ripple voltage.

The charge removed from capacitor during discharging period,

$$q_2 = I_o T_2$$

From the given wave forms,

$$T_2 = T - T_1 \approx T$$

$$\therefore \quad q_2 = I_o T$$

At steady state operation,

$$q_1 = q_2$$

$$\Rightarrow \quad Cu = I_o T$$

$$\Rightarrow \quad u = \frac{I_0 T}{C}$$

$$\Rightarrow \quad u = \frac{1 \times 1 \times 10^{-3}}{475 \times 10^{-6}} = 2.10 \text{ V}$$

2. Series Inductor Filter

In this filter a high value choke or inductor is connected in series with rectifier and load as shown in Fig. 92.

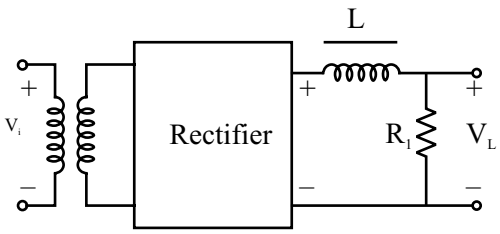


Fig.92 Rectifier with series inductor filter

The filter works on principle that inductor always opposes the change in energy stored in it. It should be noted that a decrease in the value of load resistance or an increase in the value of load current will decrease the amount of ripples in the circuit. Therefore, this filter is more efficient for small load resistance or high load currents. This filter is not used with half wave rectifier. The output voltage of series inductor filter is as shown in Fig. 93.

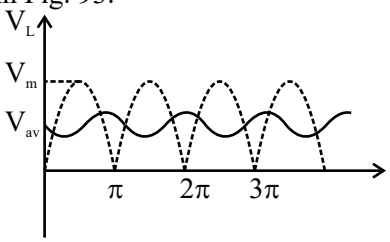


Fig.93 Output voltage of rectifier with series inductor filter

3. Choke Input or L-section or LC Filter

A simple series inductor filter reduces both the peak and effective value of output current and output voltage. On the other hand shunt capacitor filter reduces the ripple voltage but increases diode current. The diode may get damaged due to large current and at same time causes greater heating of supply transformer resulting in reduced efficiency.

In inductor filter ripple factor increases with the increase in load resistance R_L while in a capacitor filter it varies inversely with load resistance R_L. From economical point of view neither series inductor shunt capacitor are justifiable. Practical filters are derived by combining voltage stabilizing action of shunt capacitor with current smoothening action of series inductor as shown in Fig. 94. Such a filter is called L-section filter.

By using such combination ripple factor can be lowered, diode current can be restricted and ripple factor can be made independent of load resistance. Two such combination are used in L-section filter and π-filter.

The inductor passes dc and block ac component because of its small dc resistance than ac impedance. Any fluctuation still left is filtered out by shunt capacitor as it has large resistance to dc and small resistance to ac component. Ripples can be reduced effectively by making X_L greater than X_C at ripple frequency.

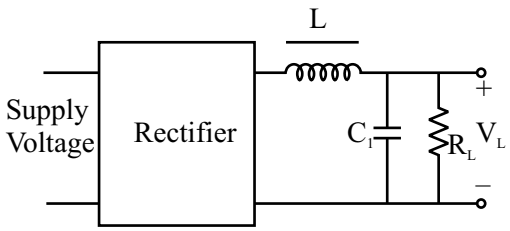


Fig.94 Rectifier with L-section filter

The LC filters are replaced by IC voltage regulators, active filters that reduce ripple and hold output dc voltage constant because their size and cost. This filter is not used for half wave rectifier.

4. Capacitor Input or π-Filter

The π-filter consists of shunt capacitor at the input side of L-section filter formed by inductor L and shunt capacitor C_2 as shown in Fig. 95. The rectifier directly feeds the capacitor input filter.

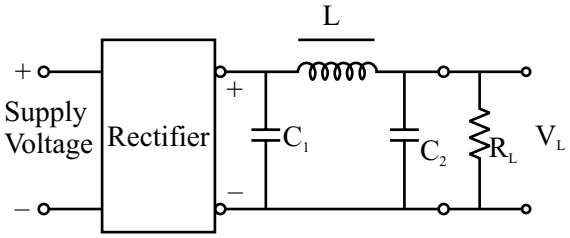


Fig.95 Rectifier with capacitor input or or π-filter

The π-filter are characterized by high output at low current drains. Such filter gives high output voltage and lower ripple than shunt capacitor and L-section filter.

The output voltage of π-filter falls off rapidly with increase in load current and, therefore, voltage regulation with this filter is very poor.

Comparison of L-section and π-filter :

i) In π-filter dc output voltage is more than L-section filter for same input.
ii) In π-filter ripples are less so clock required is smaller than L-section.
iii) RMS value of supply transformer is more in π-filter than L-section filter due charging current of input capacitor.
iv) Voltage regulation of π-filter is very poor so, π-filter are suitable for fixed loads where as L-section filter is suitable for variable load, provided a minimum current is maintained.
v) In π-filter PIV is large than L-section filter due to input capacitor.

The main drawback of π-filter is large size, more weight and higher external field developed by inductor.

Bleeder Resistance :

The operation of inductor filter is based on fact there must be same minimum current flowing through inductor all the times. To provide flow of this minimum current at all times through choke, a resister called bleeder resistor is place across filter output as shown in Fig.96.

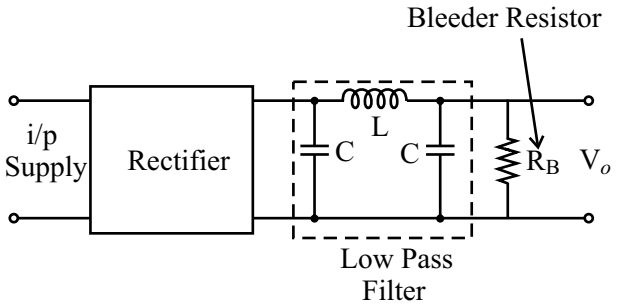


Fig.96 Capacitor input or or π-filter with Bleeder resistance

Bleeder resistor maintain same minimum current in choke even if load resistance is open circuited and improves filtering action. The value of bleeder resistor is designed to draw 10% of full load current. Bleeder resistance serves following purposes;

i) It improves voltage regulation as there is some initial drop in supply
ii) It provides safety to operator by providing discharging path to the capacitor. When power is switched off it provides path for discharging of capacitor. That is why it is called bleeder resistance.
iii) It may be used as potential divider to provide multi-level output voltage.
iv) It provides minimum current through choke even when load resistance disconnected therefore, it improves the filtering action.

Note : *Bleeder resistor should not draw more than 10% of the load current.*

5. RC Filter

The drawback of π-filter can be over come by replacing series inductor by series resistance, such circuit is called RC filter.

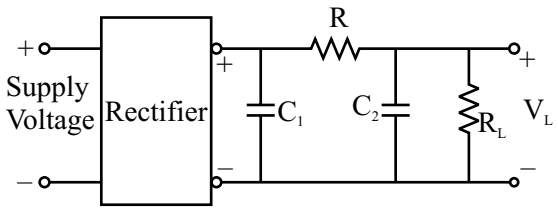


Fig.97 Rectifier with RC Filter

In RC filter ripples are dropped across series resistance R. The value of 'R' is about 10 times X_{C2}. The main drawback of this filter is that large drop across R gives poor voltage regulation. The load current flows through R so there need to be arrangement for dissipation of heat produced in 'R'. So RC filter is suitable for high load resistance only.

1.7 Zener Voltage Regulator

The breakdown voltage of a Zener diode is a fixed voltage. Therefore, a Zener diode can be used as a voltage regulator by connecting the diode in reverse biased mode across the load resistance as shown in Fig.98.

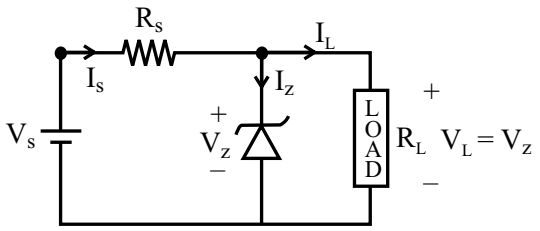


Fig. 98 Zener voltage regulator

The minimum current through a Zener diode is known as knee current. The knee current of Zener diode is determined by voltage regulation of the device and maximum current is limited by maximum current dissipation capability of the device. If $P_{D,max}$ is maximum power dissipation capability and V_z is Zener breakdown voltage of the diode then the maximum current carrying capability of the diode can be given as,

$$I_{z,max} = \frac{P_{D,max}}{V_Z} \tag{224}$$

Three design parameters of Zener voltage regulator are source voltage (V_s), source resistance (R_s) and load resistance (R_L). While designing these parameters of the circuit it should be ensured that minimum current should not fall below knee current and maximum current should not exceed limit determined by maximum power dissipation capability of the diode. Following three cases present the method to design load resistance, source resistance and source voltage by taking one parameter as variable and remaining two parameters as fixed for ease of understanding the design procedure.

Case-I : R_L is variable, V_s is constant and R_s is constant.

Supply current, $$I_s = \frac{V_s - V_z}{R_s} \tag{225}$$

If V_s and R_s are fixed then source current remains constant irrespective of load resistance.

Apply KCL, we have, $I_s = I_L + I_z$

$\Rightarrow$ $I_L = I_s - I_z$

Minimum load current, $I_{L\,min} = I_s - I_{z\,max}$

Maximum load current, $I_{L\,max} = I_s - I_{z\,min}$

Load current, $$I_L = \frac{V_L}{R_L} = \frac{V_z}{R_L} \tag{226}$$

Maximum load resistance,

$$R_{L\,max} = \frac{V_z}{I_{L\,min}} \tag{227}$$

Minimum load resistance,

$$R_{L\,min} = \frac{V_z}{I_{L\,max}} \tag{228}$$

Case-II : When R_s is variable, V_s is constant and R_L is constant

If R_L is fixed then load current remains constant irrespective of source resistance.

Load current, $$I_L = \frac{V_L}{R_L} = \frac{V_z}{R_L} \tag{229}$$

Minimum source current,

$$I_{s\,min} = I_L + I_{z\,min}$$

Maximum source current,

$$I_{s\,max} = I_L + I_{z\,max}$$

Maximum source resistance,

$$R_{s\,max} = \frac{V_s - V_z}{I_{s\,min}} \tag{230}$$

Minimum source resistance,

$$R_{s\,min} = \frac{V_s - V_z}{I_{s\,max}} \tag{231}$$

Case-III : When V_s is variable, R_s and R_L are constant.

If R_L is fixed then load current remains constant irrespective of source resistance.

The source voltage can be given as,

$$V_s = R_s I_s + V_z \tag{232}$$

Minimum source current,

$$I_{s\,min} = I_L + I_{z\,min}$$

Maximum source current,

$$I_{s\,max} = I_L + I_{z\,max}$$

Maximum source voltage,

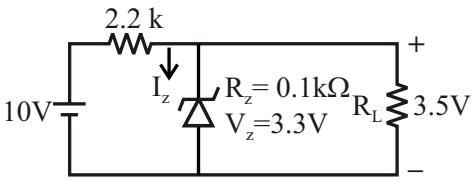
$$V_{s\,max} = R_s I_{s\,max} + V_z = R_s(I_L + I_{z\,max}) + V_z \tag{233}$$

Minimum source voltage,

$$V_{s\,min} = R_s(I_L + I_{z\,min}) + V_z \tag{234}$$

Example 27

The current through the Zener diode in figure is

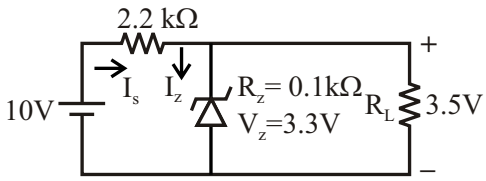


(a) 33 mA (b) 3.3 mA

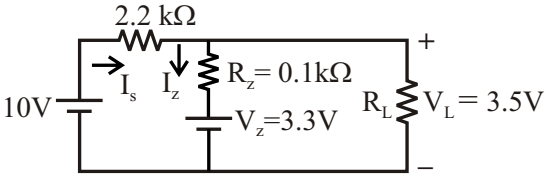
(c) 2 mA (d) 0 mA

GATE(EE/2004|1 M)

Solution : *Ans.(c)*



Replacing Zener diode by its dynamic equivalent circuit the given network can be drawn as under,



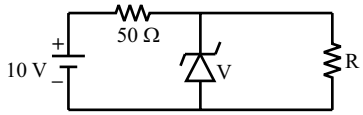
From the above circuit diagram,

$$V_L = I_z R_z + V_z$$

$$\Rightarrow \quad I_z = \frac{V_L - V_z}{R_z} = \frac{3.5 - 3.3}{0.1 \times 10^3} = 2 \text{ mA}$$

Example 28

The 6 V Zener diode shown in figure has zero Zener resistance and a knee current of 5 mA. The minimum value of R so that the voltage across it does not fall below 6 V is

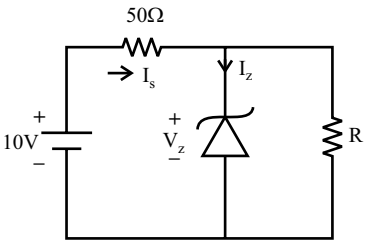


(a) 1.2 k ohms (b) 80 ohms

(c) 50 ohms (d) 60 ohms

GATE(EC/1992/2M)

Solution : *Ans.(b)*



Given, $I_{z,\,knee} = 5\text{mA}$

$V_z = 6\text{V}$

Source current,

$$I_s = \frac{10-6}{50} = \frac{4}{50} = 80\text{mA}$$

Maximum current through 'R',

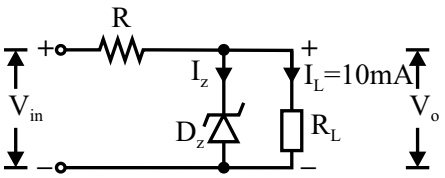
$$I_{max} = I_s - I_{zknee} = 80 - 5 = 75 \text{ mA}$$

Minimum value of R,

$$R_{min} = \frac{V_z}{I_{max}} = \frac{6}{75\times10^{-3}} = 80\ \Omega$$

Example 29

A Zener diode regulator in figure is to be designed to meet the specifications: I_L = 10 mA, V_0 = 10 V and V_{in} varies from 30 V to 50V. The Zener diode has V_z = 10V and I_{zk} (knee current) = 1 mA. For satisfactory operation.



(a) $R \le 1800\ \Omega$

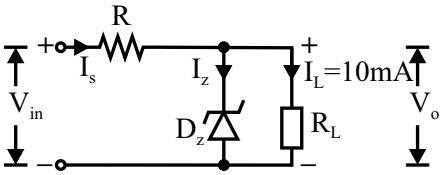
(b) $2000\ \Omega \le R \le 2200\ \Omega$

(c) $3700\ \Omega \le R \le 4000\ \Omega$

(d) $R > 4000\ \Omega$

GATE(EC/2002/2M)

Solution : Ans.(a)



Minimum diode current,

$$I_{zk} = 1 \text{ mA} = (I_z)_{min}$$

Load current, $I_L = 10$ mA

Minimum source current,

$$(I_S)_{min.} = (I_z)_{min.} + I_L$$

$$\Rightarrow \quad (I_S)_{min.} = (1 + 10) = 11 \text{ mA}$$

Source current, $I_s = \frac{V_{in} - V_z}{R}$

$$\Rightarrow \quad R = \frac{V_{in} - V_z}{I_s}$$

Maximum value of R, $R_{max} = \frac{V_{in} - V_z}{(I_s)_{min.}}$ .....(i)

Case-I: When, $V_{in} = 50$ V

$$R_{max} = \frac{50 - 10}{11} \times 10^3 = 3636.4\ \Omega$$

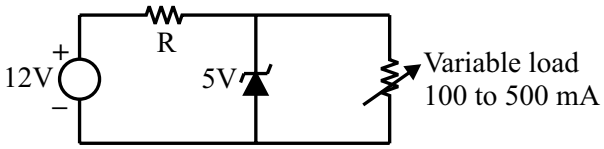
Case-II. When, $V_{in} = 30$ V,

$$R_{max} = \frac{30 - 10}{11} \times 10^3 = 1818.2\ \Omega$$

If R_{max} is selected to be 3636.4 Ω then current though Zener diode falls below knee current when V_{in} falls below 50V. Therefore, R = 3636.4 Ω circuit works satisfactorily only for V_{in} = 50V. Whereas if R_{max} is selected to be 1818 Ω then current through the Zener diode is always more than knee current for complete range of V_{in} from 30 V to 50 V. Hence the given circuit works satisfactorily if R ≤ 1800 Ω.

Example 30

In the voltage regulator shown in figure the load current can vary from 100 mA to 500 mA. Assuming that the Zener diode is ideal (i.e., the Zener knee current is negligibly small and Zener resistance is zero in the breakdown region), the value of R is

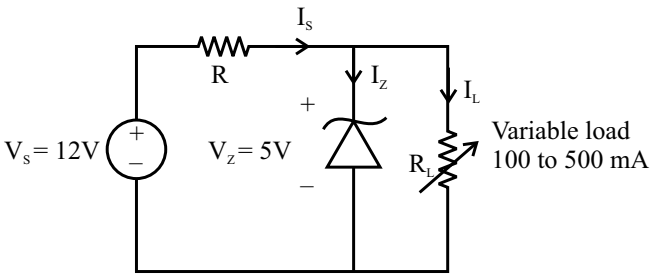


(a) 7 Ω (b) 70 Ω

(c) $\frac{70}{3}\Omega$ (d) 14 Ω

GATE(EC/2004/2M)

Solution : Ans.(d)



Current through zener diode,

$$I_Z = I_S - I_L$$

Source current, $I_S = I_Z + I_L = \frac{V_S - V_Z}{R} = \frac{12-5}{R} = \frac{7}{R}$

Load current, $I_L = \frac{7}{R} - I_Z$

Maximum load current, $I_{L,max} = \frac{7}{R} - I_{Z,knee}$

Minimum load current, $I_{L,min} = \frac{7}{R} - I_{Z,max}$

As maximum current through the Zener diode is not specified so minimum load current cannot be used to find R. The knee current of ideal Zener diode is zero.

$\therefore \quad I_{Z,knee} = 0$

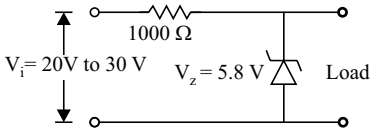
$\Rightarrow \quad I_{Lmax} = \frac{7}{R}$

$\Rightarrow \quad R = \frac{7}{I_{L\,max}} = \frac{7}{500 \times 10^{-3}} = 14\Omega$

So, the possible value of R is 14Ω.

Example 31

The Zener diode in the regulator circuit shown in figure has a Zener voltage of 5.8 Volts and a Zener knee current of 0.5 mA. The maximum load current drawn from this circuit ensuring proper functioning over the input voltage range between 20 and 30 Volts, is

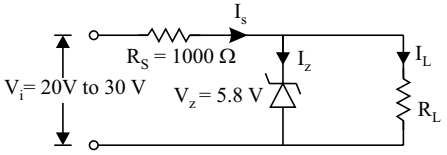


(a) 23.7 mA (b) 14.2 mA

(c) 13.7 mA (d) 24.2 mA

GATE(EC/2005/2M)

Solution : Ans.(a)



The maximum current pass through 1000 Ω resistance can be given by

$$I_{s,max} = \frac{30 - 5.8}{1000} = 24.2 \text{ mA}$$

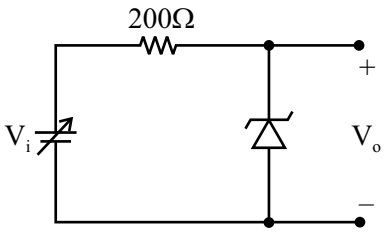
Zener knee current = 0.5 mA

The current through Zener diode should not fall below knee current for proper operation of circuit. So, the maximum load current limit will be,

$$I_{L,max} = I_{s,max} - I_{z,knee} = 24.2 - 0.5 = 23.7 \text{ mA}$$

Example 32

For the Zener diode shown in the figure, the Zener voltage at knee is 7 V, the knee current is negligible and the Zener dynamic resistance is 10 Ω. If the input voltage (V_i) range is from 10 to 16 V, the output voltage (V_o) ranges from

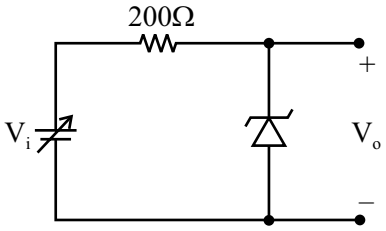


(a) 7.00 to 7.29 V (b) 7.14 to 7.29 V

(c) 7.14 to 7.43 V (d) 7.29 to 7.43 V

GATE(EC/2007/2M)

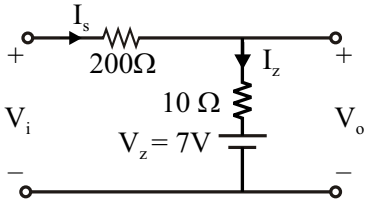
Solution : Ans.(c)



Given, $V_Z = 7$ V, $R_Z = 10\Omega$

$V_i = 10$ to 16 V

Replacing the Zener diode by its equivalent circuit, we have,



Current in zener diode, $I_z = \dfrac{V_i - 7}{200 + 10}$

Output voltage of circuit, $V_o = 10I_z + V_z = 10 \times \dfrac{V_i - 7}{200 + 10} + 7$

when, $V_i = 10\ V,$

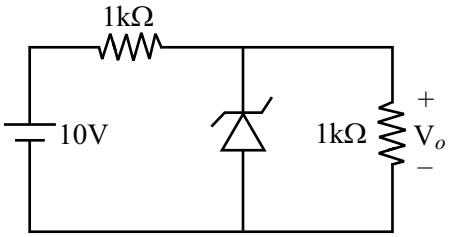
$$V_o = 10 \times \frac{10-7}{200+10} + 7 = 7.14\ V$$

when, $V_i = 16,$

$$V_o = 10 \times \frac{16-7}{200+10} + 7 = 7.43\ V$$

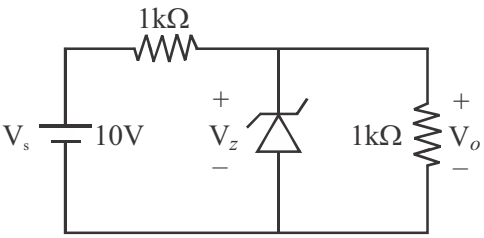
Example 33

In the circuit shown below, the Zener diode is ideal and the Zener voltage is 6V. The output voltage V_o (in volts) is .....

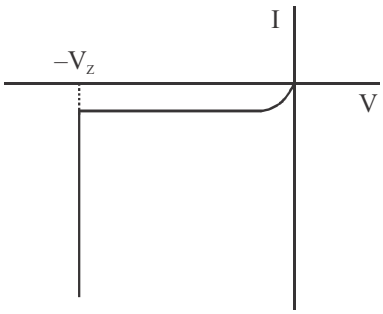


GATE(EC-I/2015/1M)

Solution : Ans. 5

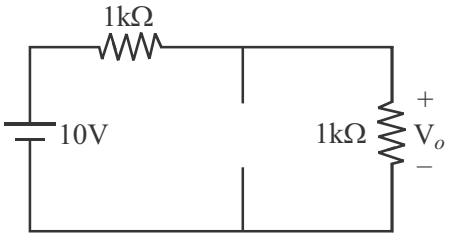


The VI Characteristics of Zener diode,



The voltage across the Zener diode is clipped at level V_Z if V_o tries to become more than V_Z.

Let us find the voltage V_o as function of input voltage when V_o is less than V_Z . When the output voltage is less than V_z the Zener diode is reverse biased and does not work in the break down region of VI characteristic. Under such condition the Zener diode behaves like and open circuit. So, the equivalent circuit become as under,



The output voltage of the circuit,

$$V_o = \frac{1k\Omega}{1k\Omega + 1k\Omega} \times 10 = 5\ V$$

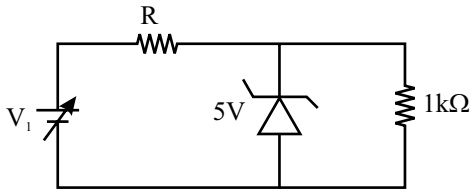
Given breakdown voltage of Zener diode,

$$V_Z = 6\ V$$

Since the voltage across the Zener diode in the given circuit is less than the breakdown voltage of the diode so the diode behaves like and open circuit and output voltage is 5 V.

Example 34

The circuit shown in the figure is used to provide regulated voltage (5 V) across the 1kΩ resistor. Assume that the Zener diode has a constant reverse breakdown voltage for a current range, starting from a minimum required Zener current, $I_{z\ min}$ = 2 mA to its maximum allowable current. The input voltage V_I may vary by 5% from its nominal value of 6 V. The resistance of the diode in the breakdown region is negligible.



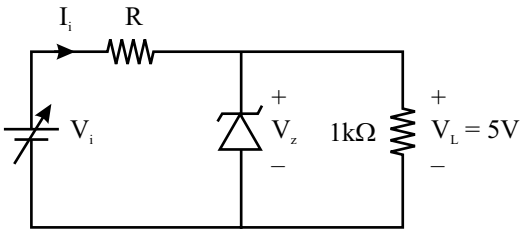
The value of R and the minimum required power dissipation rating of the diode, respectively, are

(a) 186 Ω and 10 mW (b) 100 Ω and 40 mW

(c) 100 Ω and 10 mW (d) 186 Ω and 40 mW

GATE(EC/2018/2M)

Solution : Ans.(b)



Given, $V_z = V_m + 5V$

Road resistance, $R_L = 1\ k\Omega$

Minimum current of Zener diode,

$$I_{z,\,min} = 2\ mA$$

Input voltage, $V_i = 6V + 5\%$

or $V_i = 5.7 \text{ to } 6.3\ V$

Load current, $I_L = \dfrac{V_L}{R_L} = \dfrac{5}{1000} = 5\,mA$

Minimum input current required for voltage regulation,

$$I_{i,\,min} = I_L + I_{z,\,min} = 5 + 2 = 7\ mA$$

Minimum current from supply can be related to R as under,

$$R = \frac{V_i - V_z}{I_{i,min}}$$

The maximum current through zero diode deter minimum power dissipation capability of diode and minimum value of resistance R is determined by minimum value of V_i & I_i.

$\therefore$ $$R_{min} = \frac{V_{i,min} - V_z}{I_{i,min}}$$

$$R_{min} = \frac{5.7 - 5}{7 \times 10^{-3}} = 100\Omega$$

Maximum supply current,

$$I_{i,\,max} = \frac{V_{i,max} - V_z}{R_{min}}$$

$$I_{i,\,max} = \frac{6.3 - 5}{100} = \frac{1.3}{100} = 13\,mA$$

Maximum current through Zener diode,

$$I_{z,\,max} = I_{i,\,max} - I_L = 13 - 5 = 8\ mA$$

Maximum power dissipated in the zener diode,

$$P_{z,\,max} = V_z\, I_{z,\,max} = 5 \times 8 = 40\ mW$$

The minimum power dissipation rating of the diode must be equation to the maximum power dissipation occurring in the diode.

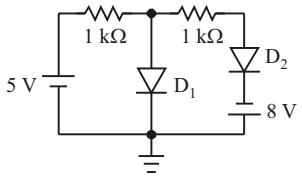
$$P_{D,\,min} = P_{z,\,max} = 40\ mW$$

1.8 Miscellaneous Diode Circuits

When diodes are connected in electrical circuits the very first step of analysis of network is to check whether the diode is ON or OFF. A diode is ON when voltage across the diode is more than cut in voltage of the diode and it is OFF when voltage across the diode is less than cut in voltage of the diode. The following examples present approach to analysis of the circuits consisting diodes as circuit elements.

Example 35

Assuming that the diodes are ideal in figure, the current in diode D_1 is

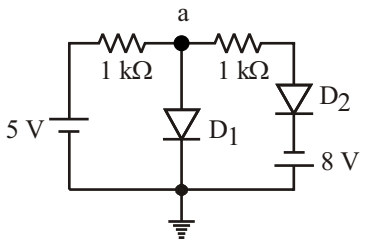


(a) 8 mA (b) 5 mA

(c) 0 mA (d) – 3 mA

GATE(EE/2004|2 M)

Solution : Ans.(c)



Since anode of diode D_2 is applied a negative potential at cathode and positive potential at anode so, it is forward biased and it behaves like as short circuit. Then the potential at node 'a' with D_1 open circuited will be,

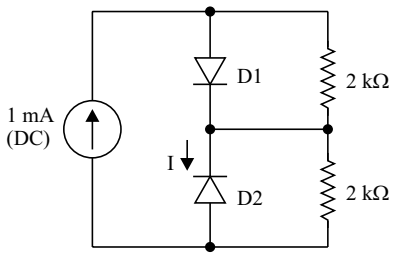
$$\frac{5-V_a}{1\times10^3} = \frac{V_a-(-8)}{1\times10^3}$$

$$V_a = -1.5\ V$$

Since V_a is negative , so, diode D_1 will be reverse biased and will behave like an open circuit. When Diode D_1 is open circuited the current through D_1 is zero.

Example 36

Assume that D1 and D2 in figure. are ideal diodes. The value of current I is

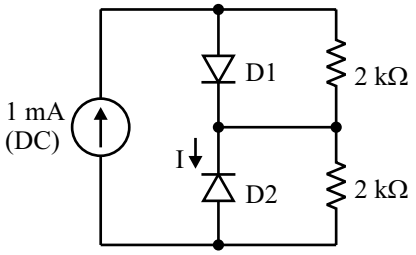


(a) 0 mA (b) 0.5 mA

(c) 1 mA (d) 2 mA

GATE(EE/2005|1 M)

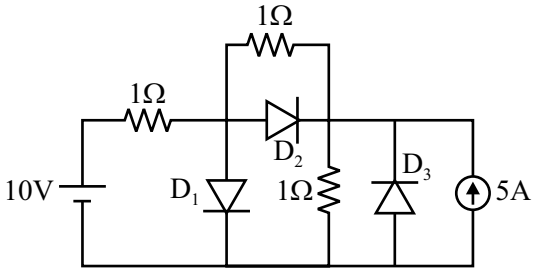
Solution : Ans. (a)



In the circuit shown above the diode D1 is forward biased and Diode D2 is reverse biased. So, current through D1 is 1mA and current through D2 is 0 mA.

Example 37

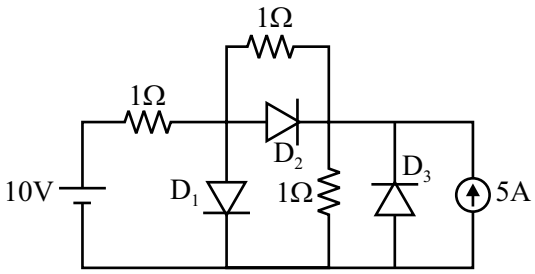
What are the states of the three ideal diodes of the circuit shown in figure ?



(a) D_1ON, D_2OFF, D_3OFF
(b) D_1OFF, D_2ON, D_3OFF
(c) D_1ON, D_2OFF, D_3ON
(d) D_1OFF, D_2ON, D_3ON

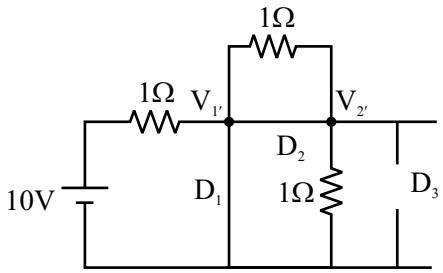
GATE(EE/2006 | 1 M)

Solution : Ans.(a)

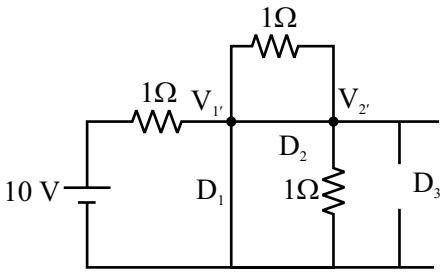


Case-I : With voltage source alone:

Taking voltage source only we have,



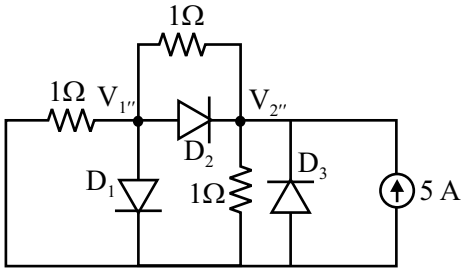
With voltage source alone the diode D_1 is forward biased , diode D_2 is forward biased and D_3 is reverse biased and equivalent circuit becomes as shown below,



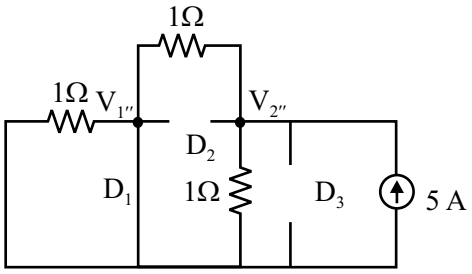
Voltages, $V_{1'} = V_{2'} = 0$ V

Case - II : Current source alone:

Taking current source only the circuit becomes,



With current source alone the Diode D_1 is forward biased , D_2 is reverse biased and diode D_3 is reverse biased. So, the equivalent circuit becomes,



Voltages, $V_{1''} = 0$, $V_{2''} = 2.5$ V

Conclusion:

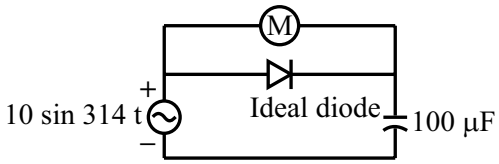
I. Diode D_1 is forward biased in both the cases so, D_1 will be ON when both sources are applied together.

II. Diode D_3 is reverse biased in both the cases so D_3 will be reverse biased when both sources are applied together.

III. Potential at node '1' with voltage source alone is 0 V and potential at node '2' with current source alone is 2.5 V . So,the diode D_2 is reverse biased when both source are applied together.

Example 38

In figure ideal moving iron voltmeter M will read

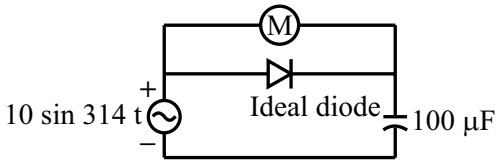


(a) 7.07 V (b) 12.24 V

(c) 14.14 V (c) 20.0 V

GATE(EC/1993/1M)

Solution : Ans.(b)



During first positive half cycle the diode gets forward biased and capacitor gets charged to peak of input voltage. Then onward the capacitor retains its voltage. Then the voltage across the diode becomes,

$$v_D = v_{in} - V_m = 10 \sin 314t - 10 \text{ ;}$$

where, $V_m = 10$ V = peak of input voltage

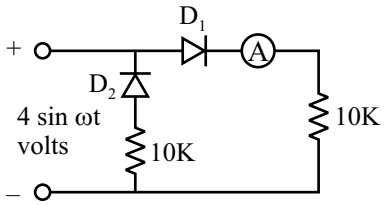
The moving iron voltmeter measures the rms value of voltage. So, the voltmeter connected across the diode measures the rms voltage across the diode.

$$V_{D,rms} = \sqrt{(10)^2 + \left(\frac{10}{\sqrt{2}}\right)^2}$$

$$V_{D,rms} = 12.24 \text{ V}$$

Example 39

In the circuit of the given figure, assume that the diodes are ideal and the meter is an average indicating ammeter. The ammeter will read

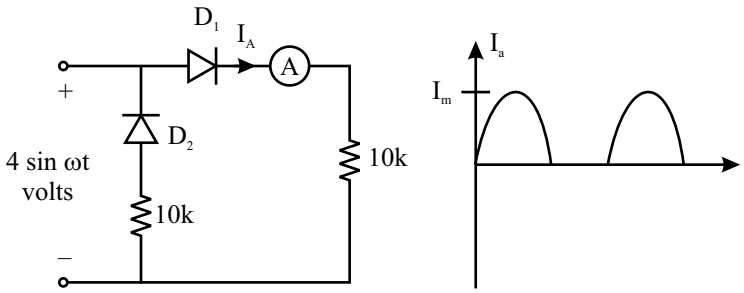


(a) $0.4\sqrt{2}$A (b) 0.4 A

(c) $\frac{0.8}{\pi}$A (d) $\frac{0.4}{\pi}$mA

GATE(EC/1996/1M)

Solution : Ans.(d)



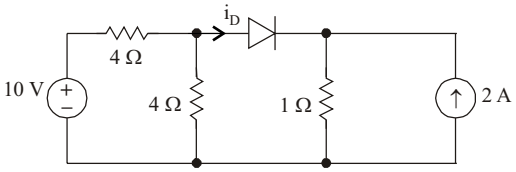
During positive half cycle D_1 is ON and D_2 is OFF and during negative half cycle D_1 is OFF and D_2 is ON. So, current through ammeter flows during positive half cycle only. As meter is average indicating type so it reads average value of current through it. The average value of current through meter can be given as,

$$I_{av} = \frac{V_m}{\pi} \times \frac{1}{10} = \frac{4}{10\pi} \text{mA}$$

$$\Rightarrow \quad \boxed{I_{av} = \frac{0.4}{\pi} \text{mA}}$$

Example 40

In the circuit of figure the current i_D through the ideal diode (zero cut-in voltage and forward resistance) equals



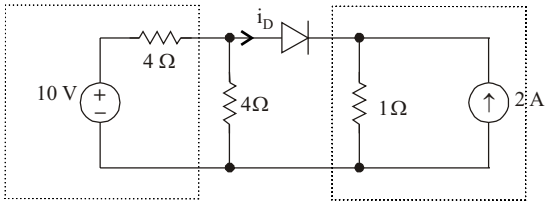
(a) 0 A (b) 4A

(c) 1A (d) None of the above

GATE(EC/1997/1M)

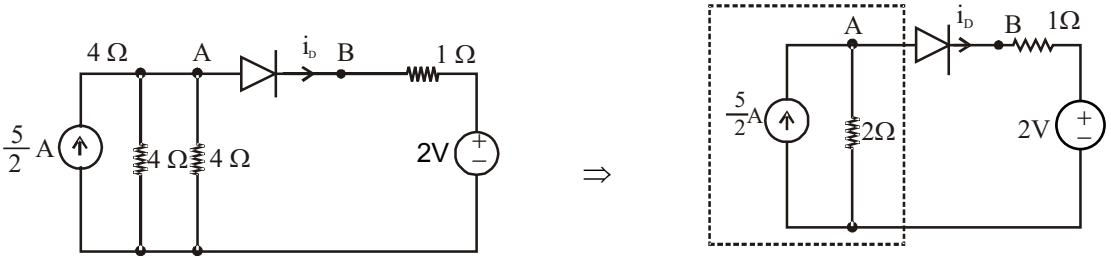
Solution : Ans.(c)

The given network is

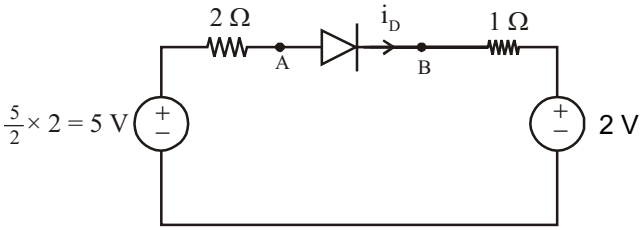


We want to calculate current i_D flowing from A to B.

Now converting the voltage source into current source and RHS current source into voltage source. The equivalent circuit becomes.



On converting left side current source into voltage source the equivalent circuit again becomes as under,



As it is clear now that the diode will be forward biased.

Applying KVL in the circuit,

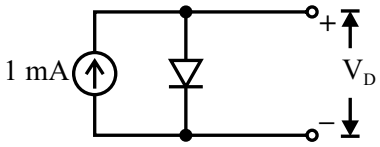
$$5 - 2\,i_D - i_D - 2 = 0$$

$$\Rightarrow \quad 3i_D = 3$$

$$\Rightarrow \quad i_D = 1A$$

Example 41

In figure a silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20°C, V_D is found to be 700 mV. If the temperature rises to 40°C, V_D becomes approximately equal to



(a) 740 mV (b) 660 mV

(c) 680 mV (d) 700 mV

GATE(EC/2002/1M)

Solution : Ans.(c)

The diode current equation is given by

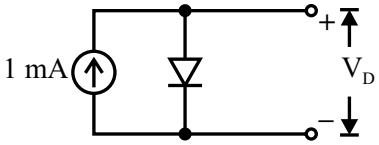
$$I = I_o\left[e^{\frac{V_D}{\eta V_T}} - 1\right]$$

Where, V_D = voltage across the diode

V_T = Thermal voltage = $\dfrac{T}{11600}$

η = 1 for Ge

= 2 for Si



For the given circuit shown above,

$I = 1$ mA

Case-I : $T_1 = 20\ ^oC$ or 293 K

Thermal voltage,

$$V_{T_1} = \frac{T_1}{11600} = \frac{293}{11600} = 0.0253\,Volts$$

The diode current,

$$I_1 = 1\times10^{-3} = I_{o1}\left[e^{\frac{0.7}{2\times0.0253}} - 1\right]$$

$$\Rightarrow \quad 1\times10^{-3} = I_{o1}\left[e^{13.83} - 1\right]$$

$$\Rightarrow \quad I_{o1} = 9.85 \times 10^{-10}\,A$$

Case-II : $T_2 = 40\ ^oC$ or 313 K

The reverse saturation current as a function of temperature is given by,

$$I_{o2} = I_{o1} \times 2^{\left[\frac{T_2 - T_1}{10}\right]}$$

$$\Rightarrow \quad I_{o2} = I_{o1} \times 2^{(40-20)/10}$$

$$\Rightarrow \quad I_{o2} = I_{o1} \times 2^2 = 4I_{o1}$$

$$\Rightarrow \quad I_{o2} = 4\times9.85 \times 10^{-10} = 3.94 \times10^{-9}\,A$$

Thermal voltage,

$$V_{T_2} = \frac{T_2}{11600} = \frac{313}{11600} = 0.02698 \text{ Volts}$$

Since the diode is connected to a current source therefore, the diode current,

$$I_2 = I_1 = 1 \text{ mA}$$

$$I_2 = 1\times10^{-3} = I_{o2}\left[e^{\frac{V_{D2}}{2\times0.02698}} - 1\right]$$

$$\Rightarrow \quad 10^{-3} = 3.94 \times 10^{-9}\left[e^{\frac{V_{D_2}}{0.05396}} - 1\right]$$

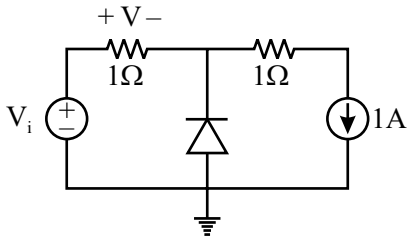
$$\Rightarrow \quad 12.44 = \frac{V_{D_2}}{0.05396}$$

$$\Rightarrow \quad V_{D_2} = 0.6712 = 671.2 \text{ mV}$$

The closest value is 680 mV

Example 42

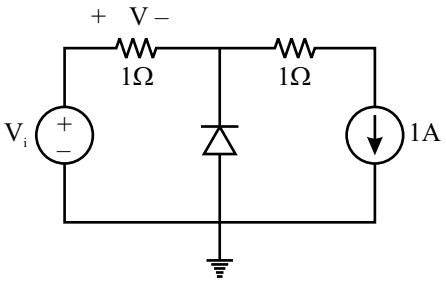
In the circuit below, the diode is ideal. The voltage V is given by



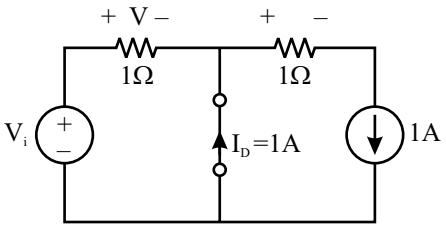
(a) min (V_i , 1)
(b) max (V_i , 1)
(c) min ($-V_i$, 1)
(d) max ($-V_i$, 1)

GATE(EC/2009/2M)

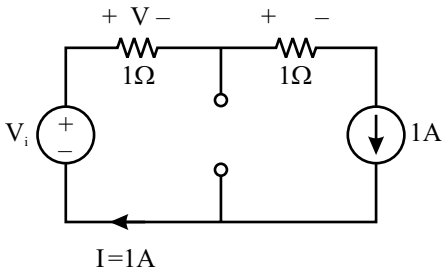
Solution : Ans.(a)



When Diode is ON given circuit becomes as under,



When Diode is OFF the circuit becomes as under,

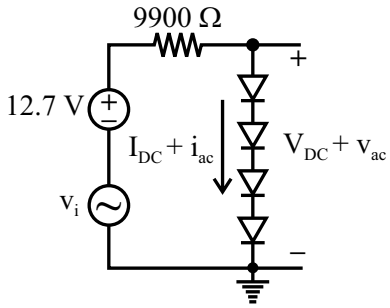


When $V_i > 1V$ Diode is OFF and V = 1 V and when $V_i < 1$ V Diode is ON and $V = V_i$. So, voltage V is minimum of V_i and 1 V.

Example 43

Statement for Linked Answer Questions 43 (i) and 43(ii) :

In the circuit shown below, assume that the voltage drop across a forward biased diode is 0.7 V. The thermal voltage $V_T = kT/q = 25$ mV. The small signal input $v_i = V_p \cos(\omega t)$ where $V_p = 100$ mV.



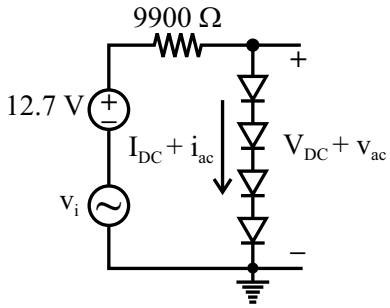
(i) The bias current I_{DC} through the diodes is

(a) 1 mA (b) 1.28mA

(c) 1.5 mA (d) 2 mA

GATE(EC/2011/2M)

Solution : Ans.(a)



DC bias current through diodes,

$$I_{DC} = \frac{12.7 - 4 \times 0.7}{9900}$$

$\Rightarrow \quad I_{DC} = 1\ mA$

(ii) The ac output voltage v_{ac} is

(a) $0.25\cos(\omega t)$ mV (b) $1\cos(\omega t)$ mV

(c) $2\cos(\omega t)$ mV (d) $22\cos(\omega t)$ mV

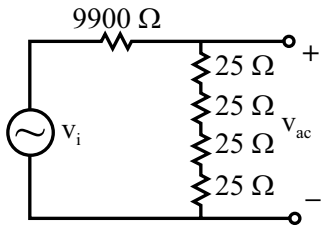
GATE(EC/2011/2M)

Solution : Ans.(b)

AC equivalent resistance of diode,

$$r = \frac{V_T}{I_D} = \frac{25}{1} = 25\Omega$$

AC equivalent circuit becomes as shown below,



AC output voltage,

$$v_{ac} = \frac{100}{9900+100} \times v_i$$

Given, $v_i = 100\cos \omega t$ mV

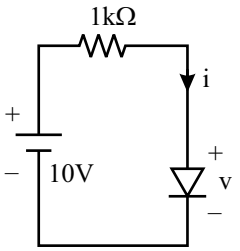
$\Rightarrow \quad v_{ac} = \frac{100}{10000} \times 100 \cos \omega t$ mV

$\Rightarrow \quad v_{ac} = 1\cos \omega t$ mV

Example 44

The i-v characteristics of the diode in the circuit given below are

$$i = \begin{cases} \frac{v-0.7}{500} A, & v \geq 0.7V \\ 0\,A, & v < 0.7V \end{cases}$$



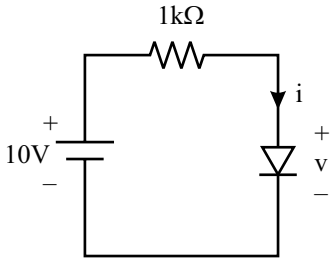
The current in the circuit is

(a) 10 mA (b) 9.3 mA

(c) 6.67 mA (d) 6.2 mA

GATE(EC/EE/IN/2012/1M)

Solution : Ans.(d)



Characteristics of diode

$$i = \frac{v-0.7}{500}A \quad ; v \geq 0.7V$$

$$= 0\ A \quad ; v < 0.7\ V$$

From given circuit, $v = 10 - 10^3 \times i$

$$\Rightarrow \quad v = 10 - 10^3 \times \frac{v-0.7}{500}$$

$$\Rightarrow \quad v = 10 - 2v + 1.4$$

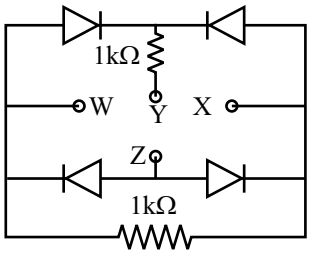
$$\Rightarrow \quad 3v = 11.4$$

$$\Rightarrow \quad v = \frac{11.4}{3} = 3.8V$$

$$\therefore \quad i = \frac{3.8-0.7}{500} = 6.2mA$$

Example 45

A voltage 1000 sin ωt Volts is applied across YZ. Assuming ideal diodes, the voltage measured across WX in Volts, is



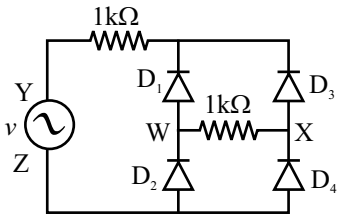
(a) sin ωt (b) (sin ωt + |sin ωt)| / 2

(c) (sin ωt – |sin ωt)| / 2 (d) 0 for all t

GATE(EC/IN/EE/2013/2M)

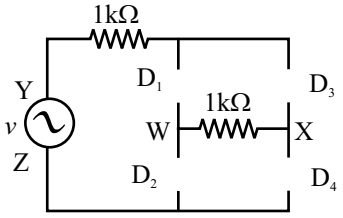
Solution : Ans.(d)

Above circuit can also be redrawn as shown under,

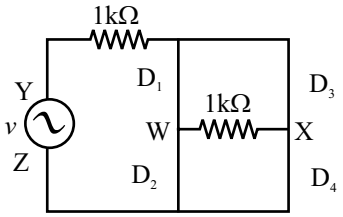


Given, v = 1000 sin ωt

When terminal Y is positive w.r.t. terminal 'Z' all the diodes are reverse biased and behave like open circuit. Then the resistance across WX is open circuited from both terminals as shown below. So, V_{WX} is zero for positive half cycle voltage V_{YZ}.



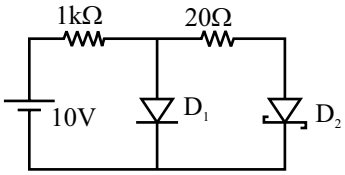
When terminal Y is negative w.r.t. Z all the diodes are forward biased and resistance across WX is short circuited as shown below. If resistance short circuited the voltage V_{WX} again becomes zero for negative half also.



Thus voltage across WX is zero all the times.

Example 46

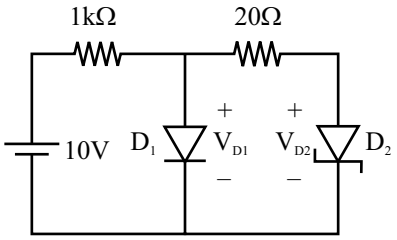
In the figure, assume that the forward voltage drops of the PN diode D_1 and Schottky diode D_2 are 0.7 V and 0.3 V, respectively. If ON denotes conducting state of the diode and OFF denotes nonconducting state of the diode, then in the circuit,



(a) both D_1 and D_2 are ON
(b) D_1 is ON and D_2 is OFF
(c) both D_1 and D_2 are OFF
(d) D_1 is OFF and D_2 is ON

GATE(EC-I/2014/1M)

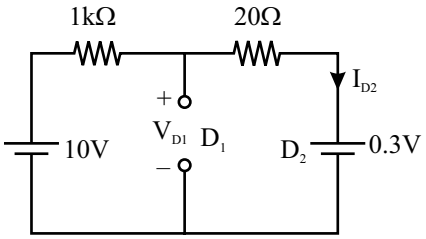
Solution : Ans.(d)



Given $V_{D1} = 0.7V$

and $V_{D2} = 0.3\ V$

The Schottky diode D_2 has lower forward voltage drop. Its cut in voltage is also small. The diode D_2 having small is cut in voltage is turned ON first. The moment diode D_2 is turned ON, the equivalent circuit becomes as under,



The current in diode D_2 , $I_{D2} = \dfrac{10-0.3}{1000+20} = 0.686\,mA$

Once diode D_2 is turned 'ON' , the voltage across diode D_1 can be given as under,

$$V_{D1} = 20\ I_{D2} + 0.3$$

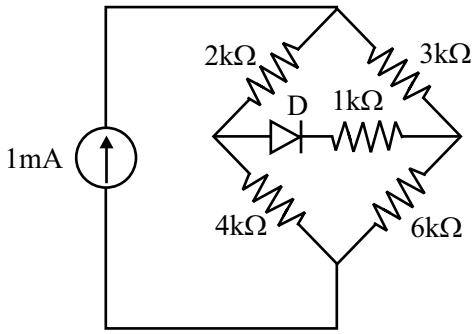
$$\Rightarrow \quad V_{D1} = 20 \times 0.686 \times 10^{-3} + 0.3$$

$$\Rightarrow \quad V_{D1} = 0.313\ V$$

Since voltage across diode D_1 is less than its forward voltage so diode D_1 will remain OFF once diode D_2 is turned ON.

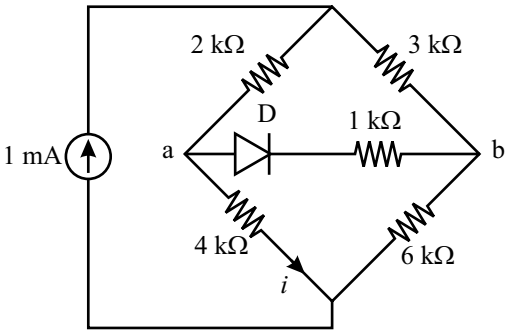
Example 47

The diode in the circuit given below has $V_{ON} = 0.7$ V but is ideal otherwise. The current (in mA) in the 4 kΩ resistor is .....



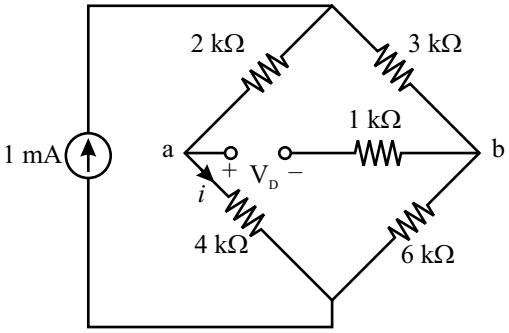
GATE(EC-II/2015/2M)

Solution : Ans.: 0.59 to 0.61



Before finding out the current in 4kΩ resistor, we need to check whether the diode 'D' is forward biased or reverse biased. If it is forward biased with $V_D > 0.7V$ than it should be replaced by a battery of 0.7 V to indicate a voltage drop and if it is reverse biased with $V_D < 0.7V$ then it should be replaced by an open circuit.

Whether diode is ON or OFF can be checked by opening the terminals of diode and then checking voltage across terminals of the diode. The equivalent circuit with diode replaced by open circuit becomes as under,



Voltage at node 'a', $V_a = \frac{6+3}{6+3+4+2} \times 1 \times 4 = \frac{12}{5} = 2.4V$

Voltage at node 'b', $V_b = \frac{4+2}{6+3+4+2} \times 1 \times 6 = \frac{36}{15} = 2.4V$

Voltage across diode, $V_D = V_a - V_b = 2.4 - 2.4 = 0V$

Since $V_D < 0.7V$ so the diode is OFF and behaves like as open circuit.

Then current through 4kΩ resistor will be,

$$i = \frac{3+6}{3+6+4+2} \times 1mA = 0.60\ mA$$

Example 48

The I-V characteristics of the Zener diodes D_1 and D_2 are shown in Figure I. These diodes are used in the circuit given in Figure II. If the supply voltage is varied from 0 to 100 V, then breakdown occurs in

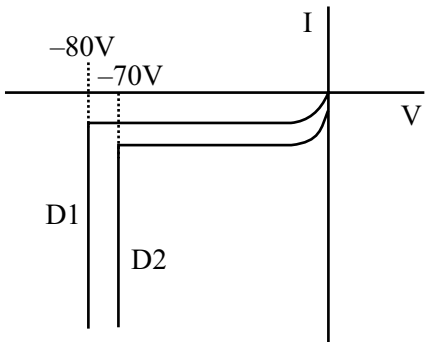


Figure I

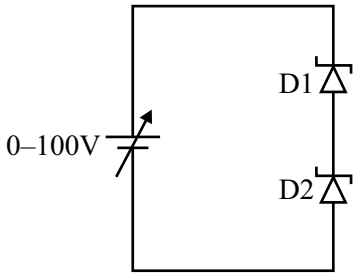


Figure II

(a) D_1 only

(b) D_2 only

(c) both D_1 and D_2

(d) none of D_1 and D_2

GATE(EC-III/2016/2M)

Solution : Ans. (*)

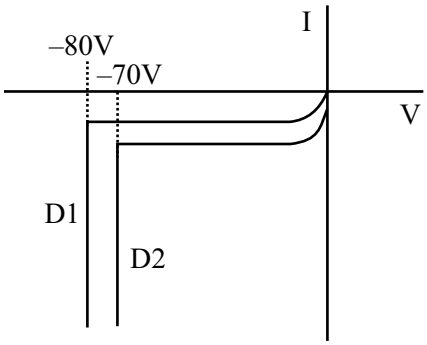


Figure I

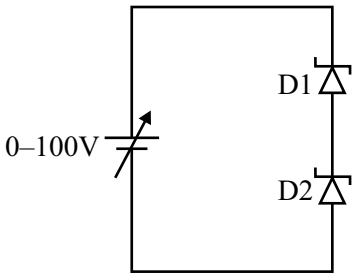


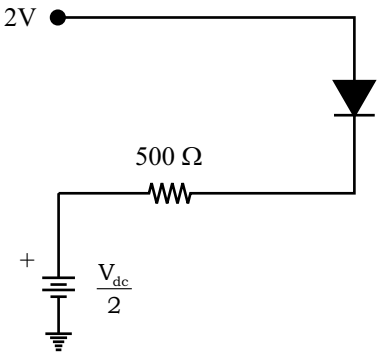
Figure II

From figure I the breakdown voltage of the diode D1 is 80 V and breakdown voltage of diode D2 is 70 V. Since diodes are connected in series therefore, the breakdown of diodes will occur only if supply voltage is more than the sum of breakdown voltage of both diodes i.e. 80 +70 (=150V). Here maximum supply voltage is 100 V so none of diode operates in breakdown region. Both diodes in the circuit will be in reverse mode and will behave like open circuit.

***Note** : As per answer key of GATE exam the answer is option (a) which is incorrect.*

Example 49

The silicon diode, shown in the figure, has a barrier potential of 0.7 V. There will be no forward current flowing through the diode, if V_{dc}, in volt, is greater than

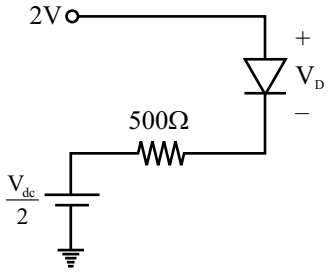


(a) 0.7 (b) 1.3

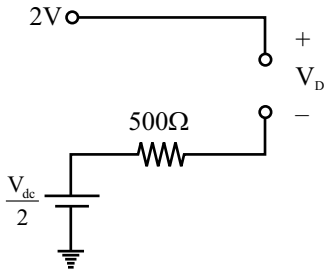
(c) 1.8 (d) 2.6

GATE(IN/2017/1M)

Solution : Ans. (d)



These is no forward current in the diode voltage across the diode, $V_D < 0.7$ V. The voltage V_D across diode should be checked by opening the terminals of the diode as under.



$$V_D = 2 - \frac{V_{dc}}{2}$$

Diode behaves as open circuit if

$$V_D < 0.7\ V$$

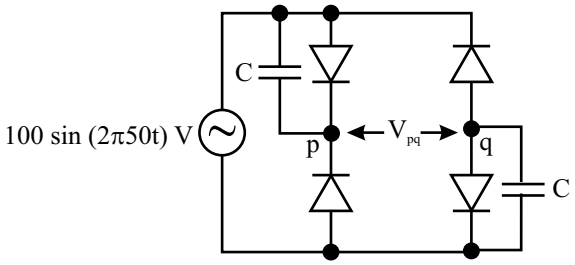
$$\therefore \quad 2 - \frac{V_{dc}}{2} < 0.7V$$

$$\Rightarrow \quad \frac{V_{dc}}{2} > 2 - 0.7$$

$$\Rightarrow \quad V_{dc} > 2.6V$$

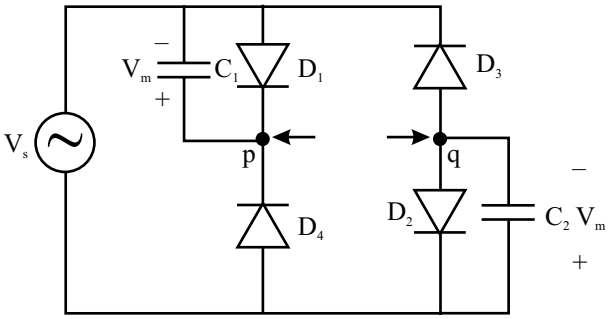
Example 50

The diodes given in the circuit are ideal. At t = 60 ms, V_{pq} (in Volts) is _____.



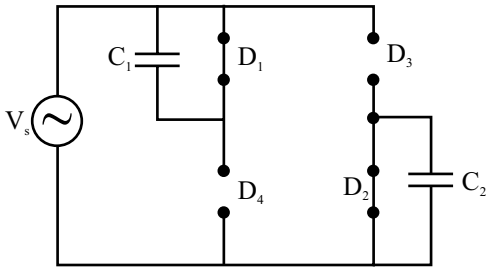
GATE(IN/2018/1M)

Solution : Ans.: 200

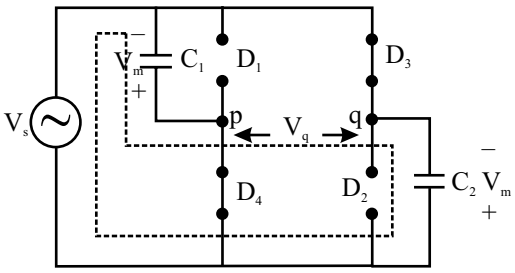


Given $V_s = 100 \sin 2\pi\ 50t$

During positive half cycle of input supply the diodes D_1 and D_2 are forward biased and D_3 & D_4 are reverse biased. The circuit is not complete and capacitors remain uncharged.



During nagative half cycle the diodes D_3 & D_4 one forward biased and diodes D_1 & D_2 are reversed biased. The capacitor C_1 gets charged to peak of input voltage through diode D_4 and capacitor C_2 gets charged to peak of input voltage through diode D_3. The equivalent circuit for negative half cycle becomes as under.



Time period of input signal,

$$T = \frac{1}{50} = 20\,ms$$

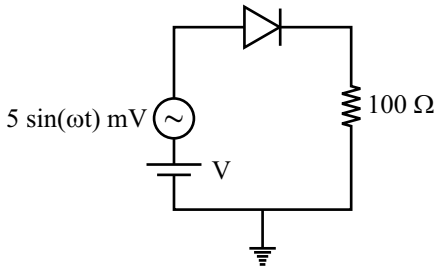
At t = 60, the input voltage is at its zero value. Then voltage across terminals p & q will be,

$$V_{pq} = V_p - V_q = V_m - (-V_m)$$

$$\Rightarrow \quad V_{pq} = 2V_m = 2 \times 100 = 200\ V$$

Example 51

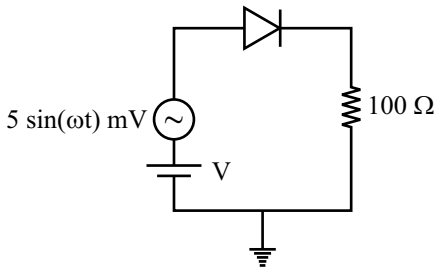
A dc current of 26 μA flows through the circuit shown. The diode in the circuit is forward biased and it has an ideality factor of one. At the quiescent point, the diode has a junction capacitance of 0.5 nF . Its neutral region resistances can be neglected. Assume that the room temperature thermal equivalent voltage is 26 mV.



For $\omega = 2 \times 10^6$ rad/s , the amplitude of the small-signal component of diode current (in μA, correct to one decimal place) is _____.

GATE(EC/2018/2M)

Solution : Ans.(6.2 to 6.6)



Frequency of supply, $\omega = 2 \times 10^6$ rad/s

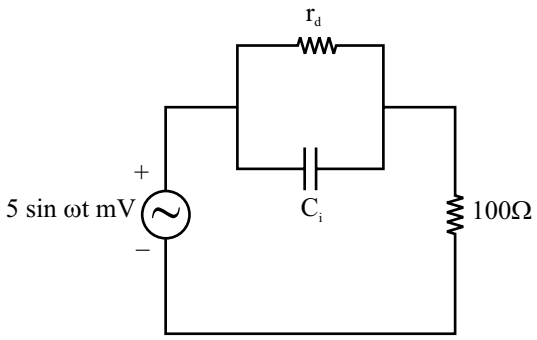
Given, Thermal voltage, $V_T = 26$ mV

DC current through diode, $I_o = 26\ \mu A = \mu A = 26 \times 10^{-3}$ mA

Dynamic resistance of diode,

$$r_d = \frac{V_T}{I_D} = \frac{26}{26 \times 10^{-3}} = 1000\Omega$$

Small signal equivalent circuit, for given diode circuit can be drawn as under.



Small signal impedance of the circuit seen by voltage source,

$$Z = 100 + \frac{r_d \times \frac{1}{j\omega C_j}}{r_d + \frac{1}{j\omega C_j}}$$

$$\Rightarrow \quad Z = 100 + \frac{1000 \times \frac{1}{j2\times10^6 \times 0.5\times10^{-9}}}{1000 + \frac{1}{j2\times10^6 \times 0.5\times10^{-9}}} = 100 + \frac{1000}{1+j1}$$

$$\Rightarrow \quad |Z| = 781.02\Omega$$

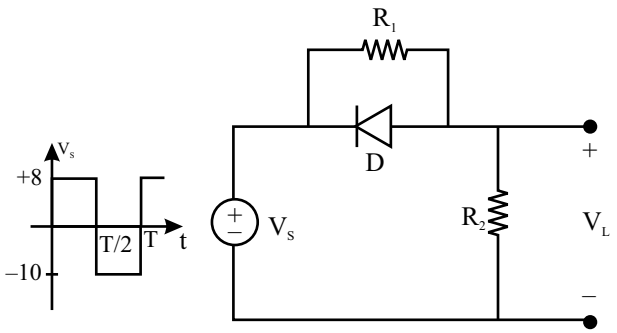
Amplitude of small signal current in the circuit,

$$i = \frac{V_m}{|Z|} = \frac{5\times10^{-3}}{781.02} = 6.4\mu A$$

Example 52

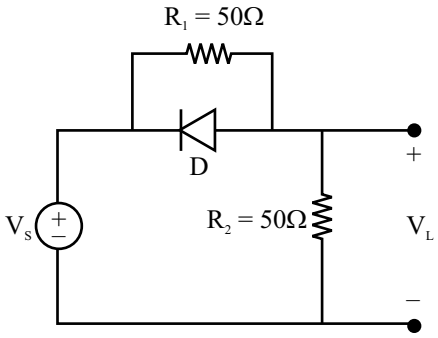
In the circuit shown, V_s is a square wave of period T with maximum and minimum values of 8 V and –10 V, respectively. Assume that the diode is ideal and $R_1 = R_2 = 50\ \Omega$.

The average value of V_L is _____ volts (rounded off to 1 decimal place).

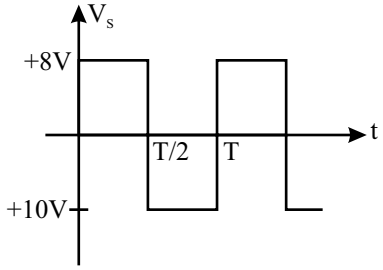


GATE(EC/2019/1M)

Solution : Ans.(-3.1 to -2.9)

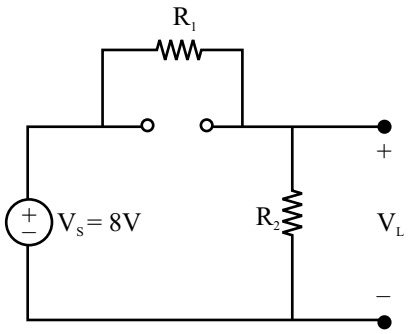


Wave form of V_s.



Case-I: Positive Half cycle

During positive half cycle of input voltage, V_s = +8. The diode D is reverse biased and acts like open circuit. The equivalent circuit becomes as under,



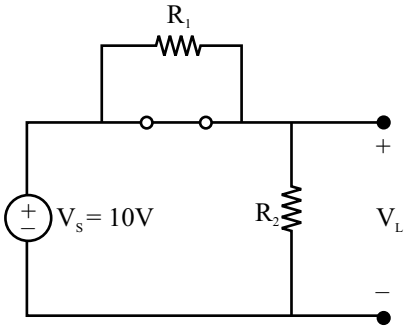
Voltage across R_2,

$$V_L = \frac{R_2}{R_1 + R_2} \times V_s = \frac{50}{50+50} \times 8$$

$\Rightarrow$ $V_L = 4V$

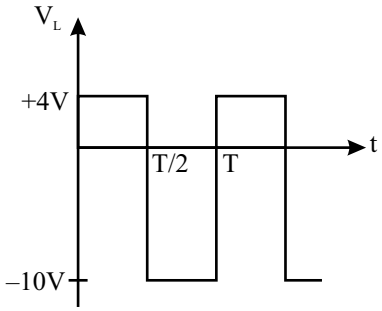
Case-II : Negative half cycle

During negative half level, $V_s = -10$. The diode 'D' is forward biased and acts like a short circuit. The equivalent circuit for negative half cycle becomes as under,



Voltage across R_2, $V_L = V_s = -10$

The wave for may V_L can be drawn as under



Average value of V_L can be given as,

$$V_{av} = \frac{1}{T}\int_0^T V_L(t)dt$$

Here, $V_L(t) = +4\ V \quad ; \ 0 < t < \frac{T}{2}$

$$= -10V \quad ; \ \frac{T}{2} < t < T$$

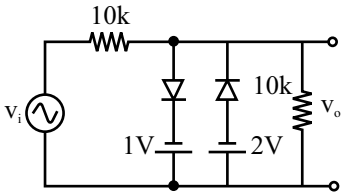
$\therefore$ $$V_{L,av} = \frac{1}{T}\left[\int_0^{T/2} 4dt + \int_{T/2}^{T} (-10)dt\right]$$

$$V_{L,av} = \frac{1}{T}\left[4\times\frac{T}{2} - 10\left(T - \frac{T}{2}\right)\right] = 2 - 5 = -3V$$

❐❐❐

GATE QUESTIONS

Q.1 Assuming the diodes to be ideal in the figure, for the output to be clipped, the input voltage v_i must be outside the range

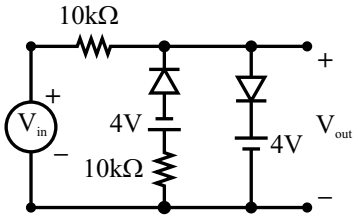


(a) –1V to –2V (b) –2V to –4V

(c) +1 V to –2V (d) +2V to –4V

GATE(EE-II/2014/2M)

Q.2 A voltage signal 10 sin ωt is applied to the circuit with ideal diode, as shown in figure. The maximum, and minimum values of the output waveform V_{out} of the circuit are respectively.

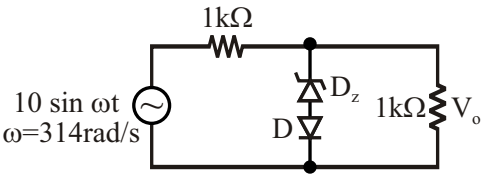


(a) + 10 V and – 10 V (b) + 4V and – 4 V

(c) + 7V and – 4 V (d) + 4 V and –7 V

GATE(EE/2003/2 M)

Q.3 The cut-in voltage of both zener diode D_z and diode D shown in Figure is 0.7 V, while break-down voltage of D_z is 3.3 V and reverse break-down voltage of D is 50V. The other parameters can be assumed to be the same as those of an ideal diode. The values of the peak output voltage (V_0) are



(a) 3.3 V in the positive half cycle and 1.4 V in the negative half cycle.

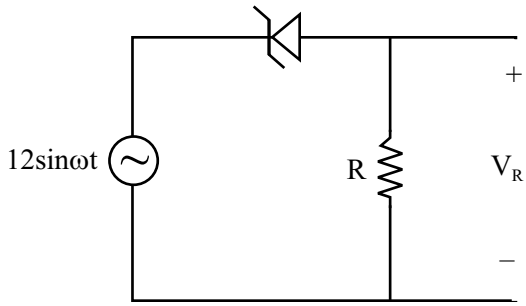
(b) 4 V in the positive half cycle and – 5 V in the negative half cycle.

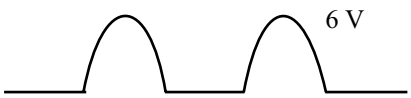
(c) 3.3 V in both positive and negative half cycles

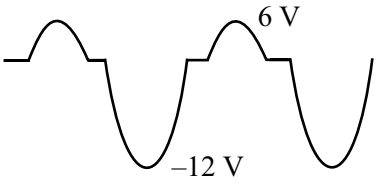
(d) 4V in both positive and negative half cycle.

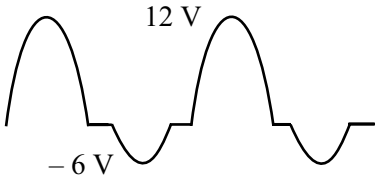
GATE(EE/2002/1 M)

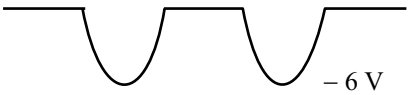
Q.4 For the circuit shown below, assume that the zener diode is ideal with a breakdown voltage of 6 Volts. The waveform observed across R is



(a) 

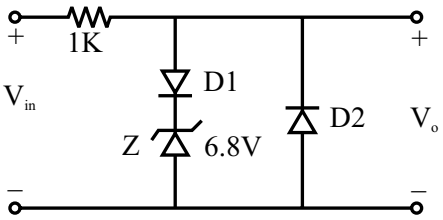
(b) 

(c) 

(d) 

GATE(EC/2006/2M)

Q.5 In the following limiter circuit, an input voltage V_i =10 sin 100πt is applied. Assume that the diode drop is 0.7 V when it is forward biased. The Zener breakdown voltage is 6.8 V.



The maximum and minimum values of the output voltage respectively are

(a) 6.1 V, – 0.7 V

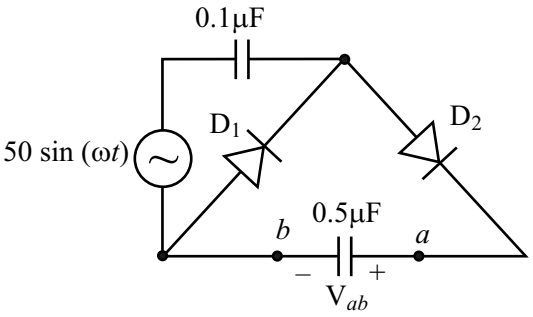
(b) 0.7 V, – 7.5 V

(c) 7.5V, – 0.7 V

(d) 7.5 V,– 7.5 V

GATE(EC/2008/1M)

Q.6 In the circuit shown, assume that diodes D_1 and D_2 are ideal. In the steady state condition, the average voltage V_{ab} (in Volts) across the 0.5 μF capacitor is .....



GATE(EC-III/2015/1M)

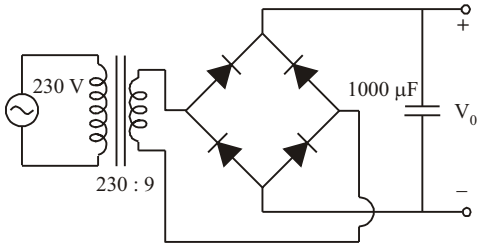
Q.7 The power delivered by a signal source with 100V r.m.s. sinusoidal voltage and 50Ω source resistance to a load consisting of a diode in series with 50Ω resistor is

(a) 25 W (b) 50 W

(c) 141 W (d) 70.7 W

GATE(IN/1997/1M)

Q.8 The peak value of the output voltage V_o across the capacitor in figure, for a 230 : 9 transformer and a 230V, 50 Hz, input, assuming 0.7 V diode drop and an ideal transformer, is

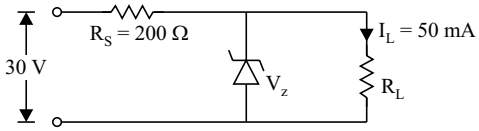


(a) 12.73 (b) 11.33

(c) 7.6 (d) 9.0

GATE(IN/2005/1M)

Q.9 The Zener diode shown in the circuit has a reverse breakdown voltage of 10 volts. The power dissipation in R_s would be

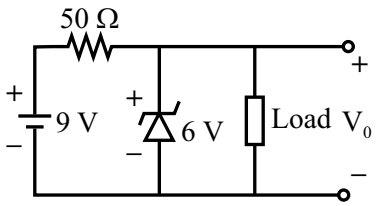


(a) 0.5 W (b) 1 W

(c) 15 W (d) 2 W

GATE(EC/1994/2M)

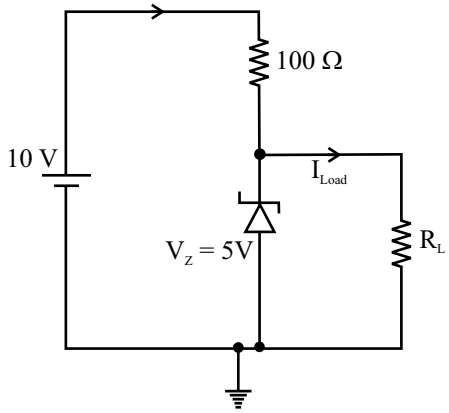
Q.10 A Zener diode in the circuit shown in figure has a knee current of 5 mA, and a maximum allowed power dissipation of 300 mW. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage V_0 constant at 6 V ?



(a) 0 mA, 180 mA
(b) 5 mA, 110 mA
(c) 10 mA, 55 mA
(d) 60 mA, 180 mA

GATE(EC/1996/2M)

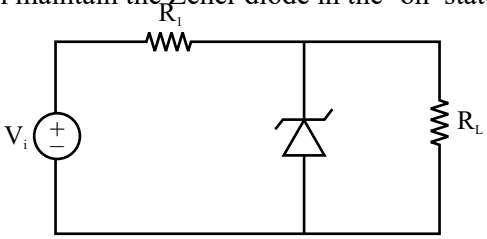
Q.11 In the circuit shown below, the knee current of the ideal Zener diode is 10 mA. To maintain 5V across R_L, the minimum value of R_L in Ω and the minimum power rating of the Zener diode in mW, respectively, are



(a) 125 and 125
(b) 125 and 250
(c) 250 and 125
(d) 250 and 250

GATE(EC/EE/IN/2013/2M)

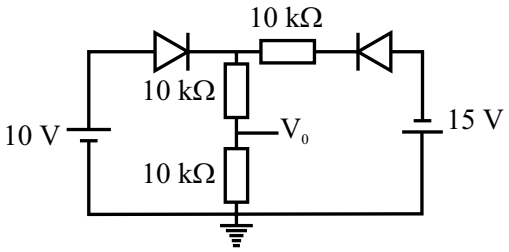
Q.12 In the circuit shown, the breakdown voltage and the maximum current of the Zener diode are 20 V and 60 mA, respectively. The values of R_1 and R_L are 200 Ω and 1 kΩ, respectively. What is the range of V_i that will maintain the Zener diode in the 'on' state?



(a) 22 V to 34 V
(b) 24 V to 36 V
(c) 18 V to 24 V
(d) 20 V to 28 V

GATE(EC/2019/2M)

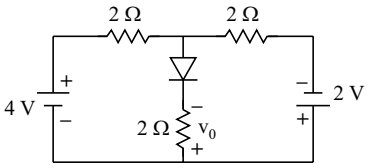
Q.13 Assuming that the diodes in the given circuit are ideal, the voltage V_0 is



(a) 4 V
(b) 5 V
(c) 7.5 V
(d) 12.12 V

GATE(EE/2010/1 M)

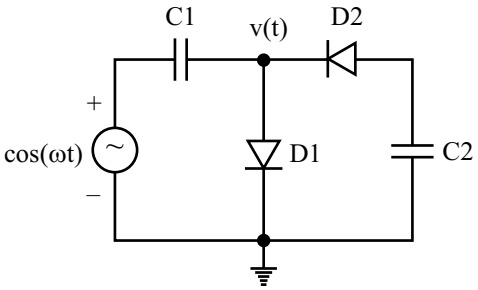
Q.14 For the circuit in figure the voltage v_0 is



(a) 2 V
(b) 1 V
(c) –1 V
(d) None of the above

GATE(EC/2000/2M)

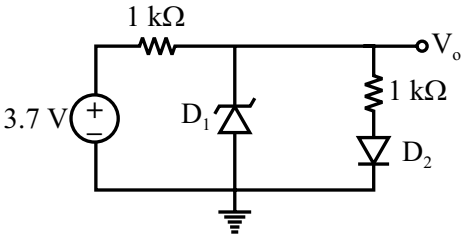
Q.15 The diodes and capacitors in the circuit shown are ideal. The voltage v (t) across the diode D1 is

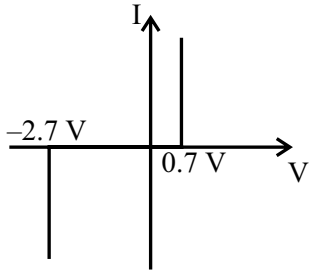


(a) cos (ωt) – 1)
(b) sin (ωt)
(c) 1 – cos (ωt)
(d) 1 – sin (ωt)

GATE(EC/2012/1M)

Q.16 Assuming Zener diode D_1 has current-voltage characteristics as shown below on the right and forward voltage drop of diode D_2 is 0.7 V, the voltage V_O in the circuit shown below is



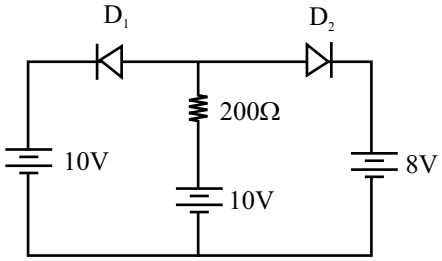


(a) 3.7 V
(b) 2.7 V

(c) 2.2 V (d) 0 V

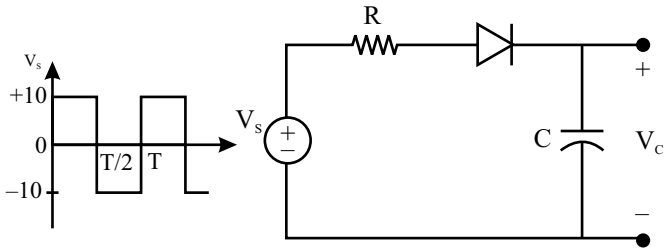
GATE(IN/2011/2M)

Q.17 For the circuit shown in the figure assume ideal diodes with zero forward resistance and zero forward voltage drop. The current through the diode D_2 in mA is_____.



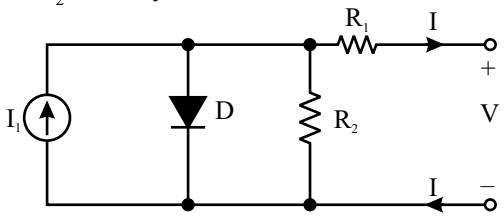
GATE(IN/2014/1M)

Q.18 In the circuit shown, Vs is a 10 V square wave of period, T = 4 ms with R = 500 Ω and C = 10 μF. The capacitor is initially uncharged at t = 0, and the diode is assumed to be ideal. The voltage across the capacitor (V_c) at 3 ms is equal to _____ volts (rounded off to one decimal place).



GATE(EC/2019/2M)

Q.19 Consider the diode circuit shown below. The diode, D, obeys the current-voltage characteristic $I_D = I_S\left(\exp\left(\frac{v_D}{nV_T}\right)-1\right)$, where $n > 1$, $V_T > 0$, V_D is the voltage across the diode and I_D is the current through it. The circuit is biased so that voltage, $V > 0$ and current, $I < 0$. If you had to design this circuit to transfer maximum power from the current source (I_1) to a resistive load (not shown) at the output, what values R_1 and R_2 would you choose?

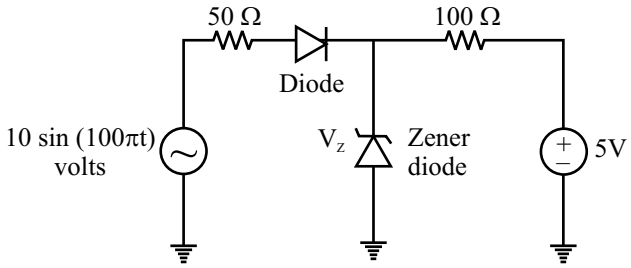


(a) Small R_1 and small R_2 (b) Large R_1 and large R_2

(c) Small R_1 and large R_2 (d) Large R_1 and small R_2

GATE(EE/2020/2M)

Q.20 If the diodes in the circuit shown are ideal and the breakdown voltage V_z of the Zener diode is 5 V, the power dissipated in the 100 Ω resistor (in watts) is _____.

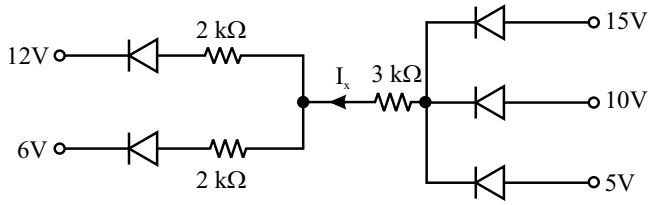


(a) 0 (b) 1

(c) 25/100 (d) 225/100

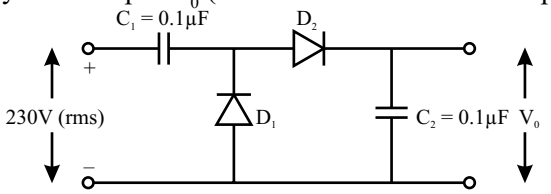
GATE(IN/2020/1M)

Q.21 Assume the diodes in the circuit shown are ideal. The current I_x flowing through the 3 kΩ resistor (in mA, rounded off to one decimal place) is _____.



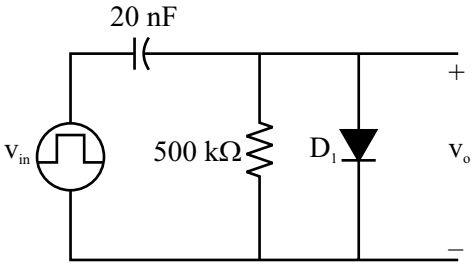
GATE(IN/2020/2M)

Q.22 In the circuit shown below, all the components are ideal and the input voltage is sinusoidal. The magnitude of the steady-state output V_0 (rounded off to two decimal places) is _____ V.



GATE(EC/2020/1M)

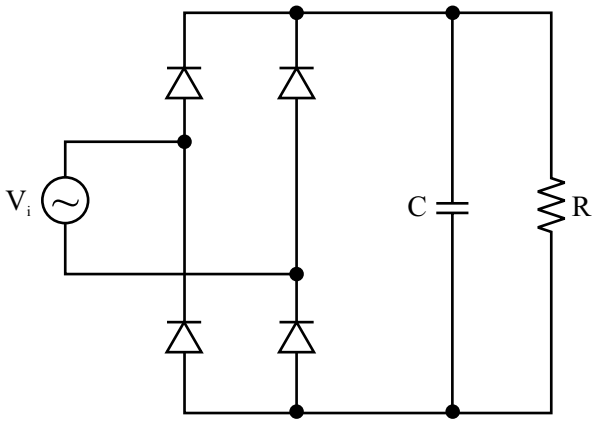
Q.23 An asymmetrical periodic pulse train v_{in} of 10 V amplitude with on-time T_{ON} = 1 ms and off-time T_{OFF} = 1 μs is applied to the circuit shown in the figure. The diode D_1 is ideal.



The difference between the maximum voltage and minimum voltage of the output waveform v_o (in integer) is _____V.

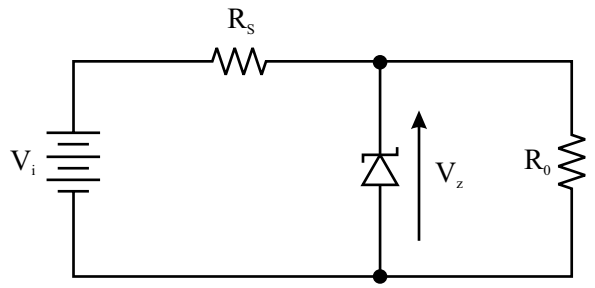
GATE(EC/2021/2M)

Q.24 In the circuit shown, the input V_i is a sinusoidal AC voltage having an RMS value of 230V± 20% . The worst-case peak-inverse voltage seen across any diode is _____ V. (Round off to 2 decimal places.)



GATE/(EE/2021/1M)

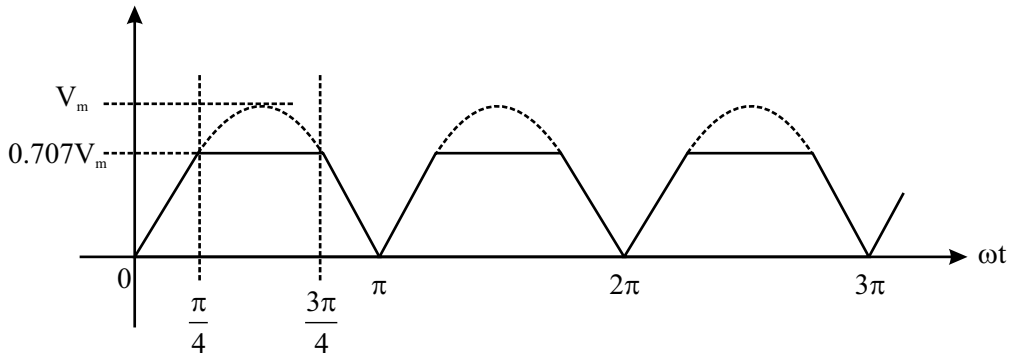
Q.25 In the circuit shown, a 5 V Zener diode is used to regulate the voltage across load R_0. The input is an unregulated DC voltage with a minimum value of 6 V and a maximum value of 8 V. The value of R_S is 6 Ω. The Zener diode has a maximum rated power dissipation of 2.5 W. Assuming the Zener diode to be ideal, the minimum value of R_0 is _____Ω.



GATE/(EE/2021/1M)

Q.26 The waveform shown in solid line is obtained by clipping a full-wave rectified sinusoid (shown dashed). The ratio of the RMS value of the full- wave rectified waveform to the RMS value of the clipped waveform is _____ .

(Round off to 2 decimal places.)



GATE(EE/2021/2M)

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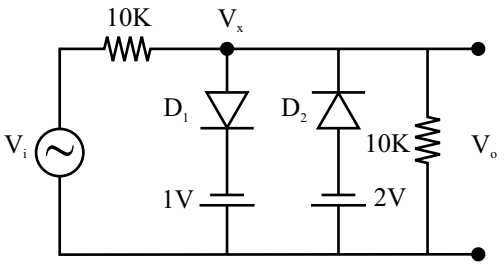
Answers & Explanations of GATE Questions

***Q.1* Ans.(b)**



The output will be clipped when either of the diode is ON.

When both diodes are off the voltage,

$$V_X = \frac{10}{10+10} \times V_i = \frac{1}{2} V_i = V_o$$

Diode D_1 is OFF when,

$$V_X < -1V$$

$$\Rightarrow \quad \frac{V_i}{2} < -1$$

$$\Rightarrow \quad V_i < -2$$

Diode D_2 is OFF when,

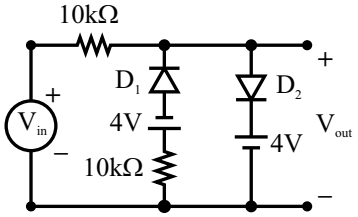
$$V_X > -2$$

$$\Rightarrow \quad \frac{V_i}{2} > -2$$

$$V_i > -4V$$

From above two cases it is observed that both diodes will be off when $-4 < V_i < -2$. Thus, either of the diode is ON and output is clipped if input voltage is outside the range $-4 < V_i < -2$.

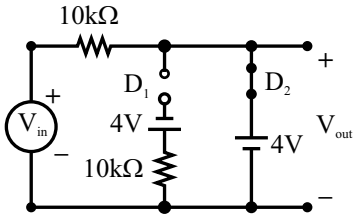
***Q.2* Ans.(d)**



In the circuit shown above it is clear that Diode D_2 turns ON only during positive half cycle and Diode D_1 turns ON only during negative half cycle of input signal.

Condition -I: D_1 is OFF and D_2 is ON

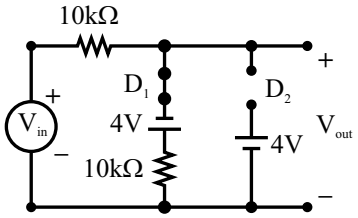
When Diode D_2 is ON and D_1 is OFF the equivalent circuit becomes as under,



When diode D_2 is ON the output voltage is clipped at level of 4 V. $\therefore V_{o,max} = 4$ V

Condition -II: D_1 is ON and D_2 is OFF

When Diode D_1 is ON and D_2 is OFF the equivalent circuit becomes as under,



Output voltage,

$$V_o = -4 + \frac{V_{in} + 4}{20} \times 10$$

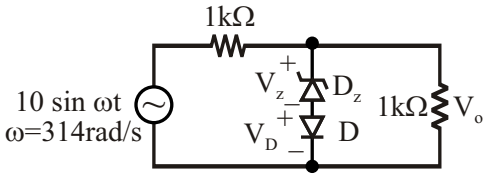
As D_1 is ON during negative half cycle only so the maximum input voltage during negative half cycle gives the maximum output voltage during negative half cycle.

Given, $V_{in,max} = -10$ V

$\therefore$ $V_{o,max} = -4 + \frac{-10 + 4}{20} \times 10 = -7$ V

Thus the maximum output voltage during positive half cycle is +4 V and during negative half cycle it is –7V.

Q.3 Ans.(b)



Case-I : Positive half cycle

$$\frac{v_{in}}{2} > (V_Z + V_D) \text{ or } v_{in} > 8V$$

$D_Z \rightarrow$ ON (Zener break down)

D→ ON (forward biased)

So, $v_o = V_Z + V_D = 3.3 + 0.7 = 4V$

when, $v_{in} < 2(V_Z + V_D)$, D_Z is OFF and $v_o = \frac{1}{2}v_{in}$

Case-II :Negative half cycle

During negative half cycle

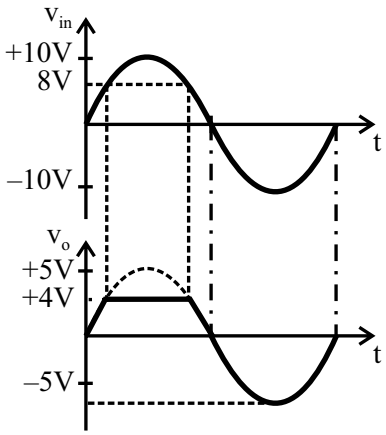
D = OFF (Reverse biased as $v_{in} < 50V$)

D_Z = OFF (Because D is OFF)

So, $v_o = \frac{1}{2}v_{in} = 5 \sin \omega t$

$v_{o\,peak} = 5$ V

waveforms :

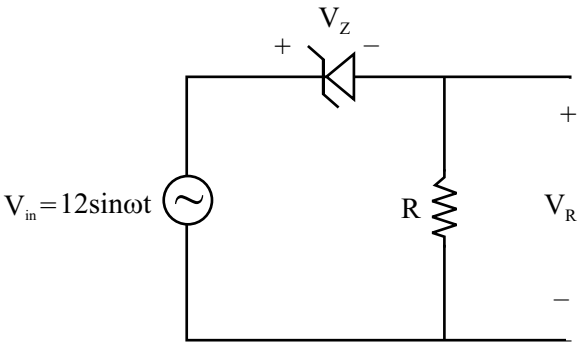


So, peak output voltage,

$v_{o\,peak}$ = 4 V ; During +ve half cycle

= – 5V ; During –ve half cycle.

Q.4 Ans.(b)



Case-I : Positive half cycle

During positive half cycle the diode is reverse biased till $V_{in} < V_z$ and forward biased for $V_{in} > V_z$.

Where V_z is breakdown voltage of diode. Therefore,

For $V_{in} < V_z$;

$V_R = 0$

For $V_{in} > V_z$;

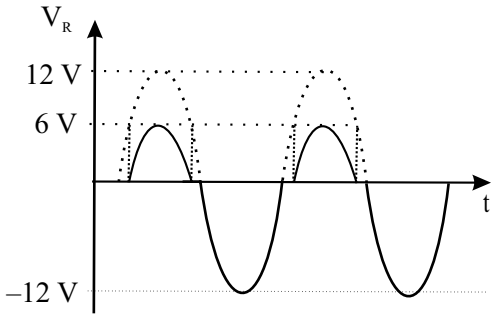
$V_R = V_{in} - V_z = 12 \sin \omega t - 6V$

Case-II: Negative half cycle

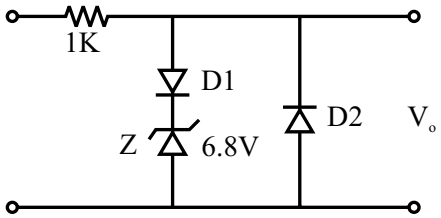
During negative half cycle the diode is forward biased . Therefore,

$V_R = V_{in} = 12 \sin \omega t$

Waveform of V_R :



Q.5 Ans.(c)



Input voltage $V_i = 10 \sin 100\pi t$

Case-I : Positive half cycle

A. when, $v_{in} > (V_Z + V_{D1})$ or $v_{in} > (6.8 + 0.7)$ V

$D_Z \rightarrow$ ON (zener break down)

$D_1 \rightarrow$ ON (forward biased)

$D_2 \rightarrow$ OFF (reverse biased)

So, $v_o = V_Z + V_{D1} = 6.8 + 0.7 = 7.5V$

B. when, $v_{in} < (V_Z + V_D)$,

$D_Z \rightarrow$ OFF (reverse biased)

$D_1 \rightarrow$ OFF (Because series connected diode D_z is OFF)

$D_Z \rightarrow$ OFF (reverse biased)

So, $v_o = v_{in} = 10 \sin 100\pi t$

Case-II: Negative half cycle

During negative half cycle,

A. when, $v_{in} > -0.7$ V

$D_Z \rightarrow$ OFF (voltage is less than cut in voltage)

$D_1 \rightarrow$ OFF (reverse biased)

$D_2 \rightarrow$OFF (voltage is less than cut in voltage)

So, $v_o = v_{in}$

B. When, $v_o < -0.7$ V

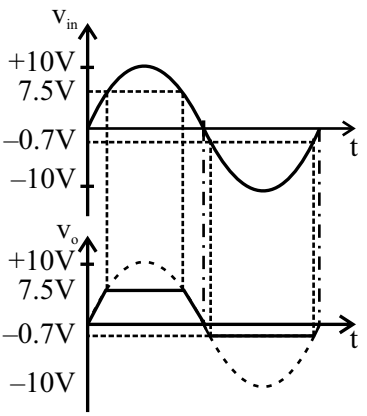
$D_Z \rightarrow$ OFF (voltage is less than cut in voltage)

$D_1 \rightarrow$ OFF (reverse biased)

$D_2 \rightarrow$ OFF (voltage is less than cut in voltage)

So, $v_o = V_{D2} = -0.7$ V

Wave forms :

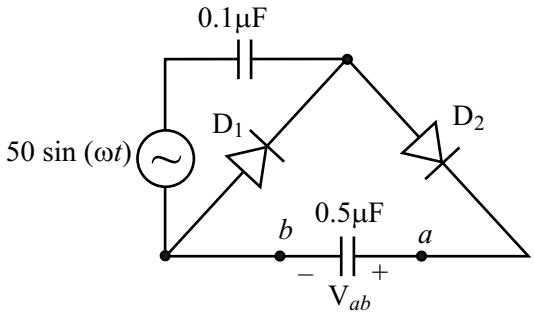


So, peak output voltage,

$v_{o\,peak}$ = 7.5 V ; During +ve half cycle

= – 0.7V ; During –ve half cycle

Q.6 Ans. 100



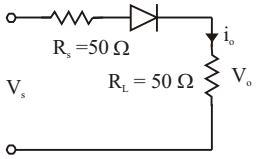
During very first negative half cycle of input voltage, the diode D_1 is forward biased and 0.1μF capacitor gets charged to peak of input voltage such that,

$$V_{C1} = 50\ V$$

and during positive half cycle just after the first negative half cycle, the diode D_1 is reverse biased and diode D_2 is forward biased and 0.5μF capacitor gets charged to V_{C1} plus peak of input voltage. So,

$$V_{ab} = (V_{C1} + 50\ V) = 100\ V$$

Q.7 Ans.(a)



The given circuit is half wave rectifier. The rms current at the output of rectifier is given by,

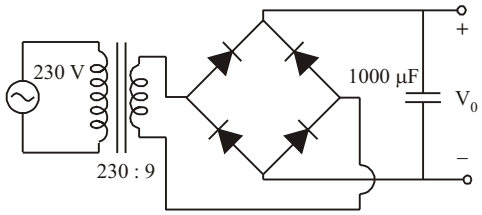
$$I_{o,rms} = \frac{I_m}{2} = \frac{1}{2}\frac{V_m}{R_s + R_L} = \frac{1}{2}\frac{\sqrt{2}V_{in,rms}}{R_s + R_L}$$

$$\Rightarrow \quad I_{o,rms} = \frac{1}{2}\frac{\sqrt{2}\times 100}{50+50} = \frac{1}{\sqrt{2}}\ A$$

The power delivered to the load,

$$\Rightarrow \quad P = I_{o,rms}^{\ 2} R_L = \left(\frac{1}{\sqrt{2}}\right)^2 \times 50 = 25W$$

Q.8 Ans.(b)



The supply voltage on secondary side of transformer is,

$$V_{s2} = \frac{9}{230} \times 230 = 9V$$

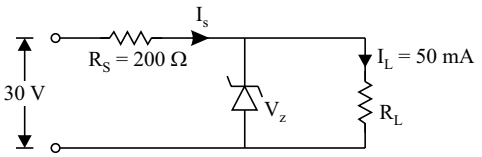
The output of transformer is connected to full wave bridge rectifier. The peak output voltage across the capacitor will be,

$$V_{o,peak} = V_m - 2V_D$$

where V_m is peak of supply voltage and V_D is voltage drop across the diode

$$\Rightarrow \quad V_{o,peak} = \sqrt{2} \times 9 - 2 \times 0.7 = 11.32 \text{ V}$$

Q.9 Ans.(d)



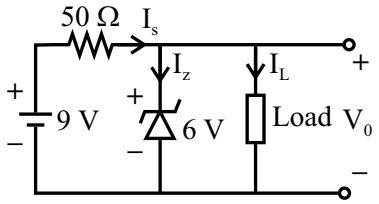
Current drawn from the source,

$$I_s = \frac{V_s - V_z}{R_s} = \frac{30 - 10}{200} = \frac{20}{200} = 0.1 \text{ A}$$

So, power dissipated in R_s ,

$$P = I_s^2 R_s = (0.1)^2 \times 200 = 2 \text{ W}$$

Q.10 Ans.(c)



Knee current is minimum current of Zener diode. Therefore, minimum Zener diode current,

$$I_{z,min} = 5 \text{ mA}$$

Maximum power dissipation,

$$P_{Z,max} = V_z \times I_{z,max}$$

$$\Rightarrow \quad 300 \times 10^{-3} = 6 \times I_{z,max}$$

$$\Rightarrow \quad I_{z,max.} = 50 \text{ mA}$$

From the circuit diagram , the source current,

$$I_s = \frac{9 - 6}{50} = 60 \text{ mA}$$

Since, the source current is constant therefore, the current through the load will be minimum when current through Zener diode is maximum.

So, minimum load current is ,

$$I_{L_{min}} = I_s - I_{Z_{max}}$$

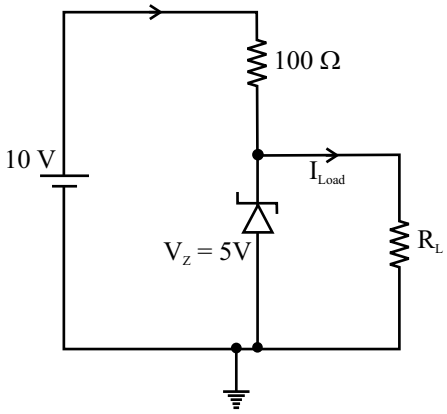
$$= 60 - 50 = 10 \text{ mA}$$

and maximum load current is ,

$$I_{L_{min}} = I_s - I_{Z_{min}} = 60 - 5$$

$$\Rightarrow \quad I_{L_{min}} = = 55 \text{ mA}$$

Q.11 In the circuit shown below, the knee current of the ideal Zener diode is 10 mA. To maintain 5V across R_L, the minimum value of R_L in Ω and the minimum power rating of the Zener diode in mW, respectively, are

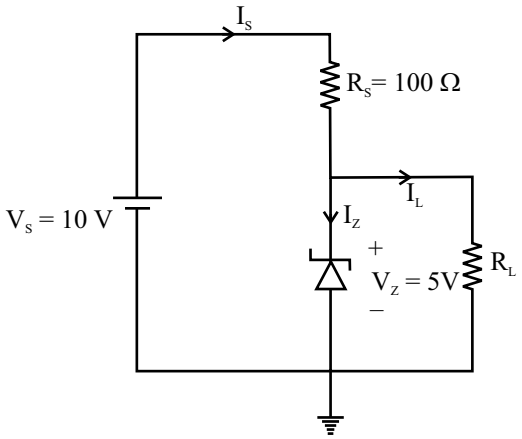


(a) 125 and 125 (b) 125 and 250

(c) 250 and 125 (d) 250 and 250

GATE(EC/EE/IN/2013/2M)

Q.11 Ans.(b)



Given, knee current of Zener diode,

$$I_{z\,knee} = 10 \text{ mA}$$

Current supplied by the source,

$$I_s = \frac{V_S - V_Z}{R_s} = \frac{10-5}{100} = 50 \text{ mA}$$

Maximum load current,

$$I_{L\,max} = I_S - I_{Z\,knee}$$

$$\Rightarrow \quad I_{L\,max} = 50 - 10 = 40 \text{ mA}$$

Minimum load resistance,

$$R_{L\,min} = \frac{V_Z}{I_{L\,max}} = \frac{5}{40\times10^{-3}} = 125\Omega$$

Maximum current in Zener diode,

$$I_{Z,\,max} = I_S$$

Maximum power dissipation of Zener diode determines the minimum power rating of Zener diode. Maximum current in Zener diode gives maximum power dissipation in diode which occurs when load current is zero. Maximum current in diode flows when load is open circuited.

$\therefore$ Maximum current in Zener diode,

$$I_{Z\,max} = I_S = 50 \text{ mA}$$

$\therefore$ Maximum power dissipation in Zener diode,

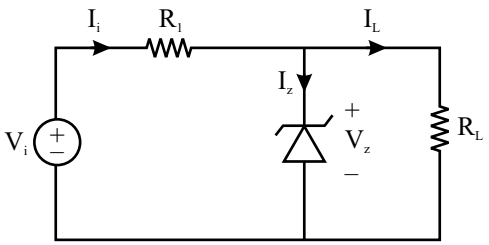
$$P_{D\,max} = V_Z\, I_{Z\,max} = 5 \times 50 \times 10^{-3} \text{ W}$$

$$\Rightarrow \quad P_{D\,max} = 250 \text{ mW}$$

$\therefore$ Minimum power rating of diode,

$$P_Z = P_{D\,max} = 250 \text{ mW}$$

Q.12 Ans.(b)



Given, $V_z = 20V,$

$$I_{Z,\,max} = 60 \text{ mA} = 60 \times 10^{-3}$$

$$R_l = 200\ \Omega$$

$$R_L = 1k\Omega = 1000\Omega$$

Load current, $I_L = \frac{V_Z}{R_L} = \frac{20}{1000} = 20mA = 20 \times 10^{-3} \text{ A}$

Input supply current,

$$I_i = I_Z + I_L$$

Maximum value of input supply current,

$$I_{i,\,max} = I_{Z,\,max} + I_L$$

$$\Rightarrow \quad I_{i,\,max} = 60 + 20\ mA = 80\ mA$$

Input supply current in term of input voltage is given by

$$I_i = \frac{V_i - V_Z}{R_1}$$

I_i is maximum when V_i is maximum

$$\therefore \quad I_{i,\,max} = \frac{V_{i,max} - V_Z}{R_1}$$

$$\Rightarrow \quad V_{i,\,max} = I_{i,\,max} R_1 + V_Z$$

$$\Rightarrow \quad V_{i,\,max} = 80 \times 10^{-3} \times 200 + 20\ V = 36\ V$$

Knee current of Zener diode is not given. So, assuming, $I_{i,\,min} = 0$

$\therefore$ Minimum supply current,

$$I_{i,\,min} = I_L = 20 \times 10^{-3}\ A$$

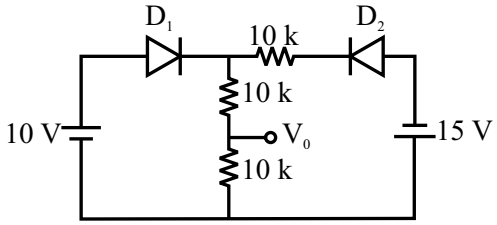
Minimum supply voltage,

$$V_{i,\,min} = I_{i,\,min} R_1 + V_Z$$

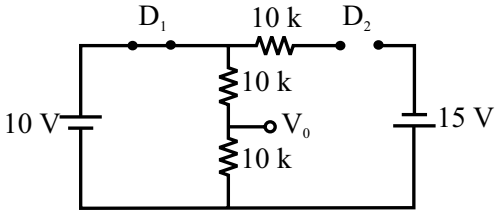
$$\Rightarrow \quad V_{i,\,min} = 20 \times 10^{-3} \times 200 + 20 = 24V$$

Thus, range of V_i for keeping the Zener diode in 'ON' state is 24V to 36V.

Q.13 Ans.(b)



In the given circuit the diode D_1 is forward biased and diode D_2 is reverse biased. So, the diode D_1 behaves like a short circuit and D_2 behaves like open circuit. Then the equivalent circuit becomes as shown under,

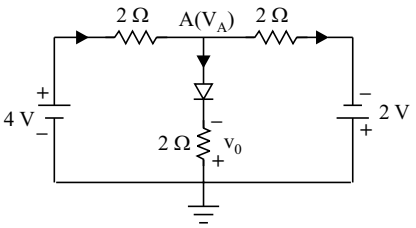


Applying the voltage divider rule, we have,

$$V_o = \frac{10}{10+10} \times 10 \text{ V} = 5 \text{ V}$$

Q.14 Ans.(d)

Let diode is ideal with $v_D = 0$



Assuming diode to be forward biased by node voltage.

The KCL at node 'A' gives,

$$\frac{V_A - 4}{2} + \frac{V_A}{2} + \frac{V_A + 2}{2} = 0$$

$$\Rightarrow \quad V_A = \frac{2}{3} Volts$$

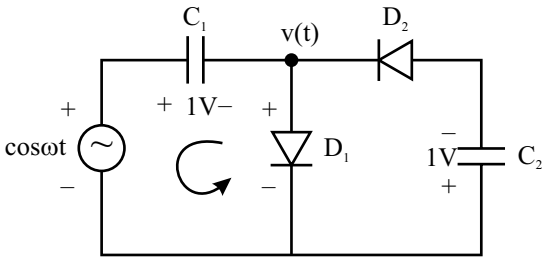
From circuit, $V_A = V_D - V_o$

$$\Rightarrow \quad V_0 = -V_A + V_D = \frac{-2}{3} + V_D$$

If diode is assume to be ideal then $V_D = 0$

$$\Rightarrow \quad V_0 = -\frac{2}{3} V$$

Q.15 Ans.(b)



The given circuit is a half wave voltage doubler. During first positive half cycle of input voltage diode D_1 is forward biased and diode D_2 is reverse biased. The capacitor C_1 gets charged to peak of input voltage. During negative half cycle of the input signal D_2 is forward biased and diode D_1 is reverse biased and capacitor C_2 gets charged to peak of input voltage as shown in figure. Once both capacitors get charged both diodes get turned of and capacitors remain charged because there in no

path for discharging of these capacitor.

Applying KVL on source side, we have,

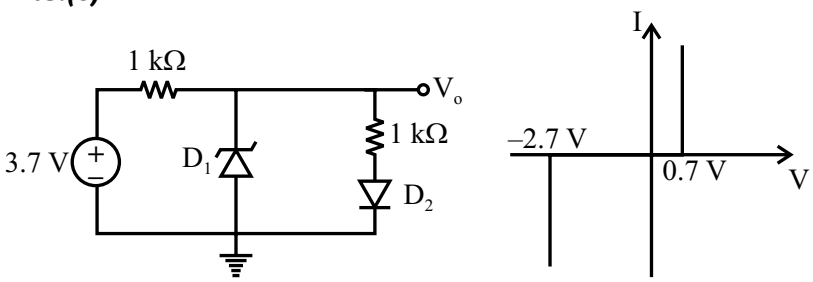
$$v(t) + v_{c1} - \cos \omega t = 0$$

$$v(t) = \cos \omega t - v_{c1}$$

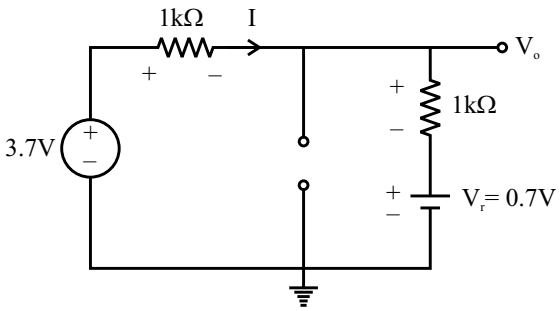
but $v_{c1} = 1V$

$\Rightarrow$ $v(t) = \cos \omega t - 1\ V$

Q.16 Ans.(c)



Let Zener diode D_1 is reverse biased but not working in breakdown region. Then D_1 behaves like open circuit. Then equivalent circuit becomes as under.



Current supplied by source,

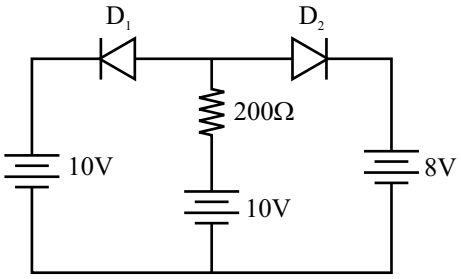
$$I = \frac{3.7 - 0.7}{2k} = 1.5mA$$

Output voltage, $V_o = 1.5 \times 1 + 0.7$

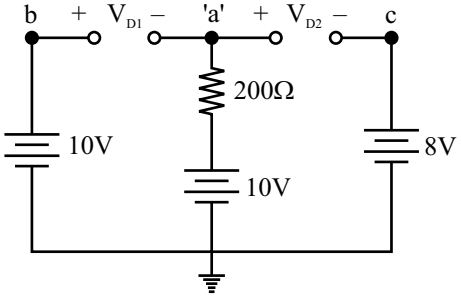
$\Rightarrow$ $\boxed{V_o = 2.2V}$

Since V_o appears across Zener diode also. This voltage is less than break down voltage of zener diode, so Zener diode is not working in breakdown region.

Q.17 Ans. 10



The diodes circuits are solved by finding which diode is ON and which is OFF. Whether a diode is ON or OFF can be checked by opening the diode and finding voltage across the diode. So, replacing both the diodes by open circuit, the equivalent circuit will be as shown below.

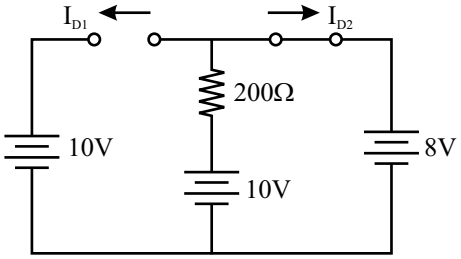


If both diodes are off then current through 200 Ω resistance is zero and voltage at node 'a' is $V_a = 10V$. Now let us find voltage across diode D_1 and D_2 under this condition,

$$V_{D1} = V_a - V_b = 10 - 10 = 0V$$

$$V_{D2} = V_a - V_c = 10 - 8 = 2V$$

Since diode are ideal therefore diode D_1 will remain off because it is not forward biased and diode D_2 will be ON as it is forward biased. Ideal diode is replaced is short circuit when it is ON and by an open circuit when it is OFF. So, equivalent circuit becomes as under,



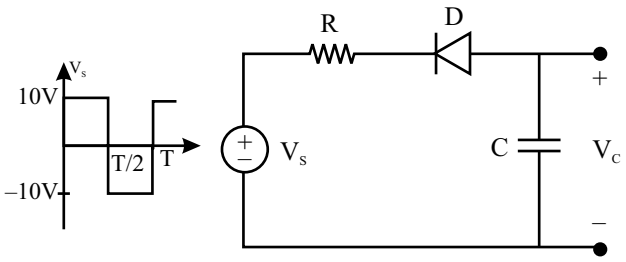
So, current through diode D_2 will be,

$$I_{D2} = \frac{10-8}{200} = 10\,mA$$

The current through diode D_1

$$I_{D1} = 0$$

Q.18 Ans.(3.2 to 3.4)



Given, $R = 500\Omega, C = 10\ \mu F$

Time period on input signal, T = 4 ms

Diode 'D' is forward biased during positive half cycle and behave like short circuit. The voltage across the capacitor during positive half cycle of input supply can be given by

$$V_c(t) = V_{c\infty} - \left(V_{c\infty} - V_{c0+}\right)e^{-\frac{t}{RC}}$$

Here, $V_{C0-} = 0$

The voltage across a capacitor can be change suddenly.

$\therefore$ $V_{C0+} = V_{C0-} = 0$

$\therefore$ $V_c(t) = V_{c\infty}(1 - e^{-\frac{t}{RC}})$

The capacitor charges to 10V at t = ∞ for input supply voltage of 10V.

$\therefore$ $V_{c\infty} = 10V$

$$V_c(t) = 10\left(1 - e^{-\frac{t}{500\times10\times10^{-6}}}\right)$$

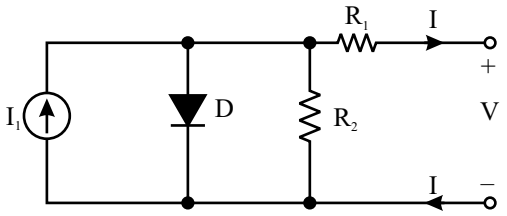
At $t = \frac{T}{2} = \frac{4\times10^{-3}}{2} = 2\times10^{-3}$

$$V_c = 10\left(1 - e^{-\frac{2\times10^{-3}}{5\times10^{-3}}}\right) = 3.29V$$

The diode is reverse biased during negative half cycle and behaves like an open circuit. So, voltage across the capacitor at t = 3 ms is same as voltage across the capacitor at $t = \frac{T}{2} = 2ms$.

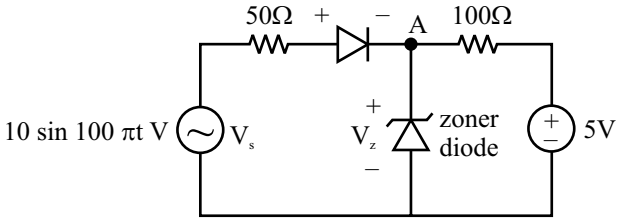
$\therefore$ $V_c(t = 3ms) = V_c(t = 2ms) = 3.29V$

Q.19 Ans(d)



For transfer of maximum power to the load the resistance R2 is kept small so the voltage drop across R2 is less than the forward bias voltage of the diode. The resistance R1 is kept large so that voltage drop across R1 is large. The large voltage drop across R1 gives large voltage across the load and hence power transferred to the load.

Q.20 Ans.(a)



Case-I : AC supply voltage less than 5V

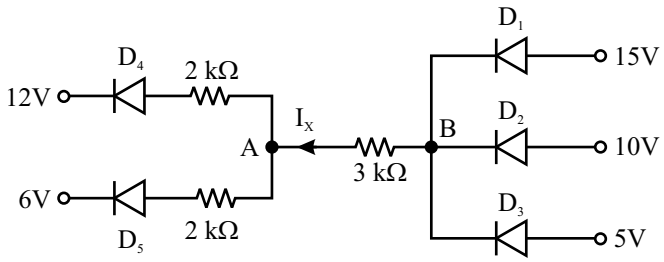
The diode D is reverse biased when AC supply voltage less than 5V and diode 'D' is OFF. Under this condition Zener diode is ON because it is reverse biased by DC supply of 5V, so, voltage V_z = 5V. But current through Zener diode is zero because if current starts flowing under this condition the voltage drop across 100Ω resistance reduces V_z below 5V and Zener diode is turned OFF.

Case-II : AC supply voltage is greater than 5V.

When AC supply becomes move than 5V, the diode D is turned ON and Zener diode operates in breakdown region with V_z = 5V. Under this condition also the voltage drop across 100 Ω resistance is zero. So, the current through 100 Ω resistance is zero under this case also.

So, the power dissipated in 100 Ω resistance is zero watt.

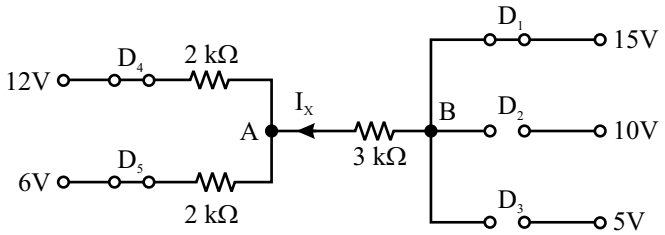
Q.21 Ans.(1.8 to 1.8)



Diode D_1 is given largest biasing voltage which forward biases the diode D_1 and reverse biases the diode D_2 and D_3. Therefore, D_1 is ON and D_2 & D_3 arc OFF.

So, voltage at node 'B' is, $V_B = 15\ V$

Assuming that anode terminals of D_4 & D_5 are at higher potential so D_4 & D_5 are forward biased so D_4 & D_5 are ON. The equivalent circuit under given biased condition can be drawn as under,



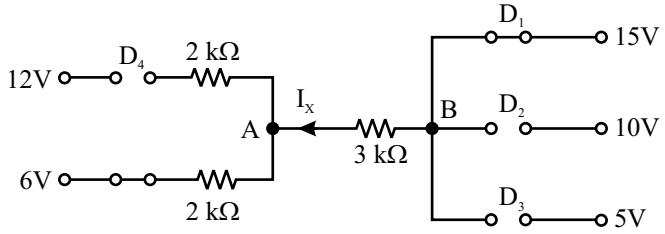
Applying KCL at node 'A', we have,

$$\frac{V_A - 12}{2} + \frac{V_A - 6}{2} + \frac{V_A - 15}{3} = 0$$

$$8V_A - 84 = 0$$

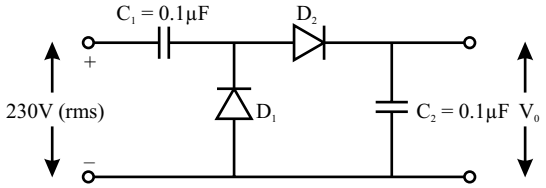
$$V_A = \frac{84}{8} = \frac{21}{2} = 10.5\,V$$

Under this condition V_A is 10.5 V which is less than 12 V so diode D_4 must reverse biased and it must be OFF. Under such condition equivalent circuit is drawn by opening terminals of diode D_4 as under,



$\therefore$ Current, $$I_x = \frac{V_A - 6}{2+3}\,mA = \frac{15-6}{5}\,mA = 1.8\,mA$$

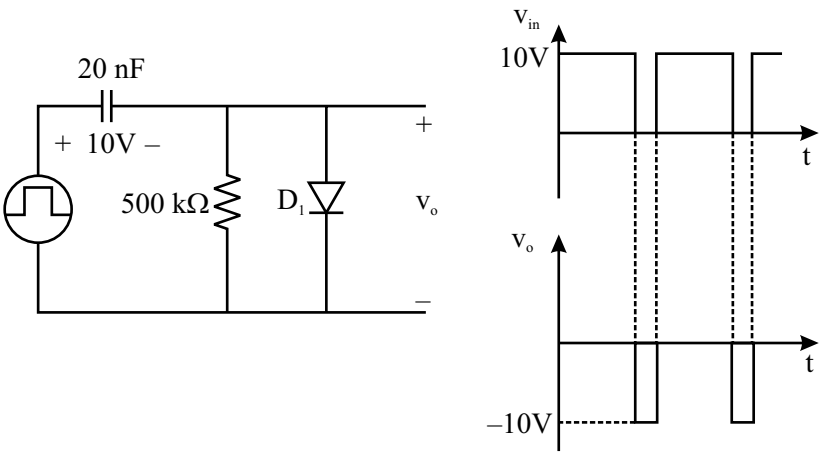
Q.22 Ans(644 to 657)



The given circuit is a half wave voltage doubler circuit. The output voltage V_o across capacitor C_2 of the circuit is twice the peak value of input supply voltage.

$\therefore$ $$V_o = 2\times\sqrt{2}\,V_{in,rms} = 2\times\sqrt{2}\times 230 \approx 650.54V$$

Q.23 Ans.(10 to 10)



Given, $T_{ON} = 1$ ms

$T_{OFF} = 1$ μs

Time constant of circuit,

$$\tau = RC = 500 \times 10^3 \times 20 \times 10^{-9} = 10^{-2} = 10 \text{ ms}$$

The diode D_1 gets forward biased during very first positive half cycle and capacitor get charged to +10V with polarity as shown in circuit. The output voltage is zero during T_{ON} period. The diode gets reverse biased during T_{OFF} period. The capacitor does not discharge because the time constant of circuit is very large in caparison to T_{OFF}.

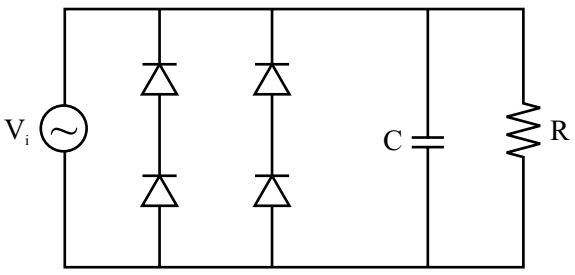
Thus the output voltage during T_{OFF} period is,

$$v_o = -v_c = -10V$$

The waveforms of input and output voltages are as shown Fig. above. Thus, the difference between maximum and minimum output voltages is,

$$\Delta v_o = V_{o,\,max} - V_{o,\,min} = 0 - (-10) = 10 \text{ V}$$

Q.24 Ans.(389 to 391)



Given circuit is a full wave rectifier whose peak inverse voltage is given by,

$$PIV = V_m$$

Where V_m is peak value of input supply voltage.

Given, $V_{rms} = 230 \text{ V} + 2\%$

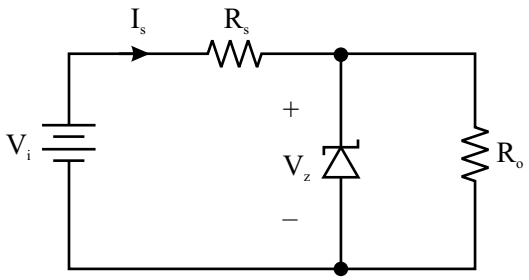
Maximum possible value of rms input voltage

$$V_{rms,\,max} = 230 + 0.2 \times 230 = 276\ V$$

$\therefore$ Worst or maximum posible PIV,

$$(PIV)_{max} = \sqrt{2} \times 276 = 390.32\,V$$

Q.25 Ans.(29.00 to 31.00)



Given, $V_z = 5V$

$V_i = 6\Omega$

$P_{z,\,max} = 2.5\ W = V_z\, I_{z,\,max}$

$\therefore$ $I_{z,\,max} = \dfrac{2.5}{V_z} = \dfrac{25}{5} = 0.5A$

Supply current, $I_s = \dfrac{V_i}{R_s}$

Maximum supply current,

$$I_{s,\,max} = \frac{V_{i,max} - V_z}{R_s} = \frac{8-5}{6}A = 0.5A$$

Minimum supply current,

$$I_{s,\,min} = \frac{V_{i,min} - V_z}{R_s} = \frac{6-5}{6} = \frac{1}{6}A$$

Load current, $I_L = I_s - I_z$

Maximum load current, $I_{L,\,max} = I_{s,\,min} - I_{z,\,min}$

Let minimum or knee current of zener diode is zero.

$\Rightarrow$ $I_{L,max} = I_{s,min} = \dfrac{1}{6}A$

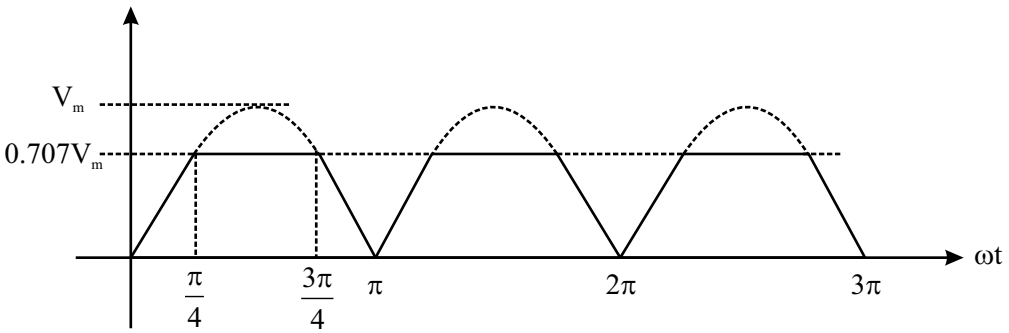
Load resistance, $R_o = \dfrac{V_z}{I_L}$

Minimum load resistance,

$$R_{o,\,min} = \frac{V_z}{I_{L,max}} = \frac{5}{1/6}\Omega$$

$$R_{o,\,min} = 30\ \Omega$$

Q.26 Ans.(1.20 to 1.23)



RMS value of unclipped rectified wave,

$$V_{rms1} = \frac{V_m}{\sqrt{2}} = 0.707V_m$$

RMS value of clipped waveform,

$$V_{rms2} = \sqrt{\frac{1}{\pi}\left[\int_0^{\frac{\pi}{4}} V_m^2 \sin^2 \omega t\ d(\omega t) + \int_{\pi/4}^{\frac{3\pi}{4}} (0.707V_m)^2\ d(\omega t) + \int_{\frac{3\pi}{4}}^{\pi} V_m^2 \sin^2 \omega t\ d(\omega t)\right]}$$

$$\Rightarrow \quad V_{rms2} = \sqrt{\frac{V_m^2}{\pi}\left[\frac{1}{2}\left(\omega t - \frac{\sin 2\omega t}{2}\right)_0^{\pi/4} + \frac{\pi}{4} + \frac{1}{2}\left(\omega t - \frac{\sin 2\omega t}{2}\right)_{\frac{3\pi}{4}}^{\pi}\right]}$$

$$\Rightarrow \quad V_{rms2} = V_m\sqrt{\frac{1}{\pi}\left[\frac{1}{2}\left(\frac{\pi}{4} - \frac{1}{2}\right) + \frac{\pi}{4} + \frac{1}{2}\left(\frac{\pi}{4} - \frac{1}{2}\right)\right]}$$

$$\Rightarrow \quad V_{rms2} = V_m\sqrt{\frac{1}{\pi}\left[\frac{\pi}{4} - \frac{1}{2}\right] + \frac{1}{4}} = 0.575V_m$$

$$\therefore \quad \frac{V_{rms1}}{V_{rms2}} = \frac{0.707\,V_m}{0.575\,V_m} = 1.229$$

❐❐❐

Ch 2 BJT Biasing and Thermal Stablization

2.1 Concept of Q-point and load line

Consider a BJT biasing circuit shown in Fig.1. In the amplifier circuit shown in the Fig.1, the capacitors C_i and C_o are called input and output coupling capacitors, respectively. The coupling capacitors are used to block DC biasing signals from AC input and output signals of the amplifier. The coupling capacitors are replaced by open circuit for DC analysis and by short circuit for small signal AC analysis. Therefore, the coupling capacitors will not be shown in remaining part of this chapter for DC analysis.

If only DC biasing signals are considered then the KVL in collector circuit can be written as,

$$V_{CC} = I_C R_C + V_{CE} \quad (1)$$

$$\Rightarrow \quad I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\Rightarrow \quad I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad (2)$$

Above equation represents a straight line on output characteristics of BJT with slope of line equal to $-\frac{1}{R_C}$ and intercept on I_C-axis at $\frac{V_{CC}}{R_C}$ and intercept on V_{CE}-axis at V_{CC} as shown in Fig. 2. The straight line represented by above equation is called as DC load line of the amplifier circuit.

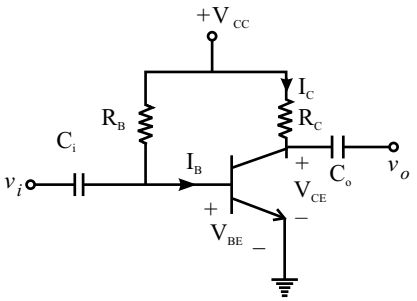


Fig. 1 BJT amplifier with fixed bais

The DC biasing base current can be obtained by applying KVL in the base circuit as under,

$$V_{CC} = I_B R_B + V_{BE} \tag{3}$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4}$$

The DC load line of amplifier circuit along with output characteristics and operating point are shown in Fig. 2

Operating Point

The intersection of DC load line with output characteristics corresponding to base current of the circuit is called the operating point or Q- point of the amplifier. The operating point is denoted by co-ordinates (V_{CEQ}, I_{CEQ}) on the output characteristics as shown in Fig.2.

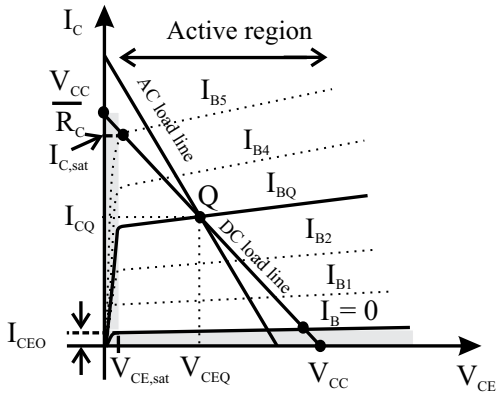


Fig.2 DC load line overlapped with output characteristics of the amplifier circuit

AC Load Line

For AC signals coupling capacitor is short circuited then load line is called AC load line. The AC load line can be drawn with a slope of $-\left[\frac{1}{R_C} + \frac{1}{R_L}\right]$ The R_C and R_L appear in parallel for AC analysis.

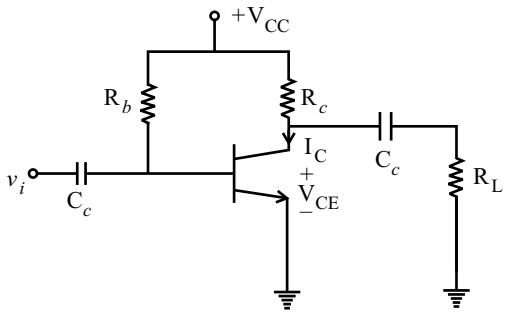


Fig. 3 BJT amplifier with fixed bais and load resistance R_L.

$$\text{Slope} = -\left[\frac{1}{R_C} + \frac{1}{R_L}\right] \tag{5}$$

When load impedance is also considered the slope of the load line becomes more negative. The selection of Q-point on a.c load line should be such that the Q-point remains in the active region for wide variations in input signal.

2.2 Biasing of BJT

Establishing the Q-point or operating point in output characteristics of a transistor with external DC voltage applied at base and collector terminals in Common-Emitter configuration or at emitter and collector in common base configuration or at collector and base in common collector configuration is called biasing of the transistor. Biasing of the transistor is essential, so that the operating point remains in desired region i.e. active region, saturation or cut off, for complete range of the input signal. For active region of operation the Q-point is located at center of load line for distortion free output signal. The load line and various regions of operation of BJT amplifier are shown in Fig. 4.

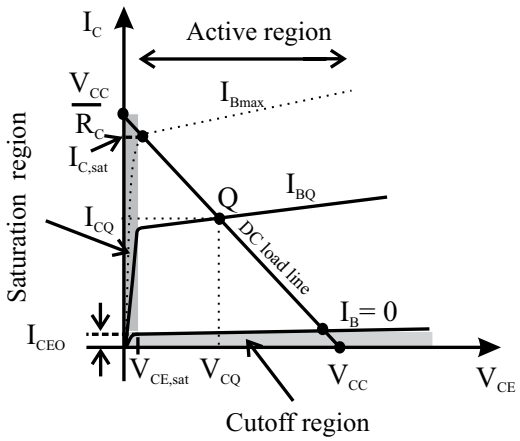


Fig.4 Regions of operation and load of CE configuration of BJT

There are three regions of operations of a BJT called active, saturation and cutoff regions which have discussed in details along with BJT characteristics. These regions are summarized as follows,

Active Region

A BJT operates in active region when emitter is in forward bias and collector in reverse bias. BJT works like a linear amplifier in active region of operation. The collector current for active region is given by,

$$I_C = \beta I_B = \frac{\alpha}{1-\alpha} I_B \tag{6}$$

Saturation Region

A BJT operates in saturation region when both emitter and collector in are forward biased.

When base current of BJT is increased the Q-point shifts from cut-off to active and then active to saturation region. The base current at the boundary of saturation and active region is given by,

$$I_B = \frac{I_{C,sat}}{\beta} \tag{7}$$

where, $$I_{c,\,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C} \quad (8)$$

The current $I_{C,\,sat}$ is collector current at boundary separating active and saturation regions.

The base current given by equation (7) is maximum current for active region and minimum current for saturation region. For saturation region, $V_{CE} = V_{CE,sat}$, when $V_{CE\,(catculated)} > V_{CE,sat}$, the BJT operates in active region. The BJT behaves like a closed switch when it operates in saturation region.

Cut-off region :

If BJT operates in cut-off region then both emitter and collector junctions are reverse biased. BJT. The BJT behaves like an open switch when it operates in cutoff region of operation.

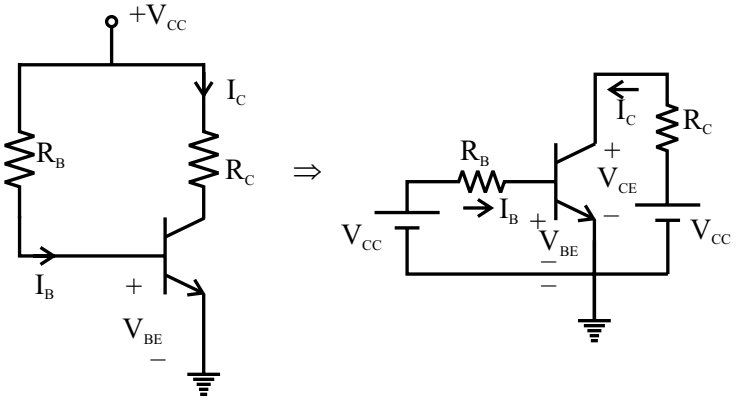
Steps of DC or Bias Analysis of BJT

i) Base current is obtained from base circuit by appling KVL
ii) Circuit is assumed in active region so that $I_C = \beta I_B$
iii) V_{CE} is obtained from collector circuit by taking $I_C = \beta I_B$
iv) If calculated value of V_{CE} is more then $V_{CE,sat}$ then BJT operates in active region else in saturation
v) If BJT operates in active region then values of I_C and V_{CE} calculated in (ii) and (iii) give Q-point
vi) If BJT operates in saturation region then $V_{CE}$is taken as $V_{CE,\,sat}$ and collector current is again calculated by taking $V_{CE} = V_{CE\,sat}$ because the relation $I_C = \beta I_B$ is not applicable to saturation region.
vii) When BJT operates in saturation region the the value of $V_{CE,\,sat}$ and collector current obtained in step (vi) give operating point.

2.3 Fixed Bias Circuits of BJT

2.3.1 Fixed Base Bias Circuit

The base circuit of fixed bias circuit is biased by connecting a resistor R_B between base and supply voltage , V_{CC} and collector circuit is biased through resistor R_C from s signal source of supply as shown in Fig. 5 (a). The circuit can be redrawn by separating base and collector circuits as shown in Fig. 5 (b).



(a) Fixed base bias b) Equaivalent circuit of fixed base bias

Fig.5 Fixed base bias circuit of CE configuration of BJT

Applying KVL in the base circuit, we have,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{9}$$

Let BJT operates in active region such that $I_C = \beta I_B$ (10)

Applying KVL in the collector circuit, we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_C \tag{11}$$

$$\Rightarrow \quad V_{CE} = V_{CC} - \beta I_B R_C \tag{12}$$

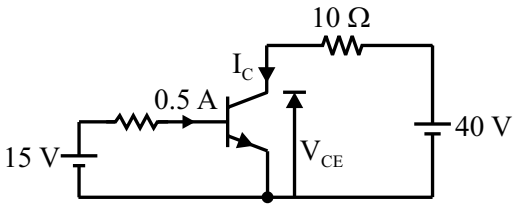
i. If $V_{CE} > V_{CE,\,sat}$ then BJT operates in active region with V_{CEQ} given by equation (12) and I_{CQ} given by equation (10).

ii. If $V_{CE} < V_{CE,\,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,\,sat}$ and I_{CQ} is obtained using equation (11) by replacing $V_{CE} = V_{CE,\,sat}$ as under,

$$I_{CQ} = \frac{V_{CC} - V_{CE,sat}}{R_C} \tag{13}$$

Example 1

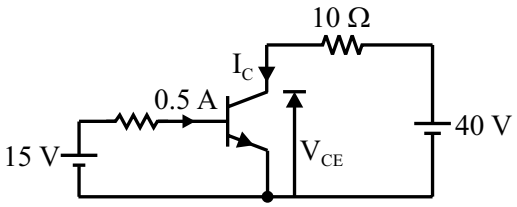
In the circuit shown in figure, the current gain (β) of the ideal transistor is 10. The operating point of the transistor (V_{CE}, I_C) is



(a) (40 V, 4A)
(b) (40V, 5A)
(c) (0V, 4A)
(d) (15V, 4A)

GATE(EE/2003/2 M)

Solution : Ans.(c)



Since base-emitter junction is forward biased in above circuit so, BJT is operating either in saturation or in active region but not in cut off.

Given, $\beta = 10, \quad I_B = 0.5$ A

Let the transistor is operating in active region.

$$\Rightarrow \quad I_C = \beta I_B = 10 \times 0.5 = 5 \text{ A}$$

From the collector circuit,

$$V_{CE} = V_{CC} - I_C R_C = 40 - 5 \times 10 = -10 \text{ V}$$

$$V_{CB} = V_{CE} - V_{BE,active} = -10 \text{ V} - 0.7 = -10.7 \text{ V}$$

Negative value of V_{CB} represents forward biased collector junction. Since V_{CB} is negative, therefore, the transistor must be operating in saturation region.

For saturation region ,

$$V_{CE,sat} = 0.2 \text{ V} \approx 0 \text{ V}$$

So, from collector circuit,

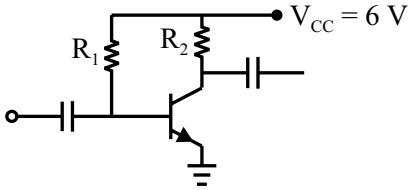
$$V_{CE,sat} = V_{CC} - I_C R_C = 0$$

$$\Rightarrow \quad I_C = V_{CC}/R_C = 40/10 = 4 \text{ A}$$

So, the operating point (V_{CEQ}, I_{CQ}) of the transistor is (0V, 4A).

Example 2

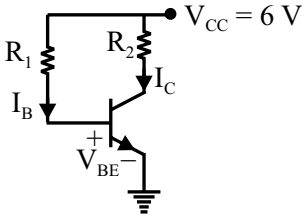
In the amplifier circuit shown in figure, the values of R_1 and R_2 are such that the transistor is operating at V_{CE} = 3 V and I_C = 1.5 mA when β is 150. For a transistor with β of 200, the operating point (V_{CE}, I_C) is



(a) (2 V, 2 mA)
(b) (3 V, 2 mA)
(c) (4 V, 2 mA)
(d) (4 V, 1 mA)

GATE(EC/2003/2M)

Solution : Ans.(a)



Given, $V_{CE} = 3$ V, $I_C = 1.5$ mA, $\beta = 150$

Base current of transistor amplifier is given by,

$$I_B = \frac{I_C}{\beta} = \frac{1.5}{150} mA = 10 \ \mu\text{A} = 0.01 \text{ mA}$$

From the base emitter circuit,

$$V_{CC} - I_B R_1 - V_{BE} = 0$$

$$6 - 0.01 R_1 - 0.7 = 0$$

$$\Rightarrow \quad R_1 = \frac{6 - 0.7}{0.01} = \frac{5.30}{0.01} = 530 \text{ k}\Omega$$

From the collector emitter circuit,

$$V_{CC} - I_C R_2 - V_{CE} = 0$$
$$6 - 1.5\, R_2 - 3 = 0$$
$$\Rightarrow \quad R_2 = \frac{6-3}{1.5} = 2\, k\Omega$$

When , $\beta = 200$,

From base- emitter cicuit,

$$V_{CC} - I_B R_1 - V_{BE} = 0$$
$$6 - I_B \times 530 - 0.7 = 0$$
$$\Rightarrow \quad I_B = \frac{6-0.7}{R_1} = \frac{5.3}{530} = 10\ \mu A$$

Collector current,

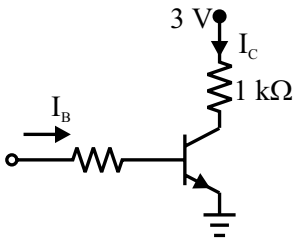
$$I_C = \beta I_B = 200 \times 10 = 2\ mA$$

From the collector emitter circuit,

$$V_{CC} - I_C R_2 - V_{CE} = 0$$
$$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_2 = 6 - 2 \times 2 = 2\ V$$

Example 3

Assuming $V_{CEsat} = 0.2$ V and $\beta = 50$, the minimum base current (I_B) required to drive the transistor in figure to saturation is

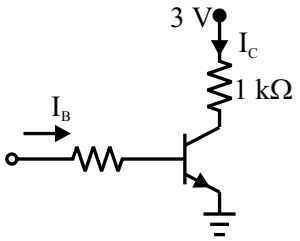


(a) 56 μA (b) 140 μA

(c) 60 μA (d) 3 μA

GATE(EC/2004/1M)

Solution : Ans.(a)



Given, $\beta = 50$,

Since $V_{CE,sat} = 0.2\ V$

From the collector circuit ,

$$I_{C,sat} = \frac{(V_{CC} - V_{CE,sat})}{R} = \frac{3 - 0.2}{1} = 2.8mA$$

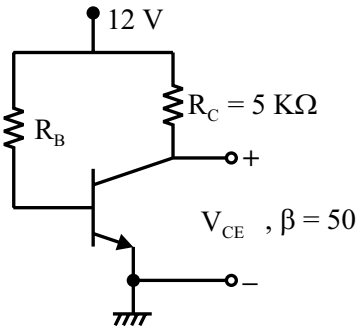
Minimum value of base current required to drive the transistor in saturation region is given by,

$$I_{B\,min} = \frac{I_{C,sat}}{\beta}$$

$$\Rightarrow \quad I_{B\,min.} = \frac{2.8}{50} = 56\ \mu A$$

Example 4

For a silicon BJT shown in Figure, find R_B to establish $V_{CE} = 2V$, Assume $V_{BE} = 0.7$ V.

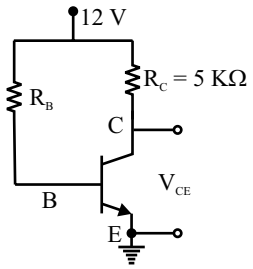


(a) 283 kΩ (b) 10 kΩ

(c) 200 kΩ (d) 242 kΩ

GATE(IN/1998/1M)

Solution : Ans.(a)



Given, $V_{BE} = 0.7\ V$, $\beta = 50$

and $V_{CE} = 2\ V$,

Collector current, $I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{12 - 2}{5} = \frac{10}{5} = 2\ mA$

Voltage, $V_{CB} = V_{CE} - V_{BE,active} = 2 - 0.7 = 1.3\ V$

Positive value of V_{CB} represents reverse biased collector junction. Since V_{CB} is positive, therefore,

the transistor is operation in active region.

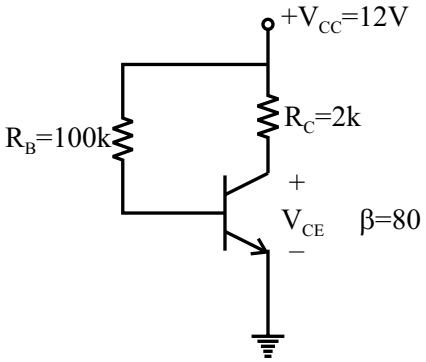
Base current of transistor in active region,

$$I_B = \frac{I_C}{\beta} = \frac{2}{50} = 0.04\ mA$$

From base circuit, $$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{0.04} = \frac{11.3}{0.04} = 282.5\ k\Omega$$

Example 5

The biasing circuit of a silicon transistor is shown below. If β = 80, what is V_{CE} for the transistor?

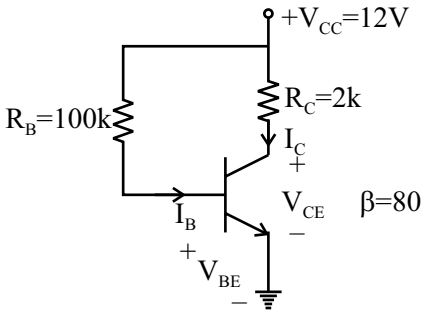


(a) – 6.08 V (b) 0.2V

(c) 1.2V (d) 6.08 V

GATE(IN/2006/2M)

Solution : Ans.(b)



KVL in base circuit gives,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow \quad 12 - I_B \times 100 - 0.7 = 0$$

$$I_B = \frac{12 - 0.7}{100} = 0.113\ \text{mA}$$

Let BJT is operating in active region with,

$$I_C = \beta I_B$$

$\therefore \quad I_C = 80 \times 0.113 = 9.04 \text{ mA}$

Applying KVL in collector circuit, we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow \quad V_{CE} = 12 - 9.04 \times 2 = -6.08 \text{ V}$$

Voltage across collector junction,

$$V_{CB} = V_{CE} - V_{BE}$$

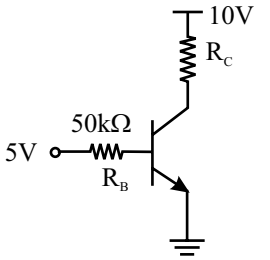
$$\Rightarrow \quad V_{CB} = -6.08 - 0.7 = -6.78$$

Negative value of V_{CB} for npn BJT indicates that collector junction is forward biased and the BJT operates in saturation region.

For saturation region, $V_{CE,\,sat} = 0.2 \text{ V}$

Example 6

In the circuit shown, the silicon BJT has $\beta = 50$. Assume $V_{BE} = 0.7$ and $V_{CE(sat)} = 0.2$ V. Which one of the following statements is correct?



(a) For $R_C = 1$ kΩ, the BJT operates in the saturation region

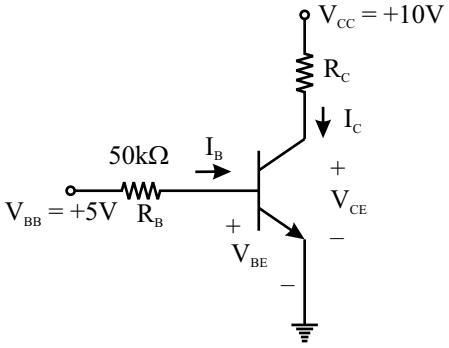
(b) For $R_C = 3$ kΩ, the BJT operates in the saturation region

(c) For $R_C = 20$ kΩ, the BJT operates in the cut off region

(d) For $R_C = 20$ kΩ, the BJT operates in the linear region

GATE(EC-III/2014/2M)

Solution : Ans (b)



Given, $V_{BE} = 0.7\text{V}$

$V_{CE(sat)} = 0.2\text{V}$

$\beta = 50$

The BJT operates in cutoff region when both collector and emitter junctions are reverse biased. Here base is given positive potential and emitter is grounded so emitter junction is forward biased. Therefore, the BJT is either in active or in saturation region depending on value of R_C.

From base circuit,

$$V_{BB} - R_B I_B - V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 - 0.7}{50}\text{mA} = 86\ \mu\text{A}$$

Let BJT is in saturation then, KVL in collector circuit gives,

$$V_{CC} = R_C I_{C,sat} - V_{CE(sat)} = 0$$

$$\Rightarrow \quad I_{C,sat} = \frac{10 - 0.2}{R_C} \qquad \text{.....(i)}$$

Minimum base current required for saturation is given by,

$$I_{B\,min} = \frac{I_{C,sat}}{\beta}$$

$\therefore$ For saturation, $I_B > \dfrac{I_{C,sat}}{\beta}$

or $$I_{C,\,sat} \leq \beta I_B$$

$$\Rightarrow \quad I_{C,sat} \leq 50 \times 86 \times 10^{-6}$$

Therefore, for saturation region,

$$\frac{10 - 0.2}{R_C} \leq 50 \times 86 \times 10^{-6}$$

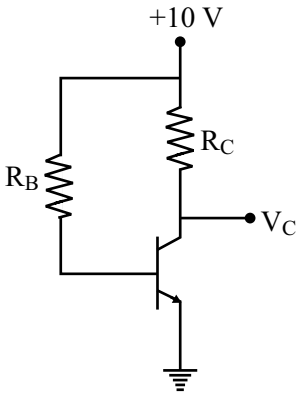
$$\Rightarrow \quad R_C \geq \frac{9.8}{50 \times 86 \times 10^{-6}}$$

$$\Rightarrow \quad R_C \geq 2.28\ \text{k}\Omega$$

So, option (b) is correct.

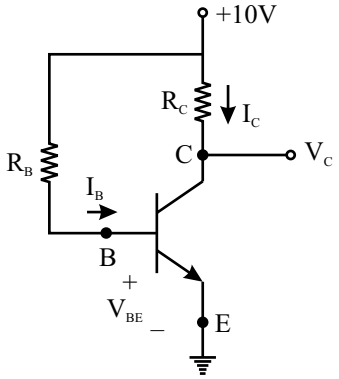
Example 7

In the following circuit, the transistor is in active mode and $V_C = 2$V. To get $V_C = 4$ V, we replace R_C with R_C'. Then the ratio $\dfrac{R_C'}{R_C}$ is .....



GATE(EE-II/2015/1M)

Solution : Ans. 0.74 to 0.76



Current in base circuit,

$$I_B = \frac{10 - V_{BE}}{R_B}$$

For active region of BJT, $V_{BE} = 0.7$

$$\Rightarrow \quad I_B = \frac{10 - 0.7}{R_B} = \frac{9.3}{R_B}$$

Collector current for active region is given,

$$I_C = \beta I_B = \beta \times \frac{9.3}{R_B} \qquad \text{.....(i)}$$

From collector circuit,

$$I_C = \frac{10 - V_C}{R_C} \qquad \text{.....(ii)}$$

For active region collector current does not change with change in R_C rather it is determined by equation (i).

Therefore, I_C remains unchanged when R_C is replaced by R'_C

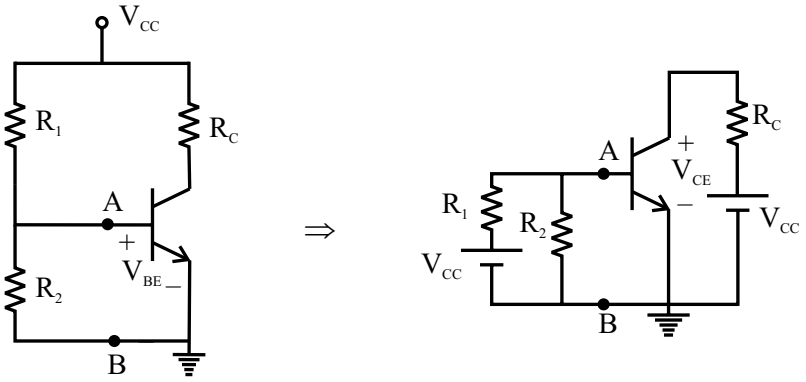
$$\therefore \quad \frac{10-2}{R_C} = \frac{10-4}{R'_C}$$

$$\Rightarrow \quad \frac{R'_C}{R_C} = \frac{10-4}{10-2} = \frac{6}{8} = \frac{3}{4}$$

$$\Rightarrow \quad \frac{R'_C}{R_C} = 0.75$$

2.3.2 Fixed Bias with Potential Divider

The base circuit of potential divider fixed bias circuit is biased using a potential divider circuit consisting of resistances R_1 & R_2 and collector circuit is biased through resistor R_C from a single source of supply as shown in Fig. 6 (a). The circuit can be redrawn by separating base and collector circuits as shown in Fig. 6 (b).



(a) Potential divider bias circuit (b) Equivalent circuit of potential divider bias

Fig.6 Potential divider fixed bias circuit of CE configuration of BJT

The potential divider circuit to the left of terminals A & B of above figure can be replaced by its Thevenin's equivalent as shown below,

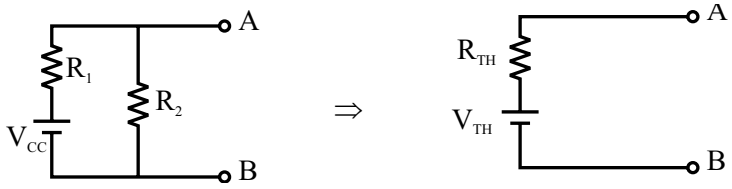


Fig.7 Potential divider circuit and its Thevenin's equivalent circuit.

The Thevenin's equivalent resistance seen across the terminals A & B is resistance seen across the terminals A &B by replacing the voltage source by short circuit. If voltage source V_{CC} is replaced by short circuit then resistance seen across A & B is parallel combination of R_1 and R_2.

$$\therefore \quad R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{14}$$

The Thevenin's voltage is open circuited voltage seen across the terminals A & B. It is voltage drop across resistance R_2 under open circuited condition.

$$\therefore \quad V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{15}$$

The circuit can be redrawn by replacing the potential divider by its Thevenin's equivalent circuit as shown in Fig.8

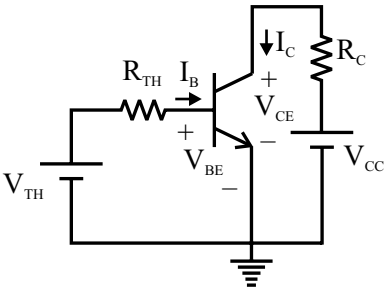


Fig.8 Potential divider fixed bias circuit of CE configuration of BJT with potential bias replaced by its Thevenin's equivalent circuit.

It is observed from circuit of Fig.8 that the biasing becomes similar to that of equivalent circuit of fixed base bias. Therefore, the method of analysis now becomes similar to analysis of Fixed bias circuit as under,

Applying KVL in the base circuit, we have,

$$V_{TH} - I_B R_{TH} - V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{TH} - V_{BE}}{R_{TH}} \tag{16}$$

Let BJT operates in active region, then

$$I_C = \beta I_B \tag{17}$$

Applying KVL in the collector circuit, we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_C \tag{18}$$

$$\Rightarrow \quad V_{CE} = V_{CC} - \beta I_B R_C \tag{19}$$

i. If $V_{CE} > V_{CE,\,sat}$ then BJT operates in active region with V_{CEQ} given by equation (19) and I_{CQ} given by equation (17).

ii. If $V_{CE} < V_{CE,\,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,\,sat}$ and I_{CQ} is obtained using equation (18) by replacing $V_{CE} = V_{CE,\,sat}$ as under,

$$I_{CQ} = \frac{V_{CC} - V_{CE,sat}}{R_C} \quad (20)$$

6.3.3 Fixed Bias with Collector Feedback

The base circuit of collector feedback fixed bias circuit is biased connecting a feedback resistor R_B from collector terminal to base of the BJT and collector circuit is biased through resistor R_C from a single source of supply as shown in Fig. 9.

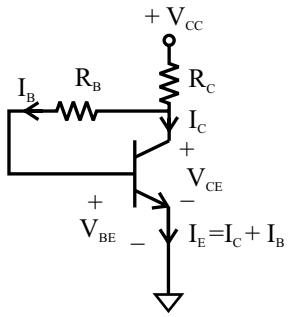


Fig.9 Collector feedback fixed bias circuit of CE configuration of BJT

From base circuit :-

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0 \quad (21)$$

Let BJT operates in active region,

$$I_C = \beta I_B \quad (22)$$

$$\Rightarrow \quad V_{CC} - [R_C(1 + \beta) + R_B] I_B - V_{BE} = 0 \quad (23)$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C[1+\beta]} \quad (24)$$

From Collector circuit :

$$V_{CC} - R_C (I_B + I_C) - V_{CE} = 0 \quad (25)$$

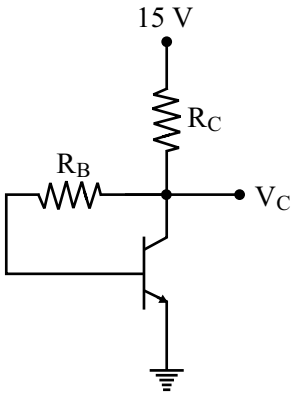
$$\Rightarrow \quad V_{CE} = V_{CC} - (1 + \beta) R_C I_B \quad (26)$$

i. If $V_{CE} > V_{CE,\,sat}$ then BJT operates in active region with V_{CEQ} given by equation (26) and I_{CQ} given by equation (22).

ii. If $V_{CE} < V_{CE,\,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,\,sat}$ and I_{CQ} is obtained using equations (21) and (25) by replacing $V_{CE} = V_{CE,\,sat}$ in equation (25)

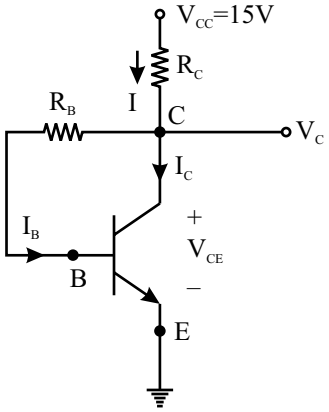
Example 8

In the given circuit, the silicon transistor has $\beta = 75$ and a collector voltage $V_C = 9V$. Then the ratio of R_B and R_C is .....



GATE(EE-I/2015/1M)

Solution : *Ans. 100 to 110*



Given, $\beta = 75, V_C = 9V$

Voltage, $V_{CE} = V_C - 0 = V_C = 9V$

Current through R_C

$$I = I_B + I_C = (1 + \beta)\, I_B$$

$$\Rightarrow \quad I = (1 + 75)\, I_B = 76\, I_B \qquad \text{....(i)}$$

Also, $$I = \frac{V_{CC} - V_C}{R_C} = \frac{15 - 9}{R_C} = \frac{6}{R_C}. \qquad \text{...(ii)}$$

Base current, $$I_B = \frac{V_C - V_{BE}}{R_B}$$

For active region, $V_{BE} = 0.7V$

$$\Rightarrow \quad I_B = \frac{9 - 0.7}{R_B} = \frac{8.3}{R_B} \qquad \text{.....(iii)}$$

From (i), (ii) and (iii), we have,

$$\frac{6}{R_C} = 76 \times \frac{8.3}{R_B}$$

$$\Rightarrow \quad \frac{R_B}{R_C} = \frac{76 \times 8.3}{6} = 105.13$$

2.4 Self Bias Circuits

A self bias circuit consists of a resistance R_E connected in series with emitter terminal of the BJT. The purpose of the resistor R_E is bias stabilization of operating point or Q-point of BJT against variations β, I_{CO} and V_{BE} with temperature.

2.4.1 Base Bias with Emitter Register

A biasing circuit with emitter resistance connected in emitter circuit of a common emitter configuration of BJT is shown in Fig. 10.

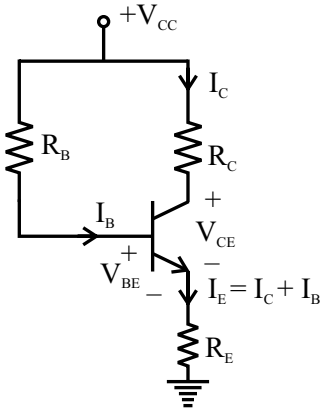


Fig.10 Self bias with emitter bias resistance in CE configuration of BJT

Applying KVL in the base circuit, we have,

$$V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0 \qquad (27)$$

Let BJT operates in active region,

$$I_C = \beta I_B \qquad (28)$$

$$\Rightarrow \quad V_{CC} - I_B R_B - V_{BE} - (\beta I_B + I_B) R_E = 0 \qquad (29)$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E} \qquad (30)$$

Applying KVL in the collector cicuit, we have,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0 \qquad (31)$$

$$\Rightarrow \quad V_{CC} - \beta I_B R_C - V_{CE} - (I + \beta) I_B R_C = 0 \qquad (32)$$

$$\Rightarrow \quad V_{CE} = V_{CC} - [\beta R_C + (1 + \beta) R_E] I_B \qquad (33)$$

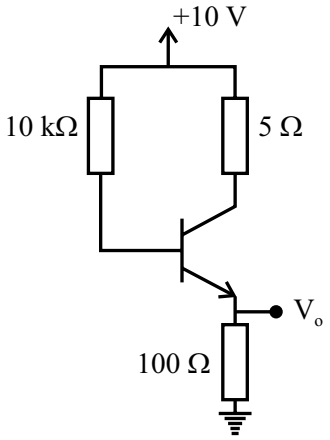
i. If $V_{CE} > V_{CE,\,sat}$ then BJT operates in active region with V_{CEQ} given by equation (33) and I_{CQ} given

by equation (28).

ii. If $V_{CE} < V_{CE, sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE, sat}$ and I_{CQ} is obtained using equations (27) and (31) by replacing $V_{CE} = V_{CE, sat}$ in equation (31).

Example 9

The transistor circuit shown uses a silicon transistor with $V_{BE} = 0.7$ V, $I_C \approx I_E$ and a dc current gain of 100. The value of V_0 is

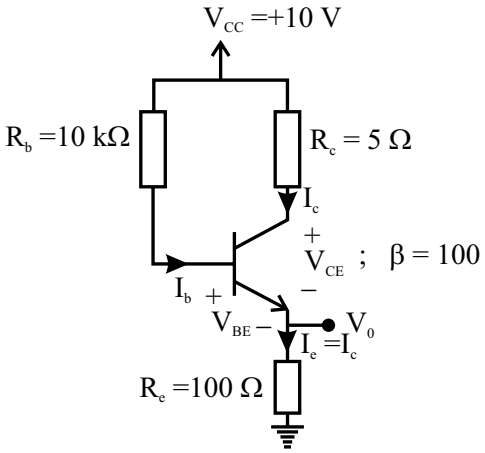


(a) 4.65 V (b) 5 V

(c) 6.3 V (d) 7.23 V

GATE(EE/2010/2 M)

Solution : Ans.(a)



Applying KVL in base circuit,

$$V_{CC} - R_b I_b - V_{BE} - R_e I_e = 0$$

$$\Rightarrow \quad 10 - 10 \times 10^3 I_b - 0.7 - I_e \times 100 = 0$$

Let BJT is operating in active region.

Then, collector current, $I_c = I_e = \beta I_b = 100 I_b$

$$\Rightarrow \quad 10 - 10 \times 10^3 I_b - 0.7 - 100 I_e = 0$$

$$\Rightarrow \quad 10 - 10 \times 10^3 I_b - 0.7 - 100 \times 100 I_b = 0$$

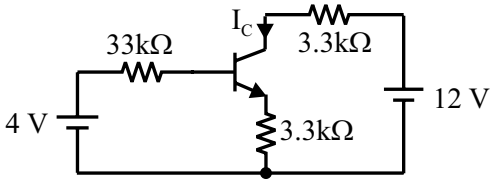
$$\Rightarrow \qquad I_b = \frac{9.3}{20}\ \text{mA} = 0.462\ \text{mA}$$

Emitter current, $$I_e \approx I_c = 100 I_b = 100 \times \frac{9.3}{20}\ \text{mA}$$

Output voltage, $$V_o = 100 \times 100 \times \frac{9.3}{20} \times 10^{-3}\ \text{V} = 4.65\ \text{V}$$

Example 10

In the circuit of figure, assume that the transistor has $h_{FE} = 99$ and $V_{BE} = 0.7$ V. The value of collector current I_C of the transistor is approximately

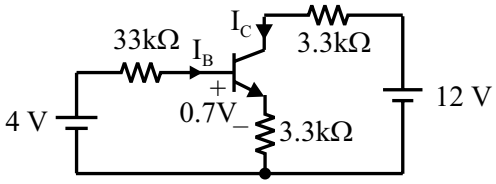


(a) [3.3/3.3] mA (b) [3.3/(3.3 +0.33)] mA

(c) [3.3/33] mA (d) [3.3/(33+3.3)] mA

GATE(EE/2003/1 M)

Solution : Ans.(b)



Given, $$h_{FE} = 99,\ V_{BE} = 0.7\ \text{V}$$

From the base circuit,

$$V_{BB} - I_B R_B - V_{BE} - (1+h_{FE}) I_B R_E = 0$$

$$\Rightarrow \qquad I_B = \frac{4 - 0.7}{33 + 100 \times 3.3} = \frac{3.3}{33 + 330}\ \text{mA}$$

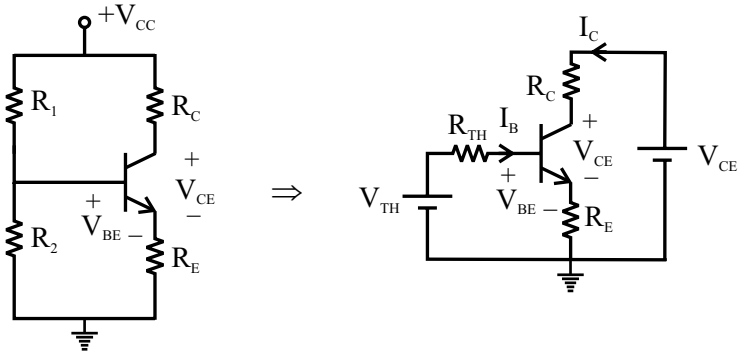
The collector current is given by,

$$I_C = h_{FE} I_B$$

$$\Rightarrow \qquad I_C = 99 \times \frac{3.3}{363}\ \text{mA} \approx \frac{3.3}{3.3 + 0.33}\ \text{mA}$$

2.4.2 Self Bias with Potential Divider

A self bias circuit with potential divider consists of a resistance connected in series with the emitter as shown in Fig.11



(a) Potential divider self bias circuit (b) Equivalent circuit of potential divider

Fig.11 Potential divider self biased circuit of BJT

When potential divider is replaced by its Thevenin's equivalent, the Thevenin's equivalent voltage and resistance of divider are given as,

$$V_{TH} = \frac{R_2}{R_1 + R_2} \cdot V_{CC} \tag{34}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{35}$$

Applying KVL in the base circuit, we have,

$$V_{TH} - I_B R_{TH} - V_{BE} - (I_B + I_C)\ ) R_E = 0 \tag{36}$$

Let BJT operates in active region,

$$I_C = \beta I_B \tag{37}$$

$$\Rightarrow V_{TH} - I_B R_{TH} - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$\Rightarrow V_{TH} - [R_{TH} + (1+\beta) R_E] I_B - V_{BE} = 0$$

$$\Rightarrow I_B = \frac{V_{TH} - V_{BE}}{(R_{TH} + (1+\beta)R_E)} \tag{38}$$

Apply KVL in collector circuit,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0 \tag{39}$$

$$\Rightarrow V_{CC} - V_{CE} - \beta I_B R_C - (1+\beta) I_B R_E = 0 \tag{40}$$

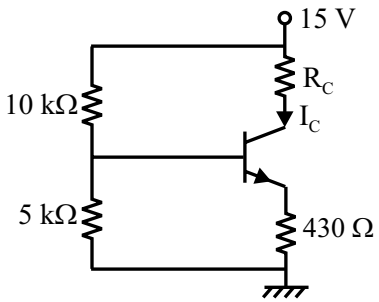
$$\Rightarrow V_{CE} = V_{CC} - [(1+\beta) R_E + \beta R_C] I_B = 0 \tag{41}$$

i. If $V_{CE} > V_{CE,\,sat}$ then BJT operates in active region with V_{CEQ} given by equation (41) and I_{CQ} given by equation (37).

ii. If $V_{CE} < V_{CE,\,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,\,sat}$ and I_{CQ} is obtained using equations (36) and (39) by replacing $V_{CE} = V_{CE,\,sat}$ in equation (39).

Example 11

In the circuit of figure shown below assume that the transistor is in active region. It has a large β and its base-emitter voltage is 0.7 V. The value of I_c is

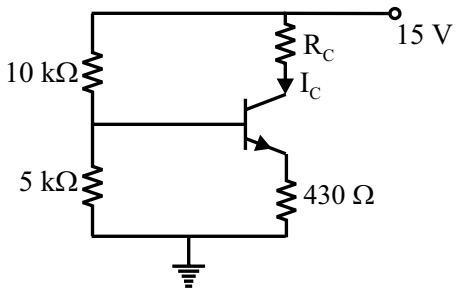


(a) Indeterminate since R_c is not given (b) 1 mA

(c) 5 mA (d) 10 mA

GATE(EC/2000/2M)

Solution : Ans.(d)



For large value of β, base current, $I_B = \frac{I_C}{\beta}$, is negligible. Then voltage at base of BJT is approximately same as Thevenin's equivalent voltage at the base. Thevenin's equivalent of voltage divider at the base of BJT,

$$V_{th} = \frac{5}{15} \times 15 = 5V = V_B$$

Voltage across emitter resistance,

$$V_E \approx V_B - V_{BE} = 5 - 0.7 = 4.3 \text{ V}$$

Collector current, $I_C = I_E - I_B$

For large of β , I_B can be neglected.

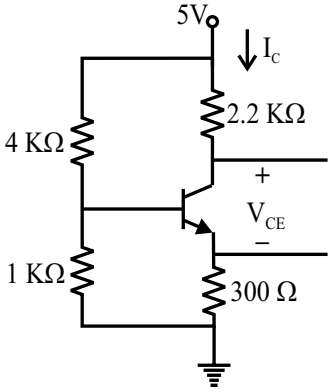
So, $$I_C \approx I_E = \frac{V_E}{R_E} = \frac{4.3}{430} = \frac{1}{100} = 10 \text{ mA}$$

***Note :** When β is large $I_C \approx I_E$. I_E can be calculated by finding out value of V_E across R_E.*

Example 12

Assuming that the β of the transistor is extremely large and V_{BE} = 0.7 V, I_C and V_{CE} in the circuit

shown in figure are



(a) $I_C = 1$ mA, $V_{CE} = 4.7$ V

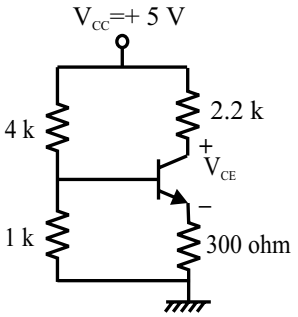
(b) $I_C = 0.5$ mA, $V_{CE} = 3.75$ V

(c) $I_C = 1$ mA, $V_{CE} = 2.5$ V

(d) $I_C = 0.5$ mA, $V_{CE} = 3.9$ V

GATE(EC/2004/2M)

Solution : Ans.(c)

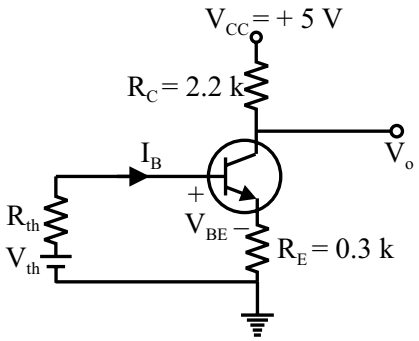


Thevenin's equivalent voltage at the base,

$$V_{th} = \frac{1}{5} \times 5 = 1V$$

Thevenin's equivalent resistance at the base,

$$R_{th} = \frac{1 \times 4}{1+4} = 0.8\, k\Omega$$



When β is large, the base current is small and drop across R_{th} is negligible.

In such case, voltage at emitter terminal,

$$V_E = V_{th} - V_{BE} = 1 - 0.7 = 0.3 \text{ V}$$

Then, emitter current, $I_E = V_E / R_E = 0.3/0.3 = 1 \text{ mA}$

Since base current is negligible, so,

$$I_C \approx I_E = 1 \text{ mA}$$

From the collector circuit, we have,

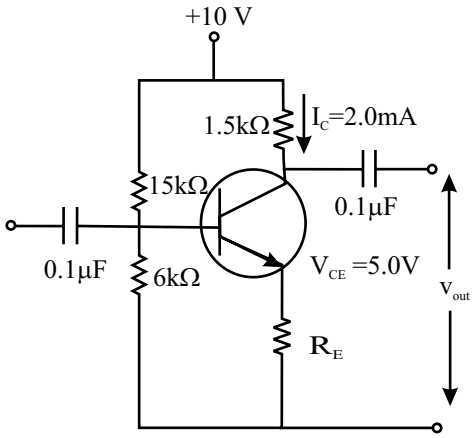
$$V_{CC} - I_C R_C - V_C = 0$$

$$\Rightarrow \quad V_C = V_{CC} - I_C R_C = 5 - 1 \times 2.2 = 2.8 \text{ V}$$

Then, $V_{CE} = V_C - V_E = 2.8 - 0.3 = 2.5 \text{ V}$

Example 13

In the transistor circuit as shown below, the value of resistance R_E in KΩ is approximately,

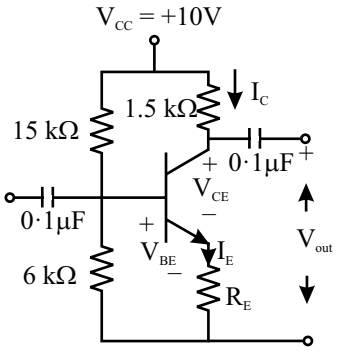


(a) 1.0 (b) 1.5

(c) 2.0 (d) 2.5

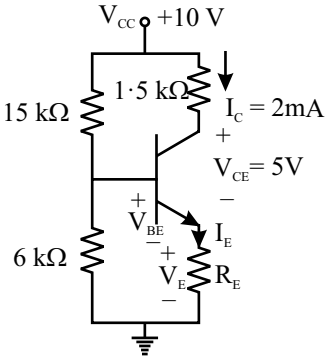
GATE(IN/2013/1M)

Solution : Ans.(a)



Given $I_c = 2 \text{ mA}, \ V_{CE} = 5.0\text{V}$

D.C. biasing circuit of BJT can be drawn as under,



Emitter current,

$$I_E = I_C + I_B = I_C + \frac{I_C}{\beta} \approx I_C$$

$$\therefore \quad I_E \approx 2\text{mA}$$

KVL in collector circuit,

$$10 - 1.5\times10^3\, I_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow\ 10 - 1.5\times10^3 \times 2 \times 10^{-3} - 5 - 2\times10^{-3} R_E = 0$$

$$\Rightarrow \quad R_E = \frac{10-8}{2\times10^{-3}} = 1\text{k}\Omega$$

2.4.3 Self Bias with Collector Feedback

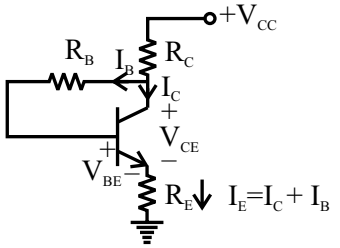


Fig.12 Potential divider self biased circuit of BJT

Apply KVL in the base circuit, we have,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0 \qquad (42)$$

Let BJT operates in active region,

$$I_C = \beta I_B \qquad (43)$$

$$\Rightarrow\ V_{CC} - (1 + \beta) I_B R_C - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0 \qquad (44)$$

$$\Rightarrow\ V_{CC} - [(1 + \beta)R_C + (1 + \beta)R_E + R_B]I_B - V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)} \qquad (45)$$

Applying KVL in the collector circuit, we have,

$$V_{CC} - (I_C + I_B)R_C - V_{CE} - (I_C + I_B)R_E = 0 \quad (46)$$

$$\Rightarrow V_{CC} - (1+\beta) I_B R_C - V_{CE} - (1 + \beta) I_B R_E = 0 \quad (47)$$

$$\Rightarrow V_{CE} = V_{CC} - (1 + \beta)(R_C + R_E) I_B \quad (48)$$

i. If $V_{CE} > V_{CE, sat}$ then BJT operates in active region with V_{CEQ} given by equation (48) and I_{CQ} given by equation (43).

ii. If $V_{CE} < V_{CE, sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE, sat}$ and I_{CQ} is obtained using equations (42) and (46) by replacing $V_{CE} = V_{CE, sat}$ in equation (46).

Note : *i. Potential divider self bias circuit is most preferred biasing circuit because it provide better stabilization among all circuits.*

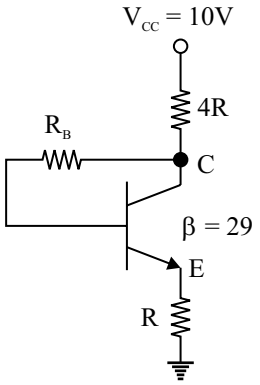
ii. Values of Junction voltage at 25°C for Si and Ge

	$V_{CE, sat}$	$V_{BE, sat}$	$V_{BE, active}$	$V_{BE,cut-in}$	$V_{BE, cut-off}$
Si	0.2	0.8	0.7	0.5	0
Ge	0.1	0.3	0.2	0.1	–0.1

iii. The value of Si is always more then value of Ge.

Example 14

For the circuit shown in the figure below, it is given that $V_{CE} = \frac{V_{CC}}{2}$. The transistor has $\beta = 29$ and $V_{BE} = 0.7V$ when the B-E junction is forward biased.



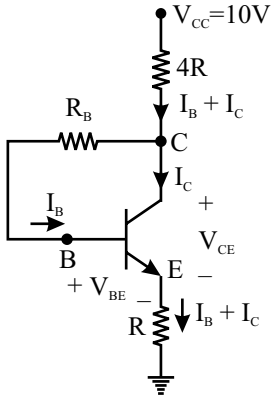
For this circuit, the value of $\frac{R_B}{R}$ is

(a) 43 (b) 92

(c) 121 (d) 129

GATE(EE-II/2017/2M)

Solution : Ans.(d)



Given, $V_{CE} = \frac{V_{CC}}{2}, V_{BE} = 0.7, \beta = 29$, V_{CC}=10 V

Applying KVL in the collector circuit gives,

$V_{CC} - 4R(I_B + I_C) - V_{CE} - R(I_B + I_C) = 0$

$$\Rightarrow \quad V_{CC} - \frac{V_{CC}}{2} = 5R(I_B + I_C)$$

$$\Rightarrow \quad \frac{V_{CC}}{2} = 5R(I_B + I_C)$$

Relation between I_C & I_B,

$$I_C = \beta I_B = 29 I_B$$

$$\Rightarrow \quad \frac{10}{2} = 5R(I_B + 29 I_B)$$

$$\Rightarrow \quad 30\, I_B R = 1$$

$$\Rightarrow \quad I_B = \frac{1}{30R} \qquad \text{.....(i)}$$

Applying KVL in base circuit gives,

$V_{CC} - 4R(I_B + I_C) - R_B I_B - V_{BE} - R(I_B + I_C) = 0$

$\Rightarrow$ $10 - 5R(I_B + 29\, I_B) - R_B I_B - 0.7 = 0$

$\Rightarrow$ $(150R + R_B)\, I_B = 9.3$

Putting expression of I_B from equation (i) in above equation, we have,

$$\Rightarrow \quad (150R + R_B) \times \frac{1}{30R} = 9.3$$

$$\Rightarrow \quad 5 + \frac{R_B}{30R} = 9.3$$

$$\Rightarrow \quad \frac{R_B}{R} = 30 \times 4.3 = 129$$

2.5. Miscellaneous Biasing Circuits

2.5.1 Bias Circuit with bias voltage at emitter

In this circuit a negative biasing voltage is applied at emitter terminal instead of a positive biasing voltage at the collector terminal. A bias circuit with negative bias voltage at emitter terminal is shown in Fig.13.

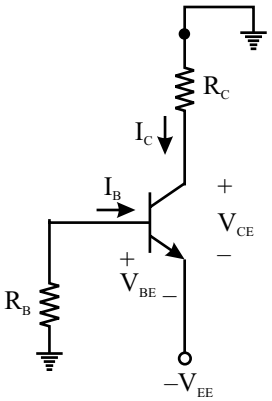


Fig.13 Bias Circuit with bais voltage at emitter

Applying KVL in base circuit, we have,

$$-R_B I_B - V_{BE} + V_{EE} = 0 \tag{49}$$

$$\Rightarrow \quad I_B = \frac{V_{EE} - V_{BE}}{R_B} \tag{50}$$

Let BJT operates in active region with

$$I_C = \beta I_B \tag{51}$$

Applying KVL in collector circuit, we have,

$$-I_C R_C - V_{CE} + V_{EE} = 0 \tag{52}$$

$$\Rightarrow \quad V_{CE} = V_{EE} - \beta I_B R_C \tag{53}$$

i. If $V_{CE} > V_{CE,sat}$ then BJT operates in active mode with V_{CEQ} given by equation (53) and I_{CQ} given by equation (51).

ii. If $V_{CE} < V_{CE,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,sat}$ and I_{CQ} is calculated using equation (52) by replacing V_{CE} by $V_{CE,sat}$.

2.5.2 Biasing of BJT with Two Power Supplies

A BJT can be biased using two power supplies with one connected on collector side and another on emitter side. The biasing of collector is done using positive voltage and biasing of emitter is done using negative voltage as shown in Fig.14

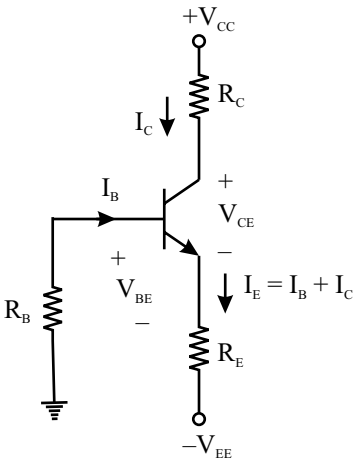


Fig.14 Biasing of BJT with two power supplies

Applying KVL in base circuit, we have,

$$-R_B I_B - V_{BE} - I_E R_E + V_{EE} = 0 \quad (54)$$

$$\Rightarrow -R_B I_B - V_{BE} - (I_B + I_C) R_E + V_{EE} = 0 \quad (55)$$

Let BJT operates in active region with

$$I_C = \beta I_B \quad (56)$$

$$\Rightarrow -R_B I_B - V_{BE} - (1 + \beta) I_B R_E + V_{EE} = 0$$

$$\Rightarrow I_B = \frac{V_{EE} - V_{BE}}{R_B + (1+\beta)R_E} \quad (57)$$

Applying KVL in collector circuit, we have,

$$V_{CC} - I_C R_C - V_{CE} - R_E (I_B + I_C) + V_{EE} = 0 \quad (58)$$

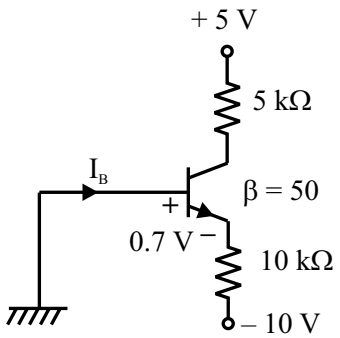
$$\Rightarrow V_{CE} = V_{CC} + V_{EE} - \beta I_B R_C - (1 + \beta) I_B R_E \quad (59)$$

i. If $V_{CE} > V_{CE,sat}$ then BJT operates in active mode with V_{CEQ} given by equation (59) and I_{CQ} given by equation (56).

ii. If $V_{CE} < V_{CE,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,sat}$ and I_{CQ} is calculated using equation (58) and (55) by replacing V_{CE} by $V_{CE,sat}$ in equation (58).

Example 15

In the circuit of figure, the value of the base current I_B will be

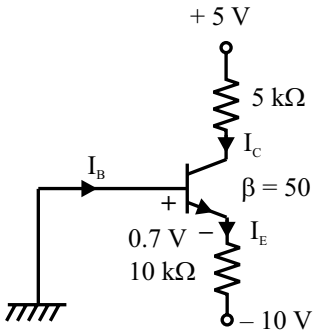


(a) 0.0 μA (b) 18.2 μA

(c) 26.7 μA (d) 40.0 μA

GATE(IN/2004/1M)

Solution : Ans.(b)



Given, $\beta = 50, V_{BE} = 0.7$ V.

Let BJT is operating in active mode with,

$$I_C = \beta I_B$$

Applying KVL in the base circuit,

$$-V_{BE} - (1+\beta) I_B R_E - V_{EE} = 0$$

$$\Rightarrow \quad -0.7 - (1+50) I_B \times 10k - (-10) = 0$$

$$\Rightarrow \quad I_B = \frac{10 - 0.7}{51 \times 10k} = 18.2\ \mu A$$

2.5.3 Biasing with Current Source

Biasing of BJT can be done with by connecting a constant current source in series with emitter as shown in Fig. 15.The biasing of BJT with current source helps in increasing input resistance at base without adversely affecting the bias stability. The emitter current is independent of β and R_B. The constant current source is implemented using a current mirror circuit which will be studied separately in later chapter on compound circuits.

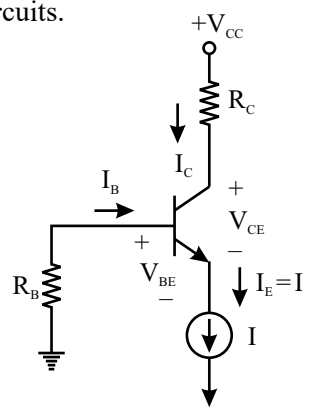


Fig.15 Biasing of BJT with current source

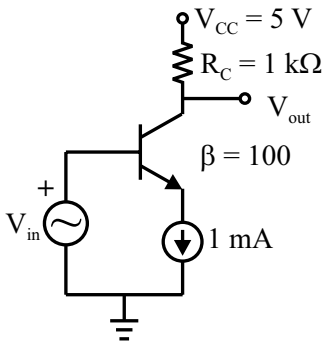
The emitter current of the BJT , $I_E = I$

Base current in terms of emitter current the BJT can be given as ,

$$I_B = \frac{I_E}{1+\beta} \quad (60)$$

Example 16

The common emitter amplifier shown in figure is biased using a 1 mA ideal current source. The approximate base current value is

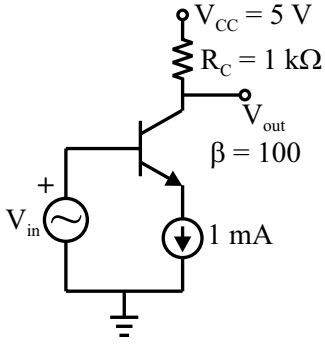


(a) 0 μA (b) 10 μA

(c) 100 μA (d) 1000 μA

GATE(EE/2005/2 M)

Solution : Ans.(b)



From above circuit,

$$I_E = 1 \text{ mA}$$

Relation between base current and emitter current,,

$$I_E = (1+\beta)I_B$$

$$\Rightarrow \quad I_B = \frac{1}{1+\beta}I_E = \frac{1}{1+100} \times 1 \text{ mA} \approx 10 \text{ μA}$$

2.5.4 Biasing of Emitter Follower or Common Collector Configuration

An emitter follower circuit has load resistance connected in series with emitter terminal. The output of the circuit is taken from the emitter terminal as shown in Fig. 16. The biasing voltage can be applied at emitter or collector terminals.

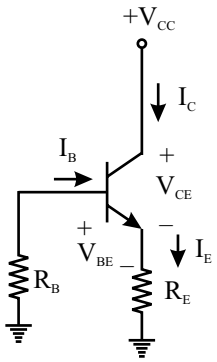


Fig.16 Biasing of emitter follower circuit of BJT

Applying KVL in the base circuit, we have,

$$-R_B I_B - V_{BE} - R_E I_E + V_{EE} = 0 \quad (61)$$

The emitter current of BJT is given in terms of base current and collector current is given as,

$$I_E = I_B + I_C \quad (62)$$

$$\Rightarrow -R_B I_B - V_{BE} - R_E (I_B + I_C) + V_{EE} = 0 \quad (63)$$

Let BJT operates in active region with,

$$I_C = \beta I_B \quad (64)$$

$$\Rightarrow -R_B I_B - V_{BE} - R_E (1 + \beta) I_B + V_{EE} = 0 \quad (65)$$

$$\Rightarrow I_B = \frac{V_{EE} - V_{BE}}{R_B + (1+\beta)R_E} \quad (66)$$

Applying KVL in collector circuit, we have,

$$-V_{CE} - I_E R_E + V_{EE} = 0 \quad (67)$$

$$\Rightarrow -V_{CE} - (I_C + I_B) R_C + V_{EE} = 0 \quad (68)$$

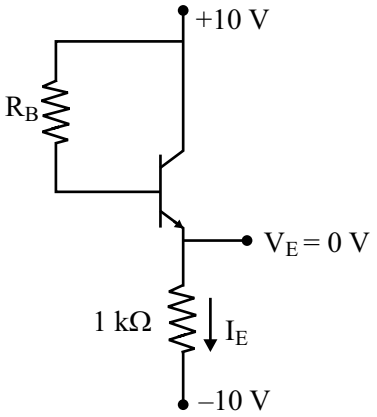
$$\Rightarrow V_{CE} = V_{EE} - (1 + \beta) I_B \quad (69)$$

i. If $V_{CE} > V_{CE,sat}$ then BJT operates in active mode with V_{CEQ} given by equation (69) and I_{CQ} given by equation (64).

ii. If $V_{CE} < V_{CE,sat}$ then BJT operates in saturation region with $V_{CEQ} = V_{CE,sat}$ and I_{CQ} is calculated using equation (68) and (63) by replacing V_{CE} by $V_{CE,sat}$ in equation (68).

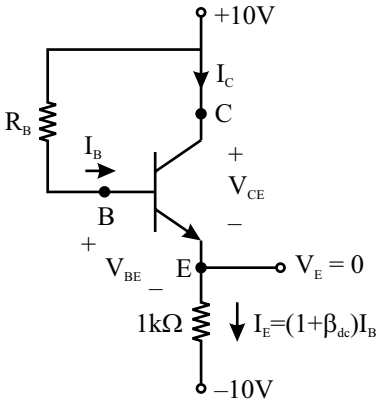
Example 17

In the circuit shown in the figure, it is found that V_{BE} = 0.7 V and V_E = 0 V. If β_{dc} = 99 for the transistor, then the value of R_B in kilo ohms is ..... kΩ.



GATE(IN/2015/2M)

Solution : Ans. 92 to 94



Given, $V_{BE} = 0.7V, V_E = 0, \beta_{dc} = 99$

Emitter current,

$$I_E = \frac{V_E - (-10)}{1k} = \frac{0+10}{1k} = 10 \text{ mA}$$

Emitter current in terms of base current is given by,

$$I_E = (1 + \beta_{dc})\, I_B$$

$$\Rightarrow \quad I_B = \frac{I_E}{1+\beta} = \frac{10}{1+99}\text{mA} = 0.1 \text{ mA}$$

Applying KVL in base circuit gives,

$$10 - I_B R_B - V_B = 0 \qquad \text{.....(i)}$$

$$V_{BE} = V_B - V_E$$

$$\Rightarrow \quad V_B = V_{BE} + V_E = 0.7 + 0 = 0.7V$$

Putting value as V_B & I_B in equation (i),

we have,

$$10 - 0.1 \times 10^{-3} R_B - 0.7 = 0$$

$$\Rightarrow \quad R_B = \frac{10-0.7}{0.1\times10^{-3}} = 93k\Omega$$

2.5.5 Biasing of PNP transistors

The biasing circuits of PNP transistors are similar to NPN transistors. The biasing voltage may be given to emitter or collector terminals. A self biased circuit of PNP transistor with bias voltage applied at collector junction is shown in Fig.17

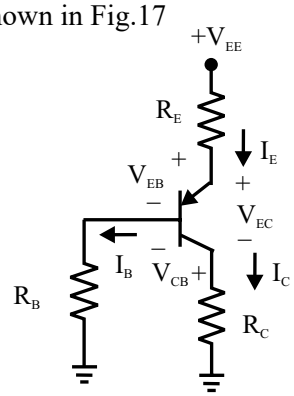


Fig.17 Biasing of self biased PNP transistor

Applying KVL in the base circuit, we have,

$$V_{EE} - R_E I_E - V_{EB} - R_B I_B = 0 \tag{70}$$

The emitter current of BJT is given in terms of base current and collector current is given as,

$$I_E = I_B + I_C \tag{71}$$

$$\Rightarrow V_{EE} - R_E(I_B + I_C) - V_{EB} - R_B I_B = 0 \tag{72}$$

Let BJT operates in active region with,

$$I_C = \beta I_B \tag{73}$$

$$\Rightarrow V_{EE} - (1+\beta)I_B R_E - V_{EB} - R_B I_B = 0 \tag{74}$$

$$\Rightarrow \quad I_B = \frac{V_{EE} - V_{EB}}{R_B + (1+\beta)R_E} \tag{75}$$

Applying KVL in collector circuit, we have,

$$V_{EE} - V_{EC} - I_E R_E - I_C R_C = 0$$

$$\Rightarrow V_{EE} - V_{EC} - (I_B + I_C)R_E - I_C R_C = 0 \tag{76}$$

$$\Rightarrow \quad V_{EC} = V_{EE} - (1+\beta)I_B R_E - \beta I_B R_C \tag{77}$$

Voltage across the collector junction,

$$V_{CB} = V_{EC} - V_{EB} \tag{78}$$

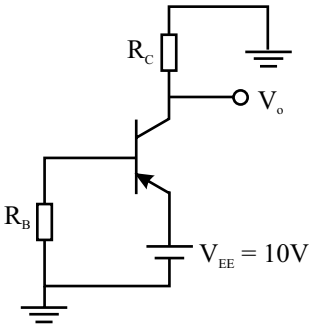
i. If $V_{CB} < 0$ then collector junction is reverse biased and BJT operates in active mode with V_{EQ} given by equation (77) and I_{CQ} given by equation (73).

ii. If $V_{CB} > 0$ then collector junction is forward biased and BJT operates in saturation region with $V_{ECQ} = V_{EC,sat}$ and I_{CQ} is calculated using equation (72) and (76) by replacing V_{EC} by $V_{EC,sat}$ in equation (76)

Note : *V_{BE} and V_{CE} are negative for PNP and positive for NPN transistors whereas V_{EB} and V_{EC} are positive for PNP and negative for NPN transistors*

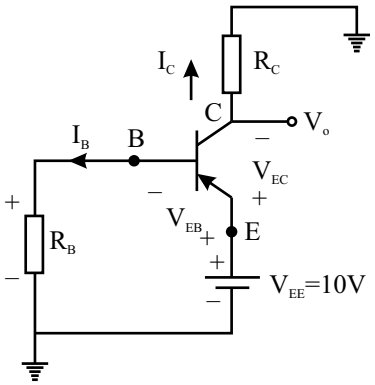
Example 18

In the circuit shown, the PNP transistor has $|V_{BE}| = 0.7$ V and $\beta = 50$.Assume that $R_B = 100$ kΩ. For V_o to be 5 V, the value of R_C (in kΩ) is_____



GATE(EC-III/2014/1M)

Solution : Ans : 1.04 to 1.12



Given, $|V_{BE}| = 0.7V, \beta = 50,$

$R_B = 100k\Omega, V_o = 5V$

$V_{EB} = 0.7V$

Applying KVL in base circuit, we have,

$$V_{EE} - V_{EB} - R_B I_B = 0$$

$$I_B = \frac{V_{EE} - V_{EB}}{R_B} = \frac{10 - 0.7}{100} mA = 93\ \mu A$$

Collector current, $I_C = \beta I_B = 50 \times 93\ \mu A = 4.65\ mA$

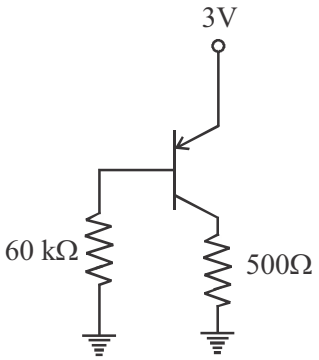
Output voltage,

$$V_o = I_C R_C$$

$$\Rightarrow \quad R_C = \frac{V_o}{I_C} = \frac{5}{4.65} k\Omega = 1.075\ k\Omega$$

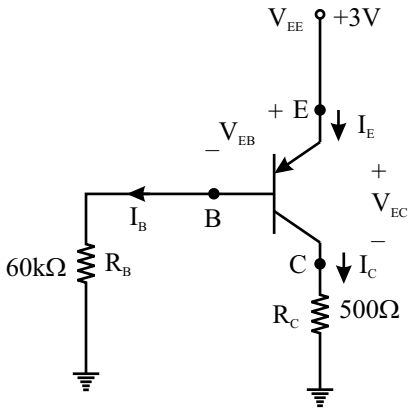
Example 19

In the circuit shown in the figure, the BJT has a current gain (β) of 50. For an emitter-base voltage V_{EB} = 600 mV, the emitter-collector voltage V_{EC} (in Volts) is .....



GATE(EC-III/2015/1M)

Solution : Ans. 2



Given, $\beta = 50, V_{EB} = 600\ mV = 0.6\ V$

Applying KVL in base to emitter circuit,

$$V_{EE} - V_{EB} - 60\ kI_B = 0$$

$$3 - 0.6 - 60\ kI_B = 0$$

$$I_B = \frac{2.4}{60k} = 40\ \mu A$$

For active region of amplifier,

$$I_C = \beta I_B = 50 \times 40 \times 10^{-6} = 2mA$$

Applying KVL in collector circuit,

$$V_{EE} - V_{EC} - 500\ I_C = 0$$

$$\Rightarrow \quad V_{EC} = 3 - 500 \times 2 \times 10^{-3} = 2\ V$$

2.5.6 BJT Biasing with Zener Diode

A Zener diode is sometimes connected between base terminal and ground to fix the voltage at base terminal of BJT as shown in Fig.18. This circuit can be used for voltage regulation if load is connected in emitter.

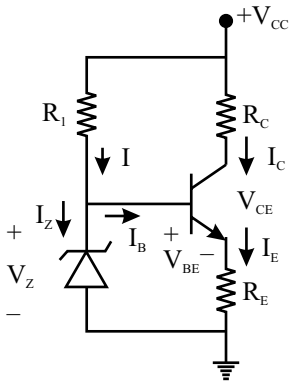


Fig.18 BJT biasing with Zener diode in base circuit

Applying KVL in base circuit,

$$V_Z - V_{BE} - I_E R_E = 0$$

$$\Rightarrow \quad I_E = \frac{V_Z - V_{BE}}{R_E} \tag{79}$$

Base current, $$I_B = \frac{I_E}{1+\beta} \tag{80}$$

Current in R_1, $$I = \frac{V_{CC} - V_Z}{R_1} \tag{81}$$

Current through Zener diode,

$$I_Z = I - I_B \tag{82}$$

Collector current, $$I_C = \beta I_B \tag{83}$$

Applying KVL in collector circuit,

$$V_{cc} - I_C R_C - V_{CE} - I_E R_E = 0$$

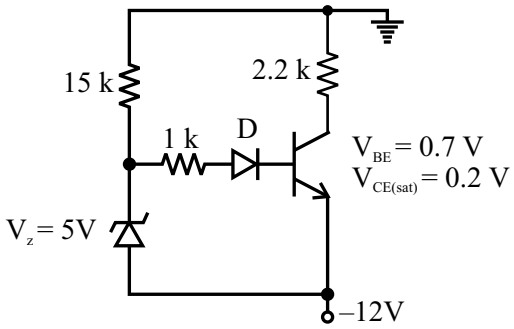
$$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E \tag{84}$$

Equation (83) and (84) give the operating point of BJT.

Example 20

The transistor used in the circuit shown below has a β of 30 and I_{CBO} is negligible.

If the forward voltage drop of diode is 0.7 V, then the current through collector will be

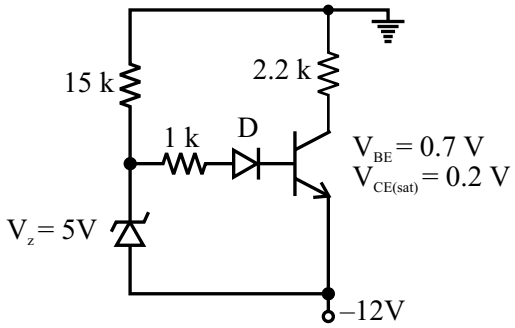


(a) 168 mA (b) 108 mA

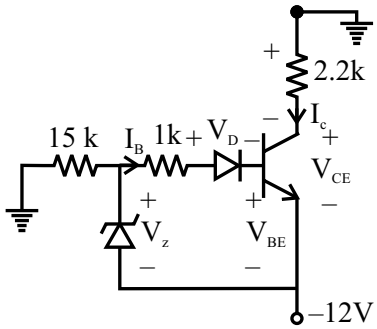
(c) 20.54 mA (d) 5.36 mA

GATE(EE/2011/2 M)

Solution : Ans.(d)



Above circuit can be redrawn as,



Given, $V_z = 5V$, $V_D = 0.7$ V, $V_{BE} = 0.7$ V, $V_{CE(sat)} = 0.2$ V, $\beta = 30$, I_{CBO} = negligible

KVL in base circuit,

$$V_z - I_B \times 1k - V_D - V_{BE} = 0$$

$$I_B = \frac{5-1.4}{1} mA = 3.6 \text{ mA} \quad ...(i)$$

Let, BJT is operating in active region,

then, $I_C = \beta I_B = 30 \times 3.6 \text{ mA} = 108 \text{ mA}$

Applying KVL in collector circuit, we have,

$$-I_C \times 2.2\text{ k} - V_{CE} + 12 = 0 \qquad \text{....(ii)}$$

$$\Rightarrow \qquad V_{CE} = 12 - 108 \times 2.2 = -225.6\text{ V}$$

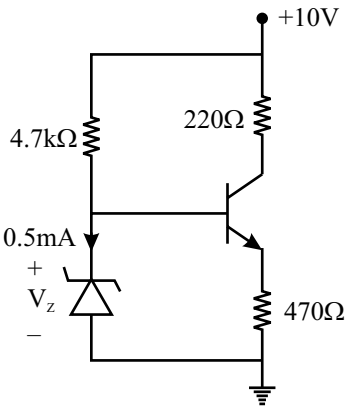
As V_{CE} is coming out to be negative so BJT must be operating in saturation region with $V_{CE} = V_{CE(sat)}$.

Taking $V_{CE} = V_{CE(sat)}$, we have

$$I_C = \frac{12 - V_{CE(sat)}}{2.2}\text{mA} = \frac{12 - 0.2}{2.2}\text{mA} = 5.36\text{ mA}$$

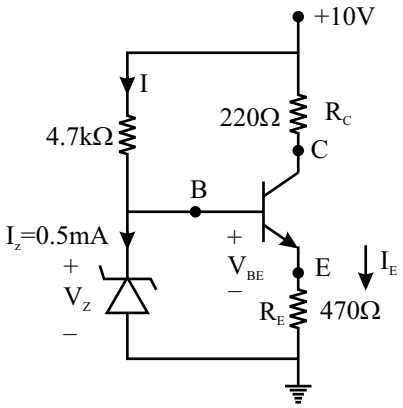
Example 21

A transistor circuit is given below. The Zener diode breakdown voltage is 5.3 V as shown. Take base to emitter voltage drop to be 0.6 V. The value of the current gain β is.....



GATE(EE-I/2016/1M)

Solution : ***Ans. 18.0:20.0***



Given, $V_Z = 5.3$ V, $V_{BE} = 0.6$V

Applying KVL in base circuit,

$$V_Z - V_{BE} - R_E I_E = 0$$

$$\Rightarrow \quad 5.3 - 0.6 - 470 \times I_E = 0$$

$$\Rightarrow \quad I_E = \frac{4.7}{470} = 0.01A = 10\ mA$$

Current in 4.7 kΩ resistance,

$$I = \frac{10 - V_Z}{4.7k} = \frac{10 - 5.3}{4.7k} = 1\ mA$$

Base current, $I_B = I - I_Z = 1 - 0.5 = 0.5\ mA$

Relation between base current and emitter current is given by,

$$I_E = (1 + \beta)I_B$$

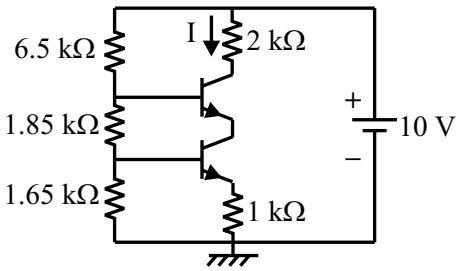
$$\Rightarrow \quad 10 \times 10^{-3} = (1 + \beta) \times 0.5 \times 10^{-3}$$

$$\Rightarrow \quad \beta = 19$$

2.5.7. Examples on Biasing of Composite Circuits

Example 22

If the transistors in figure, have high values of β and a V_{BE} of 0.65 volt, the current I, flowing through the 2 kilo ohms resistance will be....

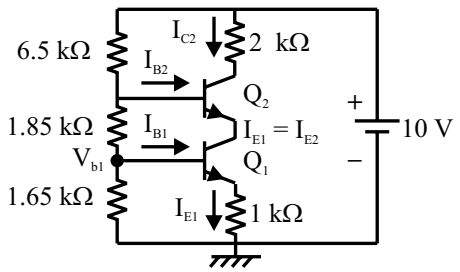


(a) 1 mA (b) 2 mA

(c) 3 mA (d) 4 mA

GATE(EC/1992/2M)

Solution : Ans.(a)



Given, $V_{BE} = 0.65$ V

For large value of β, $I_{B1} = \frac{I_{C1}}{\beta}$ and $I_{B2} = \frac{I_{C2}}{\beta}$ are negligible.

$\therefore \quad I_{E1} = I_{C1} = I_{E2} = I_{C2} = I$

Approximate voltage at base of transistor Q1,

$$V_{b1} = \frac{1.65}{1.65 + 1.85 + 6.5} \times 10 = 1.65 \text{ V}$$

Voltage across emitter resistance of Q_1,

$$V_E = V_{b1} - V_{BE} = 1.65 - 0.65 = 1 \text{ V}$$

Then, emitter current of Q_1,

$$I_{E1} = \frac{V_E}{R_E} = \frac{1}{1} = 1 \text{ mA}$$

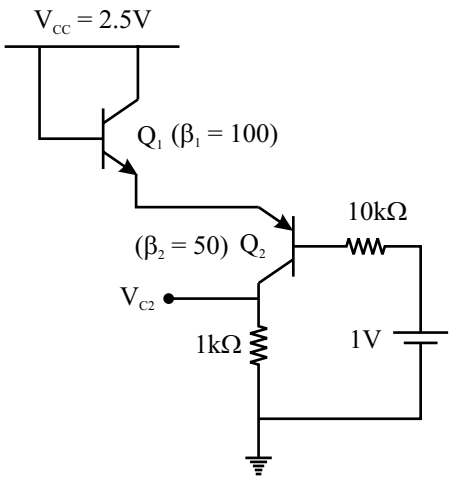
Since β of transistors is large therefore,

$$I = I_{E2} = I_{C1} = I_{E1} = 1 \text{ mA}$$

Note : *When β is large $I_C \approx I_E$. I_E can be calculated by finding out value of V_E across R_E.*

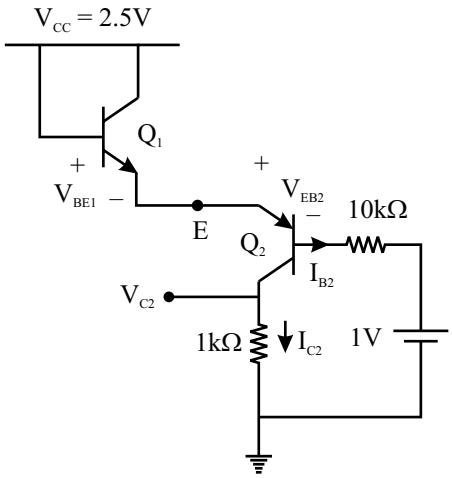
Example 23

Consider the circuit shown in the figure. Assuming $V_{BE1} = V_{EB2} = 0.7$ volt, the value of the dc voltage V_{C2} (in volt) is .....



GATE(EC-III/2016 /1 M)

Solution : *Ans. 0.45:0.55*



Given, $V_{BE1} = V_{EB2} = 0.7V,\ \beta_2 = 50,\ \beta_1 = 100$

Voltage at terminal E,

$$V_E = V_{CC} - V_{BE1} = 2.5 - 0.7 = 1.8\ V$$

From base circuit of transistor Q_2

$$V_E - V_{EB2} - 10K \times I_{B2} - 1 = 0$$

$$\Rightarrow\ 1.8 - 0.7 - 10k\ I_{B2} - 1 = 0$$

$$\Rightarrow\ I_{B2} = \frac{0.1}{10}mA = 10\ \mu A$$

Collector current of transistor Q_2

$$I_{C2} = \beta_2 I_{B2} = 50 \times 10 \times 10^{-6} = 0.5\ mA$$

$$\therefore\ \text{Voltage, } V_{C2} = 1k \times I_{C2}$$

$$\Rightarrow\ V_{C2} = 1 \times 10^3 \times 0.5 \times 10^{-3} = 0.5V$$

2.6 Bias Stability and Stability Factors

The collector current of BJT is given by,

$$I_C = \beta I_B + (1+\beta) I_{CO} (1 - e^{-\frac{V_{CB}}{\eta V_T}}) \qquad (85)$$

where, $V_{CB} = V_{CE} - V_{BE}$

When temperature of the transistor increases, β and I_{CO} increases and V_{BE} reduces. Due to change in these factors, the collector current also increases and hence Q-point shifts toward saturation region which may drive the BJT to saturation.

As collector current increases due to increase in temperature more heat is generated at collector junction, which results further increase in temperature and increase in temperature again results increase in β and I_{CO} and decrease in V_{BE}, which in turn results in further increase in I_C and the process becomes 'cumulative' finally resulting into either pushing the transistor operation to saturation or resulting into **thermal breakdown** or **thermal runaway or secondary breakdown** of the BJT.

The bias stability of BJT can be improved by using following techniques,

i) Use of self-bias circuit.

ii) Temperature compensation by using non linear temperature sensitive devices.

Stability Factors :

1. Stability factor with respect to V_{BE}
   The stability factor with respect to V_{BE} is defined as rate of change of collector current per with change in voltage V_{BE}. Mathematically it can be given as,

$$S_{V_{BE}} = \frac{\partial I_C}{\partial V_{BE}}$$

2. Stability Factor with respect to I_{CO}
   The stability factor with respect to I_{CO} is defined as rate of change of collector current per with change in voltage I_{CO}. Mathematically it can be given as,

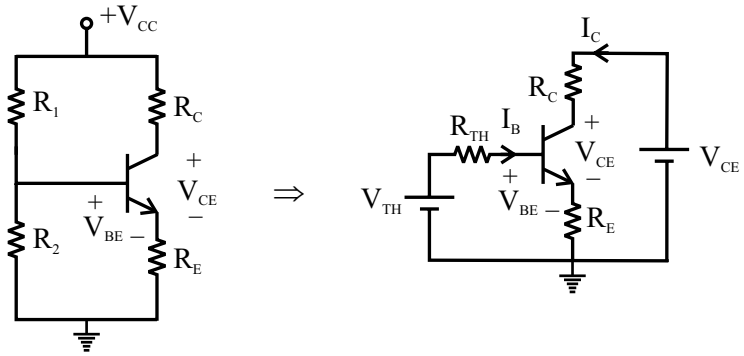
$$S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}}$$

3. Stability factor with respect to β.
   The stability factor with respect to β is defined as rate of change of collector current per with change in voltage β. Mathematically it can be given as,

$$S_{\beta} = \frac{\partial I_C}{\partial \beta}$$

2.6.1 Stability factors of potential divider self bias circuit

Consider a potential divider bias circuit as shown in Fig.19(a). The potential divider can be replaced by its Thevenin's equivalent as shown in Fig. 19(b).



(a) Potential divider self bias circuit (b) Equivalent circuit of potential divider

Fig.19 Potential divider self biased circuit of BJT

Applying KVL in the base circuit,

$$V_{TH} = R_{TH}I_B + V_{BE} + R_E(I_C + I_B)$$

$$V_{BE} = V_{TH} - R_{TH}I_B - R_E(I_C + I_B) \quad (86)$$

The collector current of BJT is given by,

$$I_C = \beta I_B + (1+\beta)\, I_{CO} \tag{87}$$

$$\Rightarrow \quad I_B = \frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{CO} \tag{88}$$

From equation (86) and (88), we have,

$$V_{BE} = V_{TH} - R_{TH}\left[\frac{I_C}{\beta} - \left(\frac{1+\beta}{\beta}\right) I_{CO}\right] - R_E\left[I_C + \frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{CO}\right]$$

$$V_{BE} = V_{TH} + (R_{TH} + R_E)\left(\frac{1+\beta}{\beta}\right) I_{CO} - \left[\frac{R_{TH}}{\beta} + \frac{R_E\,(1+\beta)}{\beta}\right] I_C \tag{89}$$

1. Stability Factor with respect to V_{BE}

The expression of stability factor w.r.t. V_{BE} can be obtained by assuming I_{CO} and β as constants and V_{BE} as variable.

Differentiate equation (89) w.r.t V_{BE}, we have,

$$\Rightarrow \quad 1 = -\frac{R_{TH} + (1+\beta)\, R_E}{\beta} \cdot \frac{\partial I_C}{\partial V_{BE}} \tag{90}$$

$$\Rightarrow \quad S_{V_{BE}} = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_{TH} + (1+\beta)\, R_E} \tag{91}$$

Assuming large β, we can approximate above expression as under,

$$\Rightarrow \quad S_{V_{BE}} \approx \frac{-\beta}{(1+\beta)\, R_E} \approx \frac{-\beta}{\beta R_E} \approx \frac{-1}{R_E} \tag{92}$$

$$\Rightarrow \quad S_{V_{BE}} \approx -\frac{1}{R_E} \tag{93}$$

Here, negative sign indicates that I_C decreases with increasing V_{BE} and vice versa. It is observed from above equation that $S_{V_{BE}}$ decreases with increase in R_E. In other other words the variation in I_C w.r.t.

V_{BE} decreases with increase in emitter resistance R_E.

Fractional change in I_C w.r.t. fraction change in V_{BE} can be derived using equation (89) as under,

$$\% \text{ Variation} = \frac{\partial I_C}{I_C} = -\frac{\partial V_{BE}}{I_C\, R_E} \tag{94}$$

$$\text{or} \quad \frac{\Delta I_C}{I_C} = \frac{-\Delta V_{BE}}{I_C\, R_E} \tag{95}$$

Note : *Variation in I_C with respect to V_{BE} is inversely proportional to drop across R_E.*

2. Stability Factor with respect to I_{CO}

The expression of stability factor w.r.t. I_{CO} can be obtained by assuming V_{BE} and β as constants and I_{CO} as variable.

Differentiate equation (89) w.r.t I_{CO}, we have,

$$\Rightarrow \quad 0 = 0 + (R_E + R_{TH})\left(\frac{1+\beta}{\beta}\right) - \frac{R_{TH} + (1+\beta)R_E}{\beta}\cdot\frac{\partial I_C}{\partial I_{CO}}$$

$$\Rightarrow \quad S_{I_{CO}} = \frac{\partial I_C}{\partial I_{CO}} = \frac{(R_E + R_{TH})(1+\beta)}{R_{TH} + (1+\beta)R_E} \tag{96}$$

$$S_{I_{CO}} = \frac{R_E + R_{TH}}{R_E + \left(\frac{R_{TH}}{1+\beta}\right)} \tag{97}$$

Assuming large β, we can approximate above expression as under,

$$S_{I_{CO}} \approx \frac{R_E + R_{TH}}{R_E} = 1 + \frac{R_{TH}}{R_E} \tag{98}$$

It is observed from above equation that $S_{I_{CO}}$ decreases with increase in R_E. In other words the variation in I_C w.r.t. I_{CO} decreases with increase in emitter resistance R_E.

Fractional change in I_C w.r.to. fraction change in I_{CO} can be derived using equation (89) as under,

$$\frac{\Delta I_C}{\Delta I_{CO}} = 1 + \frac{R_{TH}}{R_E} \tag{99}$$

$$\Rightarrow \quad \Delta I_C = \left(1 + \frac{R_{TH}}{R_E}\right)\Delta I_{CO}$$

$$\Rightarrow \quad \frac{\Delta I_C}{I_C} = \left(1 + \frac{R_{TH}}{R_E}\right)\frac{\Delta I_{CO}}{I_C} \tag{100}$$

$$\frac{\Delta I_C}{I_C} = \frac{\Delta I_{CO}}{I_C} + \Delta I_{CO}\cdot\frac{R_{TH}}{I_C R_E} \tag{101}$$

Drop across R_E results in reduction of percentage variation in I_C.

3. Stability factor with respect to β

Stability factor with respect to β is given by

$$S_\beta = \frac{\partial I_C}{\partial \beta} = \frac{I_C S}{\beta(1+\beta)} \tag{102}$$

It is observed from above equation that change of I_C w.r.t. β is small when β is large. So, the effect of temperature on transistor with higher β is less as compared to transistor with smaller 'β'.

Note : *For practical consideration, Ge transistor is stable for temperature upto '75°C' and Si transistor is stable upto'175°C'.*

2.7 Bias Compensation

Bias compensation is used to compensate the variation in I_C with variation in temperature. Bias compensation is achieved by using temperature sensitive devices such as diodes, thermistors and sensitors.

2.7.1 Bias Compensation for V_{BE}

Bias compensation against the variation in I_C due to variation in V_{BE} with temperature can be achieved by connecting a diode in the emitter circuit as shown in Fig.20. It is essential to have material of diode same as that of BJT to achieve the compensation.

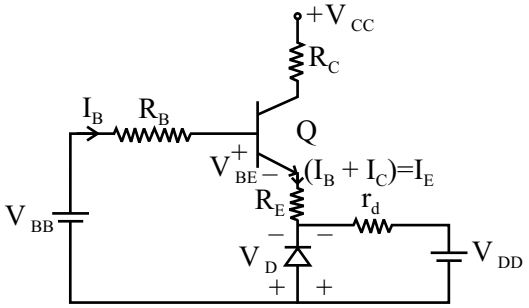


Fig.20 Circuit for bias compensation for V_{BE}

If BJT and diode are made of same material then the variation in base to emitter voltage of BJT and diode voltage is same.

$$\therefore \quad \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_D}{\partial T} = -2.5 \text{ mV/T} \tag{103}$$

Applying KVL in the base circuit, we have,

$$V_{BB} = I_B R_B + (V_{BE} - V_D) + (I_C + I_B) R_E \tag{104}$$

But ,

$$I_B = \frac{I_C}{\beta} - \frac{(1+\beta) I_{CO}}{\beta} \tag{105}$$

Putting I_B in equation (104), we have,

$$I_C = \frac{\beta[V_{BB} - (V_{BE} - V_D)] + (R_B + R_E)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E} \tag{106}$$

$$\text{If} \quad \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_D}{\partial T} \text{ then } \frac{\partial (V_{BE} - V_D)}{\partial T} = 0 \tag{107}$$

It is observed from equation (106) that the variation in I_C is function of variation in $V_{BE} - V_D$ with temperature. Since, variation in $(V_{BE} - V_D)$ with respect to temperature is zero, therefore, variation in

I_C w.r.t. variation in V_{BE} due to change in temperature will be zero.

2.7.2 Bias Compensation for I_{CO}

Bias compensation against the variation in I_C due to variation in I_{CO} with temperature can be achieved by connecting a diode between base terminal and ground as shown in Fig.21. It is essential to have material of diode same as that of BJT to achieve the compensation.

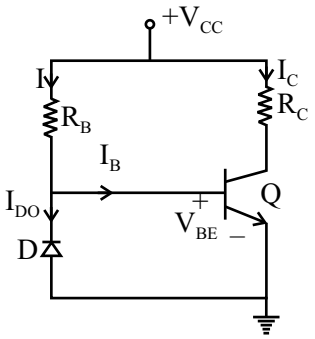


Fig.21 Circuit for bias compensation for V_{BE}

The diode in the above circuit is reverse biased. The current through a reverse biased pn diode is reverse saturation current. If I_{DO} is reverse saturation current then current I in resistance R_b can be given as,

$$I = I_B + I_{DO} \tag{108}$$

The applying KVL in the base circuit, we have,

So, $$I = \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC}}{R_B} \tag{109}$$

Base current, $$I_B = I - I_{DO} \tag{110}$$

Collector current, $$I_C = \beta I_B + (1 + \beta) I_{CO} \tag{111}$$

$\Rightarrow$ $$I_C = \beta(I - I_{DO}) + (1 + \beta) I_{CO} \tag{112}$$

$\Rightarrow$ $$I_C = \beta I + I_{CO} + \beta(I_{CO} - I_{DO}) \tag{113}$$

The reverse saturation current I_{CO} is of order of mA for G_E and nA for Si. Here, term $\beta(I_{CO} - I_{DO})$ major effect on I_C. The variation in I_{CO} with temperature is compensated by variation in I_{DO}, therefore, over all variation in I_{CO} due to temperature is compensated and I_C almost remains constant with variation in temperature.

Note : *i. The current I_{CO} is of order of μA for Ge and of order of nA for Si. Therefore, compensation for I_{CO} is used in Ge transistor, because I_{CO} plays major role in Ge.*

ii. The compensation for V_{BE} is used for Si BJT because V_{BE} higher for Si BJT as compred to Ge BJT.

2.7.3 Bias Compensation using Thermistor

The bias compensation for variation in I_C due to variation in temperature can be provided either by connecting a device with negative temperature co-efficient such as thermistor between supply terminal and emitter terminal of BJT or by connecting thermistor in either of arms of potential divider.

I. Compensation by connecting thermistor between supply terminal and emitter

The circuit for bias compensation by connecting a thermistor between supply terminal and emitter is shown in Fig. 22.

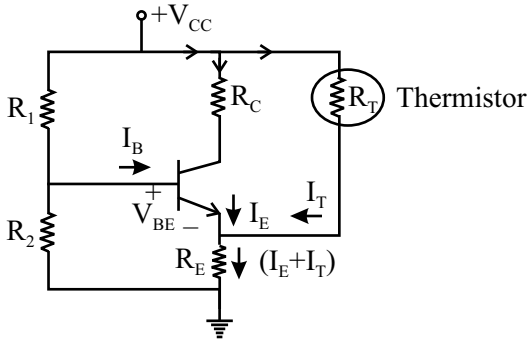


Fig.22 Bias compensation using thermistor between supply terminal and emitter

The potential divider of above circuit can be replaced by its Thevenin's equivalent as shown in Fig. 23.

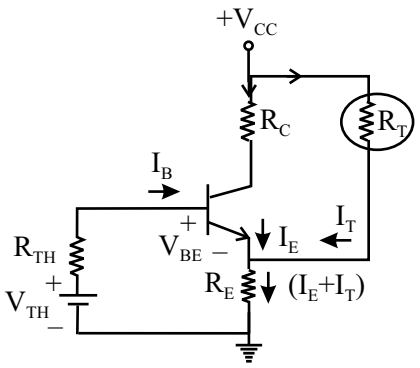


Fig.23 Potential divider replaced by its thevenin's equivalent circuit

Applying KVL in the base circuit, we have,

$$V_{TH} - I_B R_{TH} - V_{BE} - R_E(\beta + 1) I_B - R_E I_T = 0 \quad (114)$$

$$I_B = \frac{V_{TH} - V_{BE} - R_E I_T}{R_{TH} + (1+\beta) R_E} \quad (115)$$

Collector current, $I_C = \beta I_B$ (116)

When temperature of BJT is increased the collector current try to increase. As thermistor has a negative temperature co-efficient, therefore, resistance of thermistor is decreased and current I_T is

increased. Increase in current I_T results in increase in drop across R_E and which in turn results in decrease in base current. The decrease in base current again results in reduction in collector current. Hence increase in collector current with increase in temperature is compensated by reduction in base current due to decrease in resistance of thermistor. The voltage drop across R_E provides a negative feedback in base circuit which helps in stabilization of Q-point of BJT.

II. Compensation by connecting thermistor in place of lower resistance Rw of potential divider

The circuit for bias compensation by connecting a thermistor in place of lower resistor of potential divider is shown in Fig. 24.

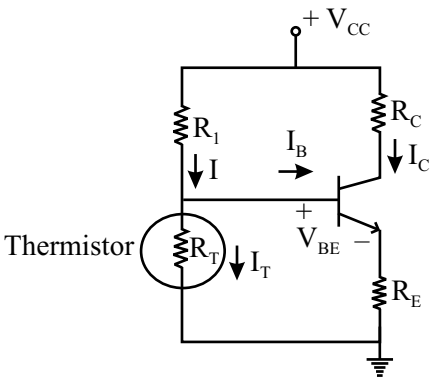


Fig.24 Bias compensation using thermistor in potential divider

Base current, $I_B = I - I_T$ (117)

Collector current, $I_C = \beta I_B$ (118)

The increase in temperature results in increase in collector current and decrease in resistance of thermistor. Decrease in resistance of thermistor results in increase in current I_T through the thermistor. The increase in thermistor current results decrease in base current I_B because current I remains almost constant with temperature. Decrease in base current results in reduction in collector current. Hence increase in collector current due to temperature is compensated by decrease in base current due to increase in thermistor current with temperature.

Note : *Thermistor in base emitter circuit provides compensation for self bias as well as fixed bias circuit. But thermistor across collector provides compensation for self bias circuit only.*

2.7.4 Bias Compensation using Sensistor

Sensistor is a semiconductor device with positive temperature coefficient. Therefore, the resistance of sensistor increases with increase in temperature.

I. Compensation by connecting sensistor in upper part of potential divider

The circuit for bais compensation by connecting a sensistor in place of upper resistance of potential divider is shown in Fig. 25.

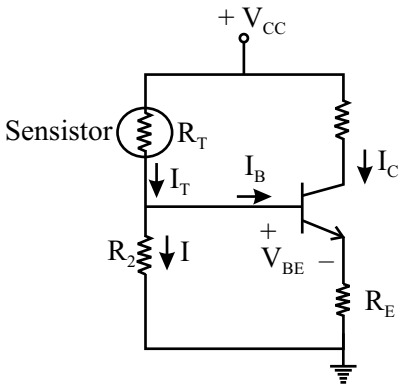


Fig.25 Bias compensation using sensistor in potential divider

Base current, $I_B = I_T - I$ (119)

Collector current, $I_C = \beta I_B$ (120)

The increase in temperature results in increase in collector current and increase in resistance of sensistor. Increase in resistance of sensistor results in decrease in current I_T through the sensistor. The decrease in sensistor current results decrease in base current I_B because current I remains almost constant with temperature. The decrease in base current results in reduction in collector current. Hence increase in collector current due to temperature is compensated by decrease in base current due to increase in thermistor current with temperature.

II. Compensation by connecting sensistor in series with emitter terminal

The circuit for bias compensation by connecting a sensistor in series with emitter terminal of BJT is shown in Fig. 26.

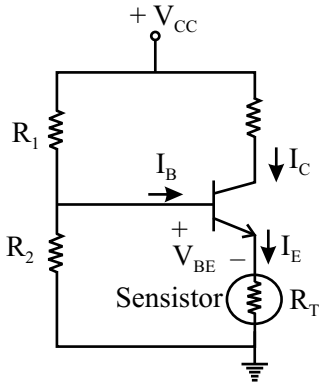


Fig.26 Bias compensation using sensistor in series with emitter

The potential divider of above circuit can be replaced by its Thevenin's equivalent as shown in Fig. 27.

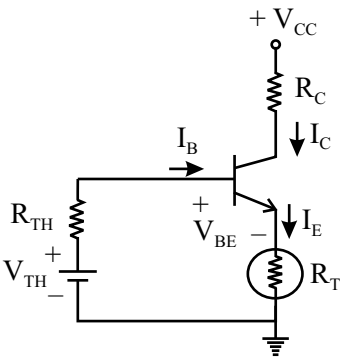


Fig.27 Potential divider replaced by its Thevenin's equivalent circuit

Applying KVL in the base circuit we have,

$$V_{TH} - I_B R_{TH} - V_{BE} - R_T(\beta + 1)\, I_B = 0 \qquad (121)$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)\, R_T} \qquad (122)$$

Collector current, $I_C = \beta I_B$ (123)

The increase in temperature results in increase in collector current and increase in resistance of sensistor. Increase in resistance of sensistor results in increase in decease in the base current. The decrease in base current results in reduction in collector current. Hence increase in collector current due to temperature is compensated by decrease in base current due to increase in resistance of sensistor.

2.8 Thermal Runaway and Thermal Stability

The maximum power dissipated in a BJT is limited by the temperature of collector junction. The collector current of BJT increases with increase in temperature. The increase in collector current with temperature results in increase in heat generated at the collector junction which in turn further increases the temperature and hence the collector current. The effect becomes cumulative resulting in thermal breakdown or thermal runaway of the BJT. The thermal runaway may damage the transistor permanently.

Thermal Resistance

The temperature rise at collector junction is proportional to the power dissipation at junction.

$$\therefore \quad T_j - T_A \propto P_D \qquad (124)$$

where, T_j is temperature of junction, T_A is ambient temperature and P_D is power dissipated

By replacing the proportionality sign by a proportionality constant, we have,

$$T_j - T_A = \theta\, P_D \qquad (125)$$

where, proportionality constant, θ, is called thermal resistance.

Differentiating P_D w.r.t. junction temperature, T_j, we have,

$$\frac{\partial P_D}{\partial T_j} = \frac{1}{\theta} \tag{126}$$

It is observed from above equation that the rate of heat dissipation w.r.t. junction temperature is equal to $\frac{1}{\theta}$.

Condition of Thermal stability

The heat generated at the junction should be less than the rate of heat dissipation for thermal stability of the transistor. Therefore, thermal runaway of BJT can be avoided if,

$$\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \tag{127}$$

where, P_C is heat generated at the collector junction of the BJT.

$$\Rightarrow \quad \frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \tag{128}$$

Condition of Thermal stability of self-bias circuit

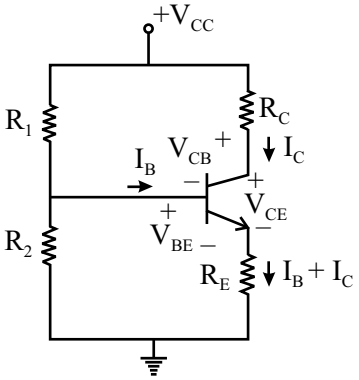


Fig.28 Circuit of CE configuration of BJT for thermal stability

Applying KVL in the collector circuit, we have,

$$V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E \tag{129}$$

Let, $$I_C + I_B \approx I_C \tag{130}$$

$$\Rightarrow \quad V_{CE} \approx V_{CC} - I_C R_C - I_C R_E \tag{131}$$

$$\Rightarrow \quad V_{CE} \approx V_{CC} - I_C (R_C + R_E) \tag{132}$$

Power generated at collector junction,

$$P_C = V_{CB} I_C \tag{133}$$

For active region, $$V_{CB} = V_{CE} - V_{BE} \approx V_{CE} \tag{134}$$

$$\Rightarrow \quad P_C \approx V_{CE} I_C$$

Putting expression of V_{CE} from equation (131) in above equation, we have,

$$P_C \approx V_{CC}I_C - I_C^2(R_C + R_E) \tag{135}$$

Condition for thermal stability of BJT,

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta} \tag{136}$$

Or $$\left(\frac{\partial P_C}{\partial I_C}\right).\left(\frac{\partial I_C}{\partial T_j}\right) < \frac{1}{\theta} \tag{137}$$

The collector current increases with increase in temperature.

$$\therefore \quad \frac{\partial I_C}{\partial T_j} > 0 \tag{138}$$

If collector current increases with temperature then heat generated at collector junction must decrease with collector current for thermal stability of BJT.

Therefore, for thermal stability of BJT,

$$\frac{\partial P_C}{\partial I_C} < 0 \tag{139}$$

$$\Rightarrow \quad \frac{\partial}{\partial I_C}(V_{CC}I_C - I_C^2(R_C + R_E) < 0 \tag{140}$$

$$\Rightarrow \quad V_{CC} - 2I_C(R_C + R_E) < 0 \tag{141}$$

$$\Rightarrow \quad I_C > \frac{V_{CC}}{2(R_C + R_E)} \tag{142}$$

From equation (131), $$I_C = \frac{V_{CC} - V_{CE}}{(R_C + R_E)} \tag{143}$$

Putting above relation of I_C in equation (7.132), we have,

$$\frac{V_{CC} - V_{CE}}{R_C + R_E} > \frac{V_{CC}}{2(R_C + R_E)} \tag{144}$$

$$\Rightarrow \quad V_{CC} - V_{CE} > \frac{V_{CC}}{2} \tag{145}$$

$$\Rightarrow \quad V_{CE} < \frac{V_{CC}}{2} \tag{146}$$

Above equation gives the condition of thermal stability of BJT in common emitter configuration of BJT. The relation given by equation (146) restricts the operating point of BJT in upper half of load

line as shown in Fig.29.

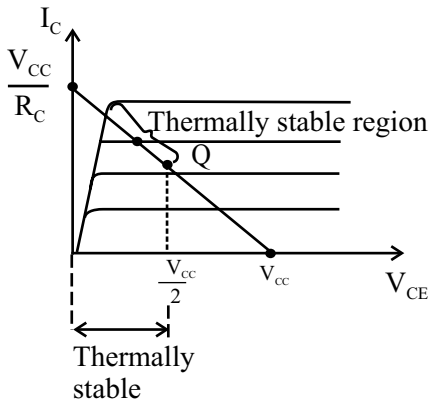


Fig.29 Location of operating point of BJT for thermal stability in CE configuration

It is observed from output characteristics and load line of CE configuration of BJT that the BJT is thermally stable if its operating point lies in upper half of load line.

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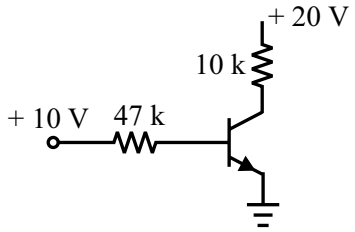
GATE QUESTIONS

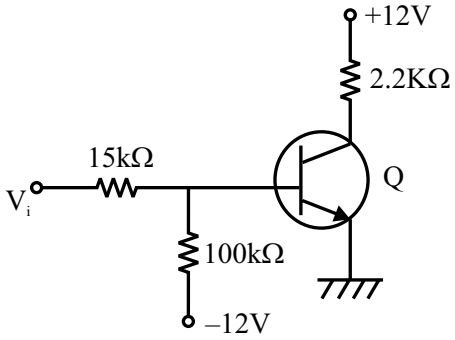
Q.1 In the transistor circuit shown in figure below, collector-to-ground voltage is + 20 V. Which of the following is the probable cause of error?



(a) Collector-emitter terminals shorted
(b) Emitter to ground connection open
(c) 10 KΩ resistor open
(d) collector-base terminals shorted

GATE(EE/1994/1 M)

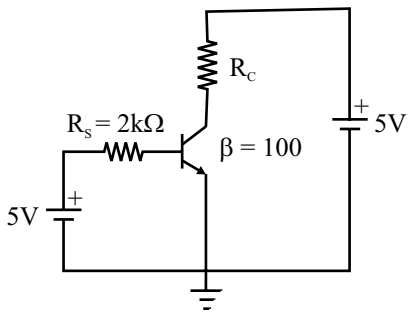
Q.2 Consider the circuit shown in figure.If the β of the transistor is 30 and I_{CBO} is 20 nA and the input voltage is +5V, the transistor would be operating in



(a) Saturation region
(b) Active region
(c) Breakdown region
(d) Cut-off region

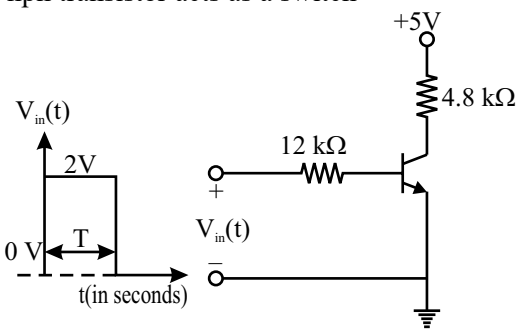
GATE(EE/2006/2 M)

Q.3 The transistor in the given circuit should always be in active region. Take $V_{CE(sat)}$ = 0.2 V, V_{BE} = 0.7 V. The maximum value of R_c in Ω which can be used, is_____



GATE(EE-II/2014/1M)

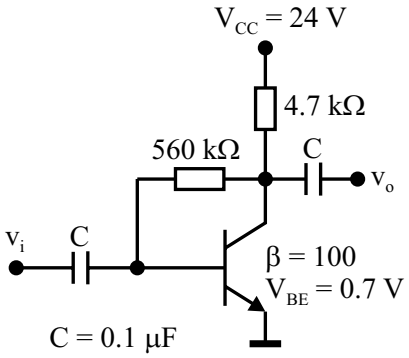
Q.4 In the figure shown, the npn transistor acts as a switch



For the input $V_{in}(t)$ as shown in the figure, the transistor switches between the cut-off and saturation regions of operation, when T is large. Assume collector-to-emitter voltage saturation $V_{CE(sat)} = 0.2V$ and base-to-emitter voltage $V_{BE} = 0.7V$. The minimum value of the common-base current gain (α) of the transistor for the switching should be _____.

GATE(EC-I/2017/2M)

Q.5 A transistor amplifier circuit is shown in figure. The quescent collector current, rounded off to first decimal, is

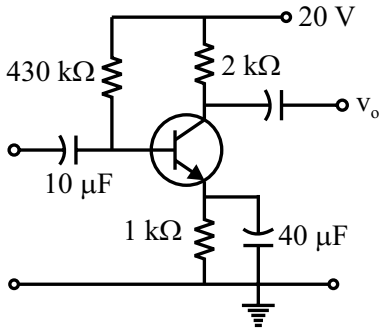


(a) 2.6 mA (b) 2.3 mA

(c) 2.1 mA (d) 2.0 mA

GATE(IN/2003/2M)

Q.6 The circuit using a BJT with $\beta = 50$ and $V_{BE} = 0.7V$ is shown in figure. The base current I_B and collector voltage V_C are respectively

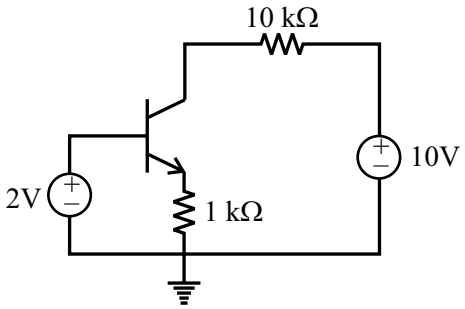


(a) 43 μA and 11.4 Volts (b) 40 μA and 16 Volts

(c) 45 μA and 11 Volts (d) 50 μA and 10 Volts

GATE(EC/2005/2M)

Q.7 For the BJT circuit shown, assume that the β of the transistor is very large and V_{BE} = 0.7 V. The mode of operation of the BJT is

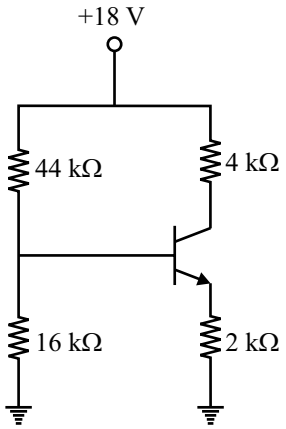


(a) Cutt-off (b) Saturation

(c) Normal active (d) Reverse active

GATE(EC/2007/2M)

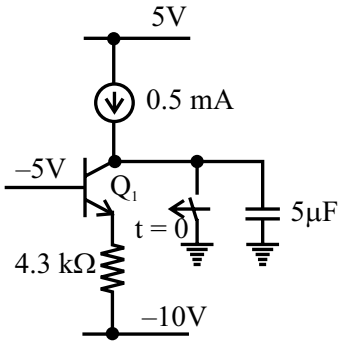
Q.8 Consider the circuit shown in the figure. Assume base-to- emitter voltage V_{BE}= 0.8 V and common base current gain (α) of the transistor is unity.



The value of the collector- to – emitter voltage V_{CE} (in volt) is _____.

GATE(EC-II/2017/1M)

Q.9 For the BJT Q_1 in the circuit shown below, β = ∞, V_{BEon} = 0.7 V. The switch is initially closed. At time t = 0, the switch is opened. The time t at which Q_1 leaves the active region is

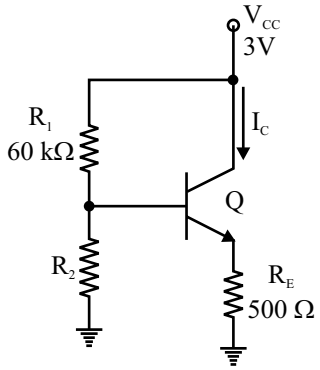


(a) 10 ms (b) 25 ms

(c) 50 ms (d) 100 ms

GATE(EC/2011/2M)

Q.10 In the circuit shown below, the silicon npn transistor Q has a very high value of β. The required value of R_2 in kΩ to produce I_C = 1 mA is

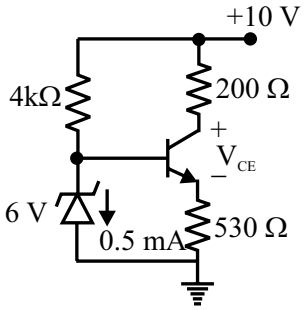


(a) 20 (b) 30

(c) 40 (d) 50

GATE(EC/2013/2M)

Q.11 In the circuit shown below, V_{BE}= 0.7 V.



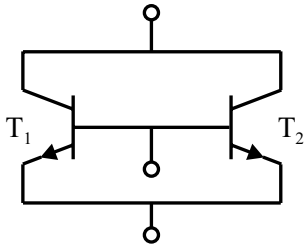
The β of the transistor and V_{CE} are, respectively.

(a) 19 and 2.8 V (b) 19 and 4.7 V

(c) 38 and 2.8 V (d) 38 and 4.7 V

GATE(IN/2007/2M)

Q.12 Discrete transistors T_1 and T_2 having maximum collector current rating of 0.75 amps are connected in parallel as shown in the figure. This combination is treated as a single transistor to carry a total current of 1 ampere, when biased with self bias circuit. When the circuit is switched on, T_1 draws 0.55 amps and T_2 draws 0.45 amps. If the supply is kept on continuously, ultimately it is very likely that

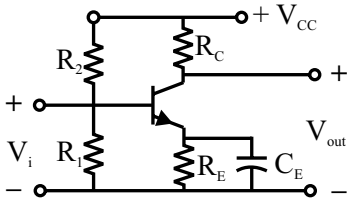


(a) Both T_1 and T_2 set get damaged (b) Both T_1 and T_2 will be safe

(c) T_1 will get damaged and T_2 will be safe (d) T_2 will damaged and T_1 will be safe.

GATE(EC/1991/2M)

Q.13 For good stabilised biasing of the transistor of the CE amplifier of figure we should have



(a) $\frac{R_E}{R_B} << 1$ (b) $\frac{R_E}{R_B} >> 1$

(c) $\frac{R_B}{R_E} << h_i L$ (d) $\frac{R_B}{R_E} << h_t L$

GATE(EC/1990/2M)

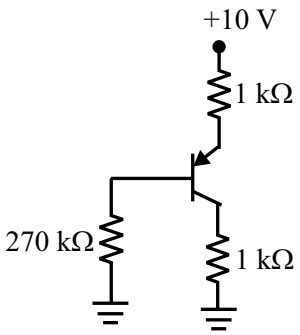
Q.14 Introducing a resistor in the emitter of a common amplifier stabilizes the dc operating point against variations in

(a) only the temperature (b) only the β of the transistor

(c) both temperature and β (d) none of the above

GATE(EC/2000/1M)

Q.15 The common emitter forward current gain of the transistor shown is β=100.



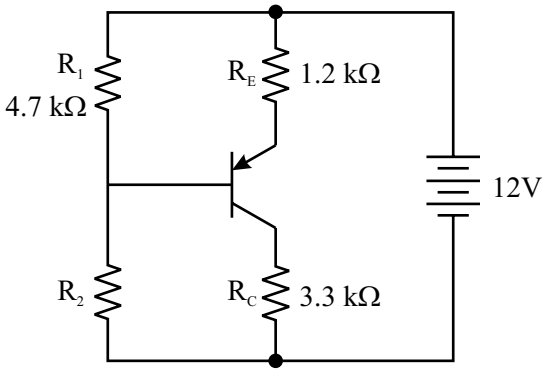
The transistor is operating in

(a) Saturation region (b) Cutoff region

(c) Reverse active region (d) Forward active region

GATE(EE/2007/1 M)

Q.16 In the BJT circuit shown, beta of the PNP transistor is 100. Assume $V_{BE} = -0.7$ V. The voltage across R_C will be 5 V when R_2 is _____ kΩ. (Round off to 2 decimal places.)



GATE/(EE/2021/1M)

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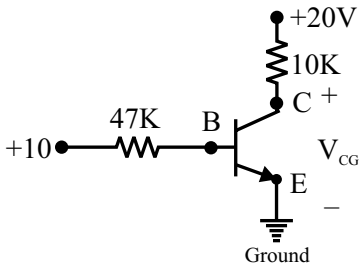
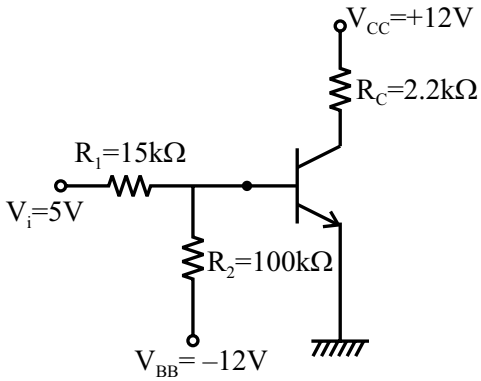
ANSWERS & EXPLANATIONS

Q.1 ***Ans.(b)***

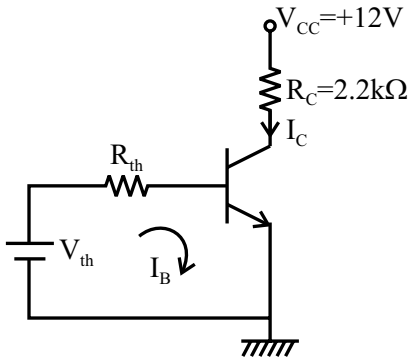


If collector to ground voltage (i.e. V_{CG}) is + 20 V then voltage drop across R_C is also zero. Voltage drop across R_C can be zero only if collector current is zero. The collector current under the given condition (i.e. $V_{CG} = +20$ V) can be zero only if either BJT is off or emitter terminal is open circuited.

Q.2 ***Ans.(b)***



Above circuit can be redrawn as under,



where,

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_i - \frac{R_1}{R_1 + R_2} \times V_{BB} = \frac{100}{100+15} \times 5 - \frac{15}{100+15} \times 12$$

$$= \frac{64}{23}\text{V}$$

and $$R_{th} = \frac{100\times 15}{100+15} = \frac{1500}{115} = \frac{300}{23}\text{k}\Omega$$

Applying KVL in base circuit, we have,

$$V_{th} - R_{th} I_B - V_{BE} = 0$$

$$\Rightarrow \quad \frac{64}{23} - \frac{300}{23}\times I_B - 0.7 = 0$$

$$\Rightarrow \quad I_B = \frac{64 - 0.7\times 23}{300} = 159.67\ \mu\text{A}$$

$$\Rightarrow \quad I_B \approx 160\ \mu\text{A}$$

Let BJT is operating in active region. Then collector current,

$$I_C = \beta I_B + (1+\beta)\, I_{CBO}$$

Given, $\beta = 30$, $I_{CBO} = 20$ nA

$$\Rightarrow \quad I_C = 30 \times 160 \times 10^{-3} + (1+30) \times 20 \times 10^{-6}\ \text{mA}$$

$$\Rightarrow \quad I_C \approx 4.8\ \text{mA}$$

Applying KVL in collector circuit, we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow \quad 12 - 4.8 \times 2.2 - V_{CE} = 0$$

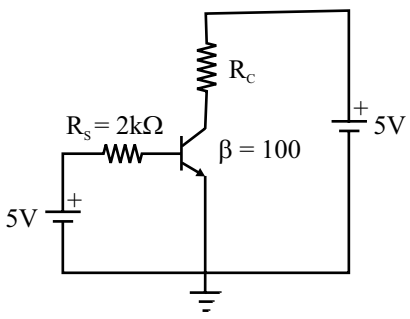
$$\Rightarrow \quad V_{CE} = 1.44\ \text{V}$$

Voltage V_{CE} at saturation, $V_{CE,sat} = 0.2$

BJT operates in active region when $V_{CE} > V_{CE,sat}$

So, transistor in given circuit operates in active region.

Q.3 Ans. (22 to 23)



Given, $V_{BE} = 0.7V$

$V_{CE(sat)} = 0.2V$

Applying KVL in base circuit gives,

$5 - 2I_B - 0.7 = 0$

$\Rightarrow \quad I_B = \frac{5-0.7}{2k} = 2.15mA$

Let BJT is operating in saturation region.

Applying KVL in the collector circuit gives,

$5 - R_C I_{C,sat} - V_{CE(sat)} = 0$

$\Rightarrow \quad I_{C,sat} = \frac{5 - V_{CE(sat)}}{R_C} = \frac{5-0.2}{R_C}$

For active region,

$$I_B < \frac{I_{C,sat}}{\beta}$$

$\Rightarrow \quad 2.15 \times 10^{-3} < \frac{5-0.2}{\beta R_C}$

Given, $\beta = 100$

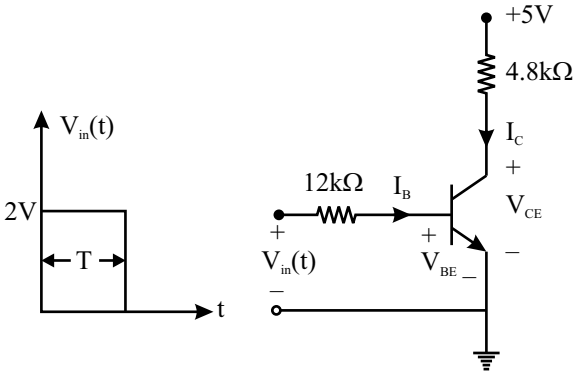
$\Rightarrow \quad R_C < \frac{4.8}{2.15\times10^{-3}\times100}$

$\Rightarrow \quad R_C < 22.32\Omega$

Therefore, maximum value of R_C for active region,

$R_C = 22.32\Omega$

Q.4 Ans. : 0.89 to 0.91



From base circuit,

$$V_{in} - 12k \times I_B - V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{in} - V_{BE}}{12k}$$

when BJT is ON, $V_{in} = 2V$

$$\Rightarrow \quad I_B = \frac{2 - 0.7}{12k} = 0.108mA$$

Collect current,

$$I_{C,sat} = \frac{5 - V_{CS(sat)}}{4.8k} = \frac{5 - 0.2}{4.8k} = 1mA$$

Minimum base current required for switching of BJT from cut-off to saturation state,

$$I_B > \frac{I_{C,sat}}{\beta}$$

$$\Rightarrow \quad 0.108 > \frac{1}{\beta}$$

$$\Rightarrow \quad \beta > \frac{1}{0.108}$$

Relation between α & β is given by,

$$\beta = \frac{\alpha}{1 - \alpha}$$

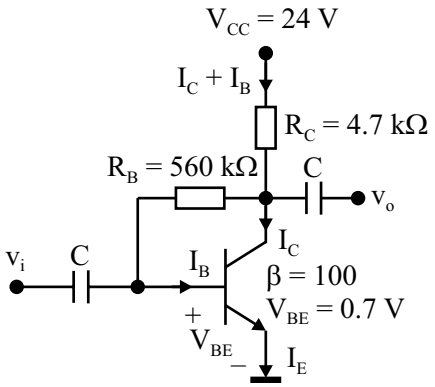
$$\therefore \quad \frac{\alpha}{1 - \alpha} > \frac{1}{0.108}$$

$$\Rightarrow \quad \alpha > 0.902$$

Therefore, minimum value of α should be

$$\alpha_{min} = 0.902$$

Q.5 Ans.(b)



Applying KVL, in base circuit, we have,

$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$

For active region,

$$I_C = \beta I_B$$

$$\Rightarrow \quad V_{CC} - V_{BE} = (1+\beta)\, I_B R_C + I_B R_B$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B}$$

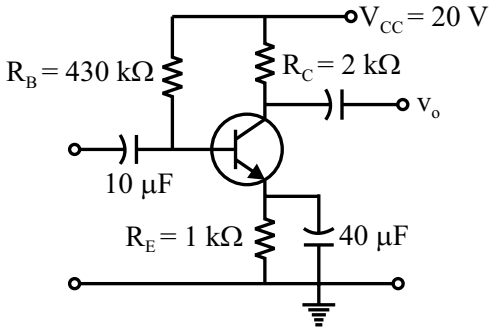
Given,

$V_{CC} = 24$V, $R_C = 4.7$ kΩ, $R_B = 560$kΩ, $\beta = 100$, $V_{BE} = 0.7$V.

$$\Rightarrow \quad I_B = \frac{24 - 0.7}{101 \times 4.7 + 560} = 22.52\ \mu A$$

So, the collector current, $I_{CQ} = \beta I_B = 100 \times 22.52\ \mu A = 2.252$ mA

Q.6 ***Ans.(b)***



The coupling capacitor behaves like open circuit for dc biasing signals.

Apply KVL in base region, we get,

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$

$$\Rightarrow \quad 20 - 0.7 = 430 \times I_B + (50 + 1) \times I_B \times 1$$

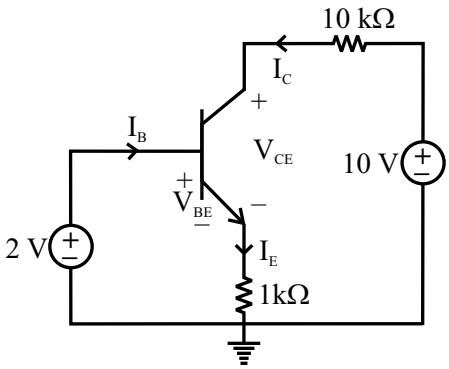
$$\Rightarrow \quad 19.3 = (430 + 51) I_B$$

$$\Rightarrow \quad I_B = \frac{19.3}{481} \text{ mA} = 40 \ \mu\text{A}$$

Collector current, $I_C = \beta I_B = 50 \times 40 \ \mu\text{A} = 2 \text{ mA}$

Collector voltage, $V_C = V_{CC} - I_C R_C = 20 - 4 = 16 \text{ V}$

Q.7 ***Ans.(b)***



Appying KVL in base circuit,

$$2 - V_{BE} = 1 \times I_E \qquad \text{.....(i)}$$

Emitter current, $I_E = I_C + I_B = I_C\left(1 + \frac{1}{\beta}\right)$

When, β is large, $1 + \frac{1}{\beta} \approx 1$

$$\therefore \quad I_E \approx I_C \qquad \text{.....(ii)}$$

Putting above relation in (i), we have,

$$2 - V_{BE} = I_C$$

$$\Rightarrow \quad I_C = 2 - 0.7 = 1.3 \text{ mA}$$

Applying KVL in collector circuit,

$$10 - I_C \times 10 - V_{CE} - 1 \times I_E = 0$$

Using relation of (ii), in above equation, we have,

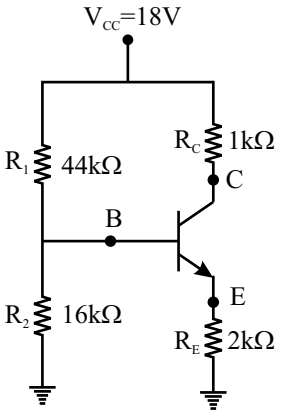
$$V_{CE} = 10 - 11 I_C = 10 - 11 \times 1.3 = -4.3 \text{ V}$$

$$V_{CB} = V_{CE} - V_{BE,active} = -4.3 - 0.7 = -5 \text{ V}$$

Negative value of V_{CB} represents forward biased collector junction. Since V_{CB} is negative, therefore,

the transistor must be operating in saturation region.

Q.8 Ans. : 5.5 to 6.5

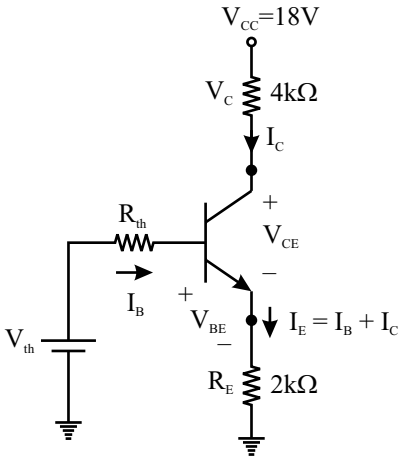


Given, $V_{BE} = 0.8V$

$\alpha = 1$

current gain, $\beta = \dfrac{1}{1-1} = \infty$

Replacing potential divider in base circuit by its Thevenin is equivalent, the circuit can be drawn as under,



The value of V_{th} and R_{th} are given as,

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{16}{44+16} \times 18 = 4.8\ V$$

and $$R_{th} = \frac{R_2 R_1}{R_2 + R_1} = \frac{16 \times 44}{16+44} = 11.73\Omega$$

KVL in base circuit gives,

$V_{th} - I_B R_{th} - V_{BE} - R_E (I_B + I_C) = 0$

$4.8 - I_B \times 11.73 - 0.8 - 2k(I_B + I_C) = 0$

$\Rightarrow \quad 11.73\, I_B + 2k\, (I_B + I_C) = 4$

Relation between I_C & I_B is given by

$$I_B = \frac{I_C}{\beta} = \frac{I_C}{\infty} = 0$$

$\therefore \quad 11.73 \times 0 + 2k\, (0 + I_C) = 4$

$\Rightarrow \qquad I_C = 2$ mA

Emitter current, $I_E = I_B + I_C = 0 + I_C = I_C = 2$ mA

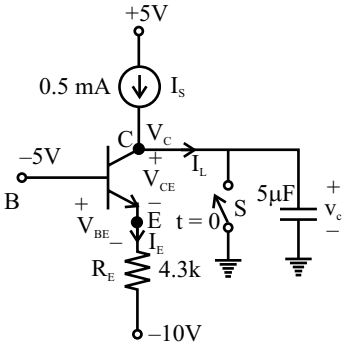
Applying KVL in collector circuit gives,

$V_{CC} - I_C R_C - V_{CE} - R_E I_E = 0$

$\Rightarrow \quad 18 - 2 \times 4 - V_{CE} - 2 \times 2 = 0$

$\Rightarrow \qquad V_{CE} = 6$V

Q.9 ***Ans.(c)***



Case-I :- When switch S is closed

When the switch S is closed the voltage at collector terminal is zero. The collector junction is reverse biased and emitter junction is forward biased and BJT operates in active region.

Applying KVL in the base circuit, we have,

$V_B - V_{BE} - V_E = 0$

$\Rightarrow \qquad -5 - 0.7 - V_E = 0$

$\Rightarrow \qquad V_E = -5.7$ V

The emitter current can be given by,

$$I_E = \frac{V_E - (-10)}{R_E} = \frac{-5.7 + 10}{4.3} = 1 \text{ mA}$$

Voltage of capacitor, $V_c = 0$ V

Case-II :- When switch S is opened at t = 0

Applying KVL on load side,

$$+\ V_C - V_{CE} - I_E R_E - V_{EE} = 0$$

$$V_C - V_{CE} - 4.3 + 10 = 0$$

At saturation, $V_{CE} = 0.2$ V

$$V_C = -10 + 4.3 + 0.7 = -5.5\text{V}$$

Applying KCL at collector terminal, we have,

$$I_S = I_C + I_L$$

Current through capacitor, $I_C = I_S - I_L$

For large value of transistor gain b, the emitter current is approximately same as collector current.

$$I_C = I_E - I_B = I_E - \frac{I_C}{\beta} \approx I_E = 1 \text{ mA}$$

$$\Rightarrow \quad 1 = 0.5 \text{ mA} - I_L$$

$$\Rightarrow \quad I_L = -0.5 \text{ mA}$$

Current through capacitor,

$$I_C = C\frac{dV_C}{dt} = I_L$$

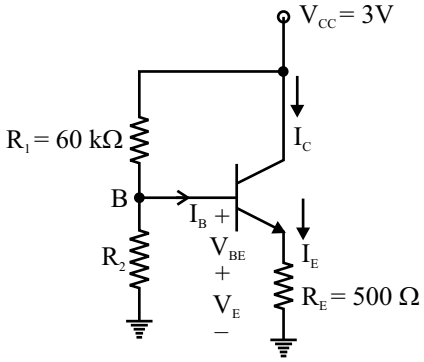
$$\Rightarrow \quad V_C = \frac{1}{C}\int_0^T I_L\, dt$$

Let T is period required to drive transistor from active to saturation. The voltage of the capacitor is appears at collector terminal. When this voltage becomes equal to the base voltage the BJT operation changes from active to saturation. So, operation of given BJT changes from active region to saturation when the capacitor voltage becomes equal to –5V.

$$\Rightarrow \quad -5 = \frac{1}{5\times10^{-6}}\int_0^T (-0.5\times10^{-3})\,dt$$

$$\Rightarrow \quad T = \frac{5\times5\times10^{-6}}{0.5\times10^{-3}} = 50 \text{ ms}$$

Q.10 Ans.(c)



Given, $I_C = 1$ mA

Base current, $I_B = \frac{I_C}{\beta} = \frac{1}{\beta}$ mA

when β is very high I_B is negligible

Emitter current,

$$I_E = I_C + I_B \approx I_C$$

$\therefore$ $I_E = 1$ mA

Voltage at base terminal,

$$V_B = V_{BE} + I_E R_E$$

$\Rightarrow$ $V_B = 0.7 + 1\times10^{-3} \times 500$

$\Rightarrow$ $V_B = 1.2$ V

If base current is negligible then,

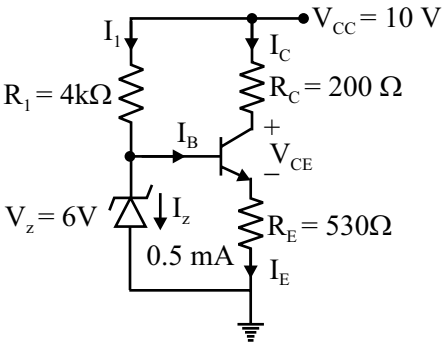
$$V_B \approx \frac{R_2}{60\times10^3 + R_2} \times V_{CC}$$

$$\Rightarrow \quad 1.2 = \frac{R_2}{60\times10^3 + R_2} \times 3$$

$$\Rightarrow \quad 1.8\, R_2 = 1.2 \times 60 \times 10^3$$

$$\Rightarrow \quad R_2 = \frac{1.2}{1.8} \times 60\times10^3 = 40\ \text{k}\Omega$$

Q.11 Ans.(a)



From above circuit,

$$I_B = \frac{V_{CC} - V_Z}{R_1} - I_Z = \frac{10-6}{4} - 0.5 = 0.5\text{mA}$$

Voltage across the emitter resistance,

$$V_E = V_Z - V_{BE} = 6 - 0.7 = 5.3 \text{ V}$$

Emitter current,

$$I_E = \frac{V_E}{R_E} = \frac{5.3}{530} - 0.5 = 10\text{mA}$$

Collector current,

$$I_C = I_E - I_B = 10 - 0.5 = 9.5 \text{ mA}$$

DC current gain of transistor,

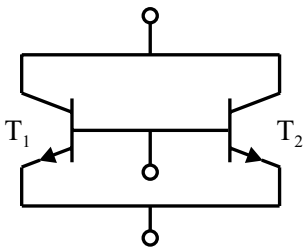
$$\beta = \frac{I_C}{I_B} = \frac{9.5}{0.5} = 19$$

Voltage at collector terminal,

$$V_C = V_{CC} - I_C R_C = 10 - 9.5 \times 0.2 = 8.1 \text{ V}$$

Voltage, $V_{CE} = V_C - V_E = 8.1 - 5.3 = 2.8$

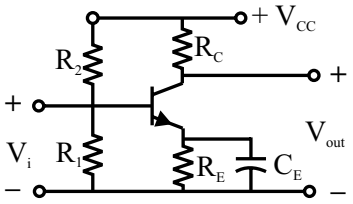
Q.12 Ans.(c)



When collector current in T_1 is more than that of T_2 the heat dissipation at collector junction is more in T_1 than T_2. So, the temperature rise at collector of T_1 is more than that of T_2. Higher heat dissipation at collector junction of T_1 results in generation of more number of electron hole pairs at collector junction of T_1 and hence collector current in T_1 is further increased and collector current in T_2 is decreased because the total current through both transistor is constant at 1 mA. This effect becomes cummulative. At one stage the current in T_1 increases beyond maximum limit resulting

in damage of collector junction of T_1. Therefore, negative temperature co-efficient of BJT makes it unsuitable for parallel operation.

Q.13 ***Ans.(b)***



The stability factor of above circuit is given by,

$$S_{I_{CO}} = \frac{(1+\beta)\left(1+\frac{R_B}{R_E}\right)}{(\beta+1)+\frac{R_B}{R_E}}$$

For good stabilizing circuit stability factor should be independent of a β for which

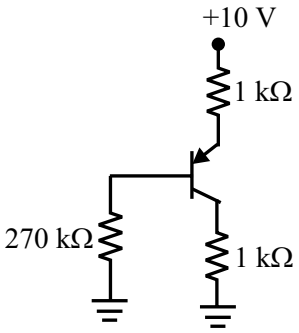
$$\frac{R_B}{R_E} \ll 1$$

$$\Rightarrow \quad \frac{R_E}{R_B} \gg 1$$

Q.14 ***Ans.(c)***

Introducing a resistor in the emitter of a common amplifier stabilizes the dc operating point against variations in both temperature and β.

Q.15 The common emitter forward current gain of the transistor shown is β=100.

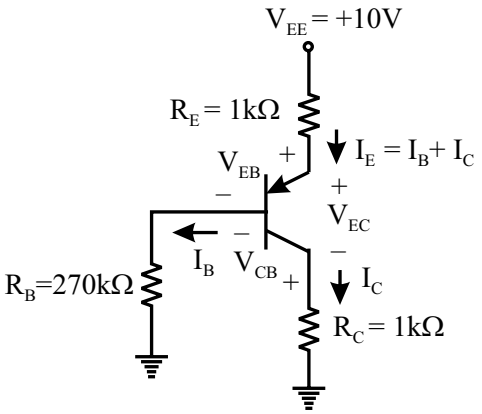


The transistor is operating in

(a) Saturation region
(b) Cutoff region
(c) Reverse active region
(d) Forward active region

GATE(EE/2007/1 M)

Q.15 ***Ans.(d)***



Applying KVL in base circuit,

$$V_{EE} - I_E R_E - V_{EB} - I_B R_B = 0$$

$$\Rightarrow \quad V_{EE} - (I_B + I_C) R_E - V_{EB} - I_B R_B = 0$$

Let BJT operates in active mode with $I_C = \beta I_B$, then

$$V_{EE} - (\beta + 1)\, I_B\, R_E - V_{EB} - I_B\, R_B = 0$$

$$\Rightarrow \qquad I_B = \frac{V_{EE} - V_{EB}}{R_B + (1+\beta) R_E}$$

For pnp transistor,

$$V_{EB} = 0.7\ \text{V}$$

$$\Rightarrow \qquad I_B = \frac{10 - 0.7}{270 + (1+100)\times 1}$$

$$\Rightarrow \qquad I_B = 25\ \mu\text{A}$$

Collector current,

$$I_C = \beta I_B = 100 \times 25\ \mu\text{A}$$

$$\Rightarrow \qquad I_C = 2.5\ \text{mA}$$

Applying KVL in collector circuit,

$$V_{EE} - (I_B + I_C)\, R_E - I_C R_C - V_{EC} = 0$$

$$\Rightarrow \quad V_{EC} = V_{EE} - (1 + \beta) I_B R_E - I_C\, R_C$$

$$\Rightarrow \quad V_{EC} = 10 - 101 \times 25 \times 10^{-3} \times 1 - 2.5 \times 1$$

$$\Rightarrow \qquad V_{EC} = 4.975$$

Voltage across collector junction,

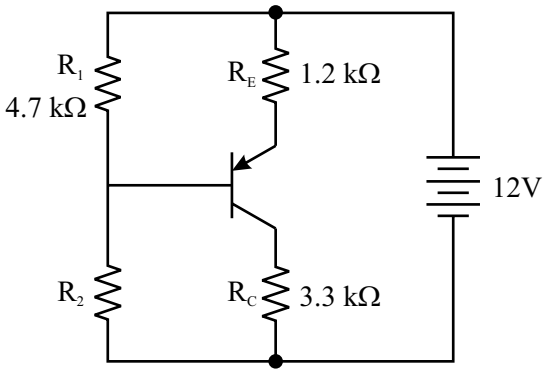
$$V_{BC} = V_{EB} - V_{EC} = 0.7 - 4.975 = -4.275$$

Negative value of V_{BC} for pnp transistor indicates that collector junction is reverse biased. So, BJT in given circuit operate in forward active mode as emitter junction is already forward biased.

Note : V_{BE} and V_{CE} are negative for PNP and positive for NPN transistors whereas V_{EB} and V_{EC} are

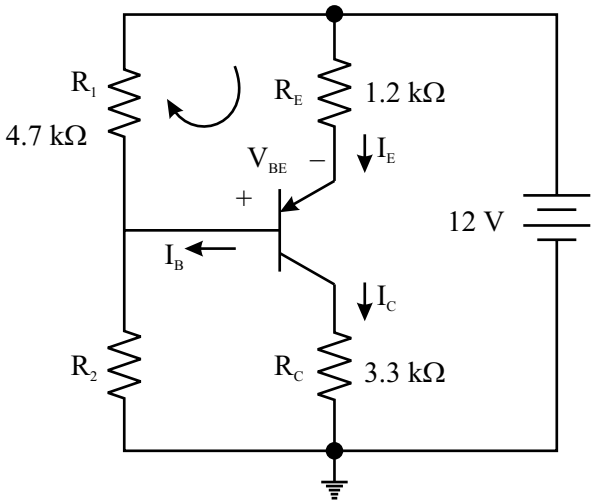
positive for PNP and negative for NPN transistors.

Q.16 In the BJT circuit shown, beta of the PNP transistor is 100. Assume $V_{BE} = -0.7$ V. The voltage across R_C will be 5 V when R_2 is _____ kΩ. (Round off to 2 decimal places.)

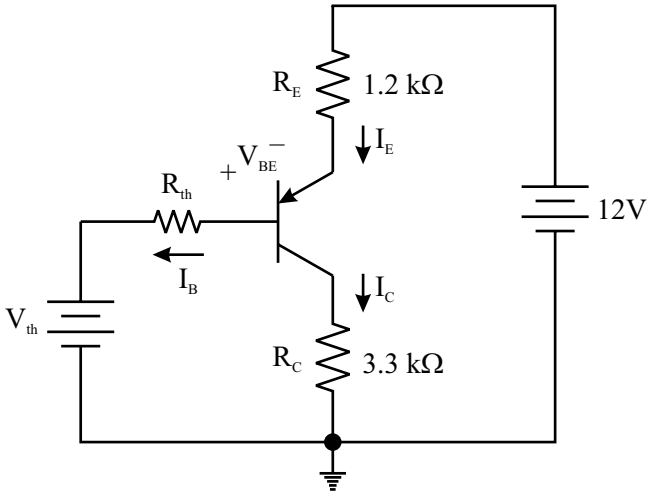


GATE/(EE/2021/1M)

Q.16 Ans.(16.70 to 17.70)



The potential divider can be replaced by ifs. Thevenin's equivalent, the circuit becomes as under,



Here, $R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$

$\Rightarrow$ $R_{th} = \frac{4.7 R_2}{4.7 + R_2}$

and $V_{th} = \frac{R_2}{R_1 + R_2} \times 12 = \frac{R_2}{4.7 + R_2} \times 12V$

Given, voltage across R_C,

$V_C = 5V$

Collector current, $I_C = \frac{V_C}{R_C} = \frac{5}{3.3} mA = 1.51 mA$

Base current, $I_B = \frac{I_C}{\beta} = \frac{5}{3.3} \times \frac{1}{100} mA$

$\Rightarrow$ $I_B = 15.15\ \mu A$

Emitter current, $I_E = \frac{1+\beta}{\beta} \times I_C = \frac{1+100}{100} \times \frac{5}{3.3} mA$

$\Rightarrow$ $I_C = 1.53\ mA$

Applying KVL in base emitter circuit, we have,

$12 - 1.2\ I_E + V_{BE} - I_B R_{th} - V_{th} = 0$

$12 - 1.2 \times 1.53 - 0.7 - 15.15 \times 10^{-3} R_{th} = V_{th}$

$\Rightarrow$ $\frac{R_2}{R_2 + 4.7} \times 12 = -\frac{15.15 \times 10^{-3} \times 4.7 R_2}{R_2 + 4.7} + 9.464$

$\Rightarrow$ $12 R_2 = -0.071\ R_2 + 9.464\ (R_2 + 4.7)$

$\Rightarrow$ $R_2 = -\frac{9.464 \times 4.7}{12 + 0.071 - 9.454} k\Omega$

$\Rightarrow$ $R_2 = 17.06\ k\Omega$

❐❐❐

Ch 3 MOSFET And JFET Biasing

3.1 Concept of Q-point and load line

Consider a enhancement MOSFET biasing circuit shown in Fig.1. In the amplifier circuit shown in Fig.1, the capacitors C_i and C_o are called input and output coupling capacitors, respectively. The coupling capacitors are used to block DC biasing signals from AC input and output signals of the amplifier. The coupling capacitors are replaced by open circuit for DC analysis and by short circuit for small signal AC analysis. Therefore, the coupling capacitors will not be shown in remaining part of this chapter for DC analysis. If only DC biasing signals are considered then the KVL in collector circuit can be written as,

$$V_{DD} = I_D R_D + V_{DS} \quad (1)$$

$$\Rightarrow \quad I_D = \frac{V_{DD} - V_{DS}}{R_D} \quad (2)$$

$$\Rightarrow \quad I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D} \quad (3)$$

Above equation represents a straight line on drain characteristics of enhancement MOSFET with slope of line equal to $-\frac{1}{R_D}$ and intercept on I_D-axis at $\frac{V_{DD}}{R_D}$ and intercept on V_{DS}-axis at V_{DD} as shown in Fig. 2. The straight line represented by above equation is called as DC load line of the amplifier circuit.

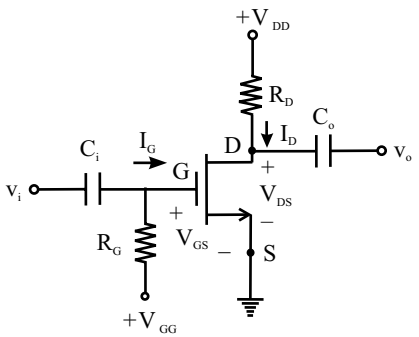


Fig. 1 MOSFET amplifier with fixed bais

A MOSFET has very high input resistance due to oxide layer, therefore, the gate current in MOSFET is zero.

$$\therefore \quad I_G = 0$$

Then gate to source voltage is same as DC biasing voltage in gate circuit as under,

$$V_{GS} = V_{GG} \tag{4}$$

The DC load line of MOSFET DC bias circuit along with drain characteristics and operating point are shown in Fig. 2.

Operating Point

The intersection of DC load line with drain characteristics corresponding to input gate to source voltage of the circuit is called the operating point or Q- point of the amplifier. The operating point is denoted by co-ordinates (V_{DSQ}, I_{DQ}) on the output characteristics as shown in Fig.2.

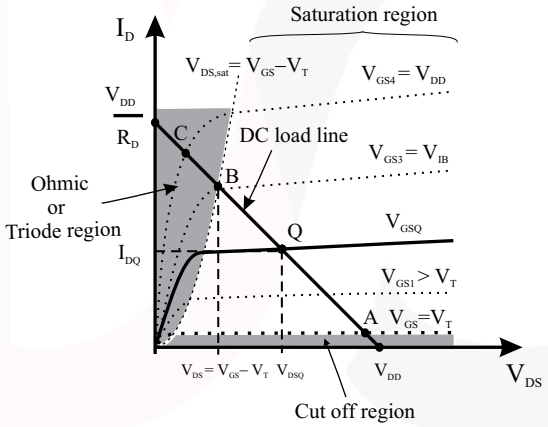


Fig.2 DC load line and drain characteristics of the MOSFET amplier circuit

3.2 Concept of Biasing of MOSFET

The biasing of a MOSFET involves establishing operating point or Q-point in desired region of operation i.e. saturation , cut-off or ohm regions. For amplifier applications the operating point should be located in saturation region and for switching applications the operating point shifts between ohmic and cut-off regions. The location of Q-point and various regions of operation of MOSFET amplifier are shown in Fig. 2. If drain voltage in amplifier circuit of Fig. 1 is taken as output voltage and gate to source voltage as input voltage then the output voltage of the circuit can be given by,

$$V_{DS} = V_{DD} - I_D R_D \tag{5}$$

The voltage transfer characteristics showing operation of MOSFET as an amplifier biased at operating point Q can be drawn as shown in Fig. 3. It is observed that the voltage transfer characteristics are almost linear for small variations of input voltage near Q-point in saturation region of operation. Therefore, MOSFET can be used as a linear voltage amplifier in saturation region of operation.

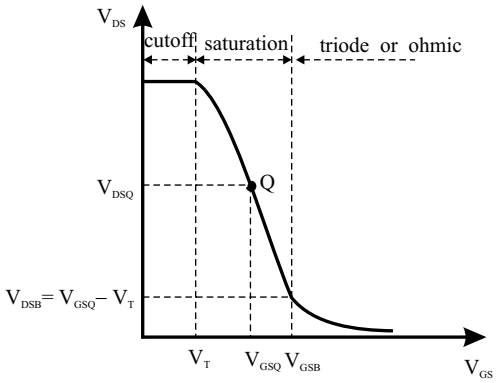


Fig.3 Voltage transfer characteristics of MOSFET amplifier circuit

Saturation region

A MOSFET works in saturation region when $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$. The drain current is non-linear function of gate to source input voltage in saturation region. The MOSFET works like a transconductance amplifier in saturation region of operation.

The drain current of enhancement type MOSFET in saturation region is given by,

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_T)^2 = K(V_{GS} - V_T)^2 \quad (6)$$

where $$K = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n}{2}\frac{W}{L}$$

and $$k_n = \mu_n C_{ox}$$

The parameters K & k_n are sometimes called as transconductance parameters. These are measured in $\mu A/V^2$.

If channel modulation effect is neglected then the drain current is independent of drain to source voltage in saturation region. However, MOSFET can be used a linear voltage amplifier in saturation region of operation for small signal variations.

Triode or Ohmic region:

A MOSFET work in ohmic region when $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$. The drain current is ohmic region is function of both gate to source and drain to source voltage. The MOSFET works like closed switch offering a finite resistance in ohmic region of operation.

The drain current of enhancement type MOSFET in ohmic region is given by,

$$I_D = K[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (7)$$

where $$K = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n}{2}\frac{W}{L}$$

Cut-off region

A MOSFET work in cut off region when $V_{GS} < V_T$ and $V_{DS} = V_{DD}$. The drain current is ohmic region is zero and the MOSFET works like an open switch cutoff region of operation.

Note: i. The drain current of N-MOSFET (or NMOS) flows from drain to source and it is represented by I_{DS} or I_D. The drain current of P-MOSFET (or PMOS) flows form source to drain and it is represented by I_{SD} or I_D. The expression of drain currents of P-MOSFET are given by,

$$I_D = \frac{\mu_p C_{ox} W}{2L}(V_{SG} - |V_T|)^2 \quad \text{; For saturation region} \qquad (8)$$

$$= \frac{\mu_p C_{ox} W}{L}\left[(V_{SG} - |V_T|)V_{SD} - \frac{V_{SD}^2}{2}\right] \quad \text{; For ohmic region} \qquad (9)$$

ii. The voltages V_{GS}, V_{DS} and V_T are positive for N-MOSFET and negative for a P-MOSFET . The voltages V_{SG}, V_{SD} are negative for N-MOSFET and postive for a P-MOSFET.

iii. A P-MOSFET works

a. In cutoff region when $V_{SG} < |V_T|$ or $V_{GS} > V_T$

b. In saturation region when $V_{SG} > |V_T|$ and $V_{SD} > (V_{SG} - |V_T|)$ or $V_{GS} < V_T$ and $V_{DS} < (V_{GS} - V_T)$

c. In ohmic region when $V_{SG} > |V_T|$ and $V_{SD} < (V_{SG} - |V_T|)$ or $V_{GS} < V_T$ and $V_{DS} > V_{GS} - V_T$

3.3 Biasing Circuits of MOSFET

3.3.1 Biasing of N-MOSFET By Fixing Voltage V_{GS}

The biasing of an enhancement type N-MOSFET by fixing voltage V_{GS} is shown in Fig. 4. This circuit has separate arrangement for base and collector circuit.

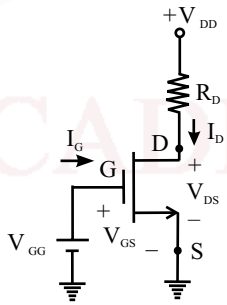


Fig. 4 Biasing of Enhancement MOSFET by Fixing V_{GS}

The gate terminal of MOSFET is isolated from channel by oxide layer so current in gate terminal is zero.

$\therefore \quad I_G = 0$

From above circuit, $V_{GS} = V_{GG}$ (10)

Applying KVL in the drain circuit, we have,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D R_D \tag{11}$$

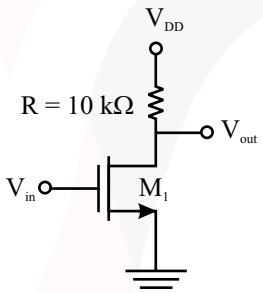
The drain current for saturation region is given by,

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 \tag{12}$$

$$\Rightarrow \quad V_{DS} = V_{DD} - \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 R_D \tag{13}$$

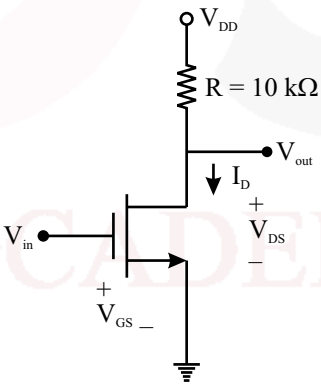
Example 1

For the MOSFET M_1 shown in the figure, assume W/L = 2, V_{DD} = 2.0 V, $\mu_n C_{ox}$ = 100μA/V² and V_{TH} = 0.5 V. The transistor M_1 switches from saturation region to linear region when V_{in} (in volts) is_____.



GATE(EC-III/2014/2 M)

Solution : Ans.(1.4 to 1.6)



Given, $\frac{W}{L} = 2, V_{DD} = 2V, \mu_n C_{ox} = 100\ \mu A/V^2, V_{TH} = 0.5$

Drain current for saturation region is given by

$$I_D = \frac{1}{2}\mu_n C_{ox} \cdot \frac{W}{L}(V_{GS} - V_{TH})^2$$

From gate circuit,

$$V_{GS} = V_{in} - 0 = V_{in}$$

$$\therefore \quad I_D = \frac{1}{2}\times 100\times 10^{-6}\times 2\left(V_{in}-0.5\right)^2$$

$$\Rightarrow \quad I_D = 10^{-4}\,(V_{in}-0.5)^2$$

Applying KVLin the drain circuit,

$$V_{DD} - I_D R - V_{DS} = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D R$$

$$\Rightarrow \quad V_{DS} = 2 - 10^{-4}(V_{in} - 0.5)^2\times 10\times 10^3$$

$$\Rightarrow \quad V_{DS} = 2 - (V_{in} - 0.5)^2 \qquad \text{....(i)}$$

MOSFET operation changes from the saturation region to linear region at,

$$V_{DS} = V_{GS} - V_{TH}$$

$$\Rightarrow \quad V_{DS} = V_{in} - V_{TH} = V_{in} - 0.5 \qquad \text{....(ii)}$$

From (i) and (ii), we have,

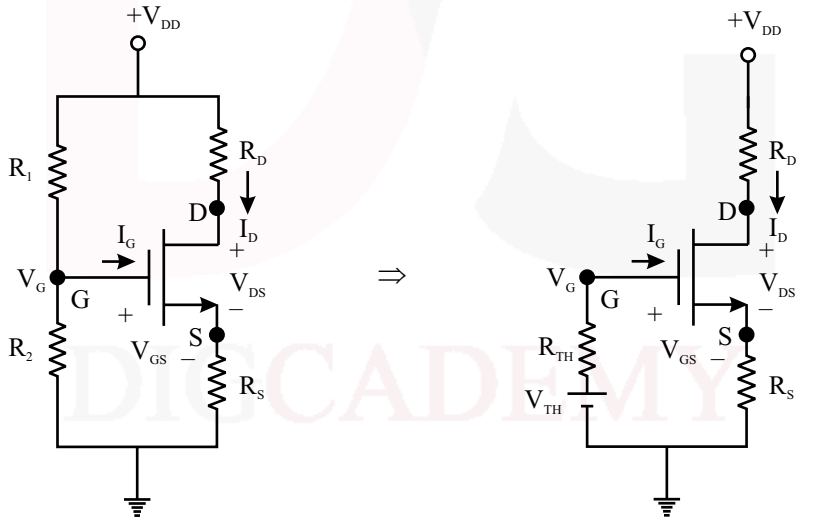
$$2 - (V_{in} - 0.5)^2 = V_{in} - 0.5$$

$$\Rightarrow \quad V_{in}^{\ 2} - 2.25 = 0$$

$$\Rightarrow \quad V_{in} = 1.5\ V$$

3.3.2 Biasing of N-MOSFET with Potential Divider

Fig.5 shows the biasing of enhancement n-channel MOSFET using a potential divider bias. The potential divider provides a fixed biasing voltage at gate terminal of the MOSFET.



(a) Potential divider bias circuit (b) Equivalent circuit of potential divider

Fig. 5 Biasing of Enhancement MOSFET with potential divider bias

The Thevenin's equivalent voltage and resistance of potential divider are given by,

$$V_{TH} = \frac{R_2}{R_1 + R_2}\cdot V_{DD} \qquad (14)$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \qquad (15)$$

The gate current of MOSFET is zero. Therefore, voltage at gate can be given as,

$$V_G = V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD} \tag{16}$$

From the gate circuit, $V_G = V_{GS} - I_D R_S$ (17)

Applying KVL in drain circuit, we have,

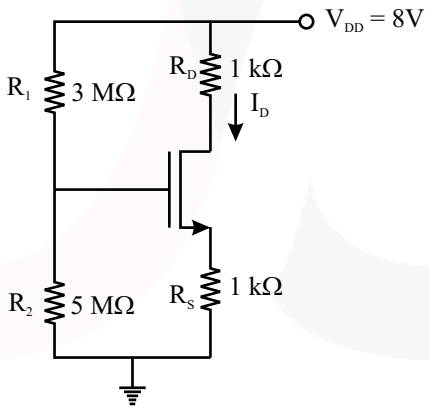
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D (R_D + R_s) \tag{18}$$

The drain current in above equation can be replaced by expression given by equation (6).

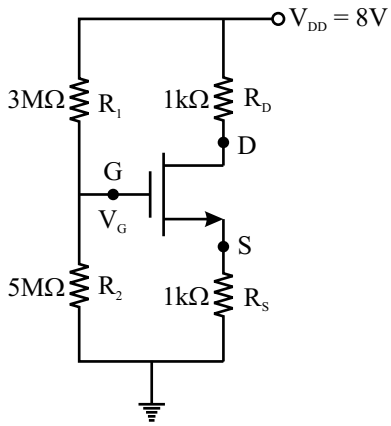
Example 2

For the circuit shown, assume that the NMOS transistor is in saturation. Its threshold voltage V_{tn} = 1V and its transconductance parameter $\mu_n C_{ox}\left(\frac{W}{L}\right) = 1\text{mA}/\text{V}^2$. Neglect channel length modulation and body bias effects. Under these conditions, the drain current I_D in mA is _____.



GATE(EC-I/2017/2 M)

Solution: Ans. (1.9 to 2.1)

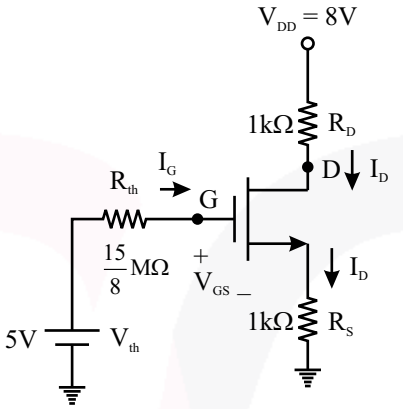


The potential divider of circuit can be replaced by its Thevenin's equivalent as under,

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{5}{3+5} \times 8 = 5V$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R} = \frac{3 \times 5}{3+5} = \frac{15}{8} M\Omega$$

The circuit can be redrawn as under



Gate current is zero for MOSFET.

$\therefore \quad I_G = 0$

Applying KVL in gate circuit, we have,

$$V_{th} - V_{GS} - I_D R_s = 0$$

$$\Rightarrow \quad V_{GS} = V_{th} - I_D R_s$$

$$\Rightarrow \quad V_{GS} = 5 - 1 \times 10^3 I_D \qquad \text{.....(i)}$$

The drain current of MOSFET for saturation region is given by,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \qquad \text{.....(ii)}$$

Given, $\frac{\mu_n C_{ox} W}{L} = 1mA/V^2, \; V_T = V_{tn} = 1V$

$$\Rightarrow \quad I_D = \frac{1}{2} \times 10^{-3} (V_{GS} - 1)^2$$

Putting expression of V_{GS} from (i) in above equation, we have,

$$I_D = \frac{1}{2} \times 10^{-3} (5 - 10^3 I_D - 1)^2$$

If drain current is taken in mA then above equation can be modified as,

$$I_D = \frac{1}{2} (5 - I_D - 1)^2$$

$\Rightarrow \quad I_D^2 - 10I_D + 16 = 0$

$\Rightarrow \quad I_D = 2 \text{ mA} \& 8 \text{ mA}$

If drain current I_D is 8 mA then voltage gate to source voltage V_{GS} becomes –3 V. In that case the MOSFET will not operate in saturation region.

$\therefore \quad I_D = 2 \text{ mA}$

3.3.3 Biasing of N-MOSFET with Feedback Configuration

Fig.6 shows the biasing arrangement of enhancement n-channel MOSFET using a feedback from drain terminal of the MOSFET.

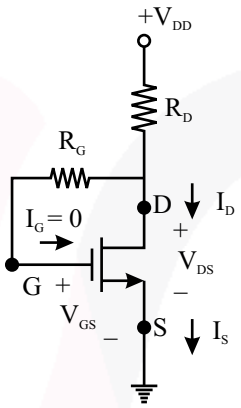


Fig. 6 Biasing of Enhancement N-MOSFET with drain feedback bias

The gate current in MOSFET is zero, therefore, the voltage drop across the feedback resistor R_G is zero and voltage at gate terminal is same as the voltage at drain terminal. Thus the circuit can also be drawn by replacing resistor R_G by short circuit as shown in Fig.7

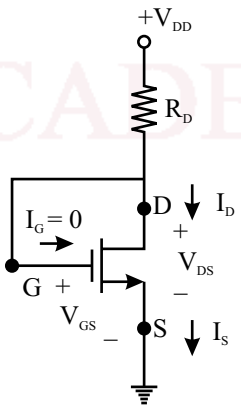


Fig. 7 Equivalent circuit of drain feedback bias

From gate circuit of Fig. 7, we have,

$$V_G = V_D \quad (19)$$

$$\therefore \quad V_{GS} = V_{DS} \quad (20)$$

If $V_{GS} = V_{DS}$ then $V_{DS} > V_{GS} - V_T$ and MOSFET works in saturation region.

Applying KVL in the drain circuit, we have,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D R_D \qquad (21)$$

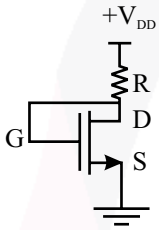
From equations (20) and (21), we have,

$$V_{GS} = V_{DD} - I_D R_D \qquad (21a)$$

The drain current in above equation can be replaced by expression given by equation (6).

Example 3

For the n-channel MOS transistor shown in the figure, the threshold voltage V_{Th} is 0.8 V. Neglect channel length modulation effects. When the drain voltage $V_D = 1.6$ V, the drain current I_D was found to be 0.5 mA. If V_D is adjusted to be 2V by changing the values of R and V_{DD}. the new value of I_D (in mA) is

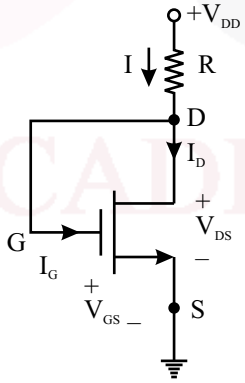


(a) 0.625 (b) 0.75

(c) 1.125 (d) 1.5

GATE(EC-II/2014/2M)

Solution : Ans.(c)



From above circuit, $V_{DS} = V_{GS} = V_D$

$\therefore \quad V_{DS} > V_{GS} - V_T$

MOSFET Operates in saturation region when $V_{DS} > V_{GS} - V_T$.

The drain current for saturation region is given by,

$$I_D = \frac{k_n}{2}\frac{W}{L}(V_{cs} - V_T)^2 = K\,(V_{GS} - V_T)^2$$

Case-I when $V_D = V_{DS} = V_{GS} = 1.6V$

$$I_D = 0.5 \text{ mA}$$

$$0.5\times 10^{-3} = K(1.6 - 0.8)^2$$

$$K = \frac{0.5}{0.64}\times 10^{-3}$$

Case-II when $V_D = V_{DS} = V_{GS} = 2V$

$$I_D = \frac{0.5\times 10^{-3}}{0.64}(2 - 0.8)^2$$

$$\Rightarrow \quad I_D = 1.125 \text{ mA}$$

3.3.4 Biasing of N-MOSFET with Two Power Supplies

Fig.8 shows the biasing of enhancement n-channel MOSFET using separate power supplies for drain and source terminal.

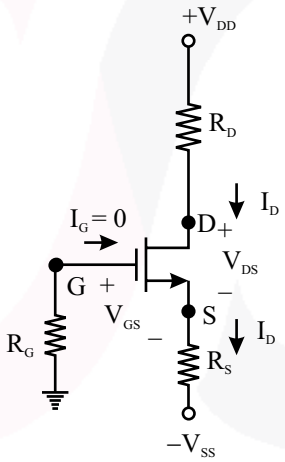


Fig. 8 Biasing of Enhancement N-MOSFET with drain feedback bias

The gate current in MOSFET is zero, therefore, the voltage drop across the resistor R_G is zero. So, the source current is also same as the drain current. Applying KVL in the gate circuit, we have,

$$-V_{GS} - I_D R_S + V_{SS} = 0 \quad (22)$$

$$\therefore \quad V_{GS} = V_{SS} - I_D R_S \quad (23)$$

Applying KVL in the drain circuit, we have,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D (R_D + R_S) \quad (24)$$

The drain current in above equation can be replaced by expression given by equation (6).

3.3.5 Biasing of N-MOSFET with a Constant Current Source

The biasing of a enhancement type n-channel MOSFET with a constant current source series with

source terminal is shown in Fig.9.

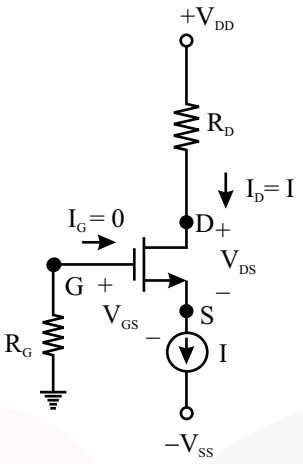


Fig. 9 Biasing of enhancement MOSFET with drain feedback bias

The constant current source is implemented using a current mirror circuit which will be discussed latter in compound circuits.

3.3.6 Biasing of P-MOSFET

N-MOSFET is preferred over the P-MOSFET due to its better frequency response of on account higher mobility of electrons. However, a simple biasing circuit of a P-MOSFET has been discussed in this topic to make better understanding of biasing of P-MOSFET. Fig.10 shows the biasing of enhancement p-channel MOSFET by connecting biasing voltage at the source terminal.

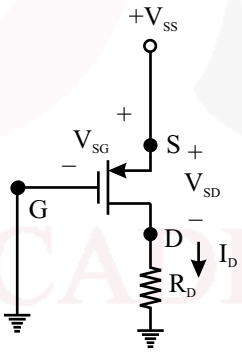


Fig. 10 Biasing of Enahancement P-MOSFET

The gate current in MOSFET is zero. So, the source current is also same as the drain current.

From above circuit, $V_{SG} = V_{SS} - 0 = V_{SS}$ (25)

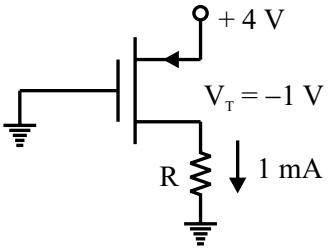
Applying KVL in the drain circuit, we have,

$$V_{SS} - V_{SD} - I_D R_D = 0$$

$$\Rightarrow \quad V_{SD} = V_{SS} - I_D R_D \qquad (26)$$

Example 4

The value of R for which the PMOS transistor in figure will be biased in linear region is

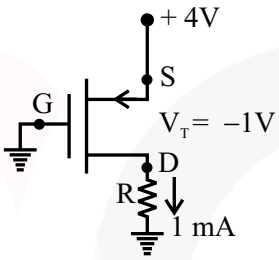


(a) 220 Ω (b) 470 Ω

(c) 680 Ω (d) 1200 Ω

GATE(EE/2004 /2 M)

Solution: Ans.(d)



From above circuit,

$$V_D = I_D R = 1R = R$$

Also,
$$V_{SD} = V_S - V_D = 4 - R \quad \text{.....(i)}$$
$$V_{SG} = V_S - V_G = 4 - 0 = 4V \quad \text{....(ii)}$$

A PMOS is biased in linear region, when,

$$V_{SD} \le V_{SG} - |V_T| \quad \text{....(iii)}$$

Threshold voltage V_T is negative for PMOS.

Given, $V_T = -1$ .....(iv)

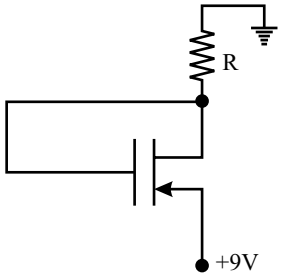
Putting value of V_{SD}, V_{SD} and V_T from (i), (ii) and (iv) in equation (iii), we have,

$$4 - R \le 4 - |-1|$$
$$\Rightarrow \quad 4 - R \le 3$$
$$\Rightarrow \quad R \ge 4 - 3$$
$$\Rightarrow \quad R \ge 1\ k\Omega$$

Among the given options R = 1200 Ω satisfies the above condition.

Example 5

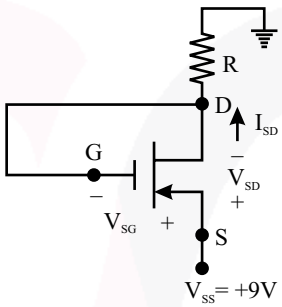
The PMOSFET circuit shown in the figure has $V_{TP} = -1.4$ V, $K_P = 25\ \mu A/V^2$, L = 2 μm, λ = 0. If $I_{DS} = -0.1$ mA and $V_{DS} = -2.4$V then the width of channel W and R are respectively.



(a) 16 μm and 66 kΩ
(b) 18 μm and 33 kΩ
(c) 16 μm and 33 kΩ
(d) 18 μm and 66 kΩ

IES(E&T,16)

Solution: Ans.(a)



The voltages V_{DS}, V_{GS} and current I_{DS} are negative and V_{SD}, V_{SG} and current I_{SD} are positive for a PMOSFET .

When the drain terminal of MOSFET is shorted with gate terminal the MOSFET works in saturation region. The drain current of PMOSFET for saturation region is can be given by,

$$I_{SD} = \frac{1}{2}K_p\frac{W}{L}(V_{SG} - |V_{TP}|)^2$$

Given, $V_{TP} = -1.4$ V, $K_P = 25\ \mu A/V^2$, $L = 2\ \mu m$, $\lambda = 0$, $I_{DS} = -0.1$ mA and $V_{DS} = -2.4$V

The source to drain voltage, $V_{SD} = -V_{DS} = -(-2.4)V = 2.4$ V

The source to drain current, $I_{SD} = -I_{DS} = -(-0.1)$ mA $= 0.1$ mA

Since drain is shorted with gate terminal,

$$\therefore \quad V_{SG} = V_{SD} = 2.4V$$

Putting above values in expression of drain current, we have,

$$0.1\times10^{-3} = \frac{25\times10^{-6}}{2}\frac{W}{2\times10^{-6}}(2.4-1.4)^2$$

$$\Rightarrow \quad W = 16\ \mu m$$

Voltage at drain terminal, $V_D = V_{SS} - V_{SD} = 9 - 2.4 = 6.6$ V

Voltage at drain terminal is related to source to drain current as under,

$$V_D = RI_{SD}$$

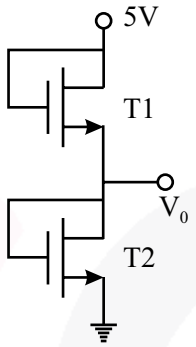
$$\Rightarrow \quad 6.6 = R\ (0.1\times 10^3)$$

$\Rightarrow$ $R = 66\ k\Omega$

3.3.7 Examples on Biasing of Combination of MOSFETs

Example 6

Both transistors T1 and T2 shown in the figure, have a threshold voltage of 1 Volts. The device parameters K_1 and K_2 of T1 and T2 are, respectively, 36 $\mu A/V^2$ and 9 $\mu A/V^2$. The output voltage V_0 is

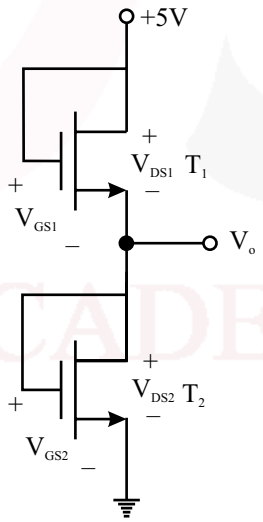


(a) 1 V (b) 2 V

(c) 3 V (d) 4 V

GATE(EC/2005/2M)

Solution : Ans.(c)



For both MOSFETs, $V_{GS} = V_{DS}$

So, $V_{DS} > V_{GS} - V_T$..

When $V_{DS} > (V_{GS} - V_T)$ MOSFET Work in saturation region. The drain current for saturation region as

$$I_D = K(V_{GS} - V_T)^2$$

Where K is parameter of MOSFET.

As both MOSFET are connected in series, therefore,

$$I_{D1} = I_{D2}$$

$$\Rightarrow K_1(V_{GS1} - V_{T1})^2 = K_1(V_{GS2} - V_{T2})^2$$

Given, $K_1 = 36\ \mu A/V^2$, $K_2 = 9\ \mu A/V^2$, $V_{T1} = V_{T2} = 1\ V$

Also from given circuit,

$$V_{GS1} = V_{DS} = 5 - V_0$$

$$V_{GS2} = V_{DS2} = V_0$$

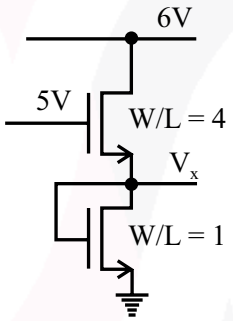
$$\Rightarrow 36(5 - V_0 - 1)^2 = 9(V_0 - 1)^2$$

$$\Rightarrow 2(4 - V_0) = V_0 - 1$$

$$\Rightarrow V_0 = 3\ V$$

Example 7

In the circuit shown below, for the MOS transistors, $\mu_n C_{ox} = 100\ \mu A/V^2$ and the threshold voltage V_T is 1 V. The voltage V_X at the source of the upper transistor is

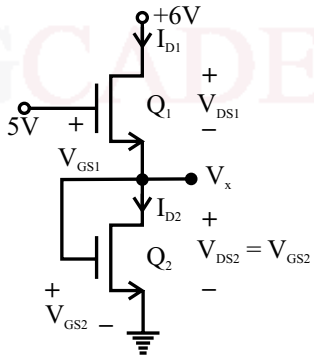


(a) 1 V (b) 2 V

(c) 3 V (d) 3.67 V

GATE(EC/2011/2M)

Solution : Ans.(c)



MOSFET Q1:

$$V_{DS1} = 6 - V_x\ ;\ V_{GS1} = 5 - V_x$$

$$V_{GS1} - V_T = 5 - V_x - 1 = 4 - V_x$$

$$\Rightarrow V_{DS1} > V_{GS1} - V_T$$

MOSFET operates in saturation when $V_{DS} > V_{GS} - V_T$

So, MOSFET Q_1 is operating in saturation region with drain current,

$$I_{D1} = \frac{kW}{L}(V_{GS1} - V_T)^2$$

where, $$K = \frac{\mu_n C_{ox}}{2}$$

Given, $\mu_n C_{ox} = 100\ \mu A/V^2$, $\frac{W}{L} = 4$, $V_T = 1\ V$

$$\therefore \quad I_D = \frac{100}{2} \times 4\ (V_{GS1} - 1)^2\ \mu A$$

$$\Rightarrow \quad I_{D1} = 50 \times 4\ (5 - V_x - 1)^2$$

$$\Rightarrow \quad I_{D1} = 200\ (4 - V_x)^2 \qquad .....(i)$$

MOSFET Q_2:

$$V_{DS2} = V_{GS2} = V_x\ ;$$

$$V_{GS2} - V_T = V_x - 1$$

$$\Rightarrow \quad V_{DS2} > V_{GS2} - V_T$$

So, MOSFET Q_2 is also operating in saturation region with drain current,

$$I_{D2} = \frac{kW}{L}(V_{GS2} - V_T)^2$$

For MOSFET Q_2, $$\frac{W}{L} = 1$$

$$\Rightarrow \quad I_{D2} = 50 \times 1\ (V_x - 1)^2$$

As both MOSFETS are in series, therefore,

$$I_{D1} = I_{D2}$$

$$\Rightarrow \quad 200\ (4 - V_x)^2 = 50(V_x - 1)^2$$

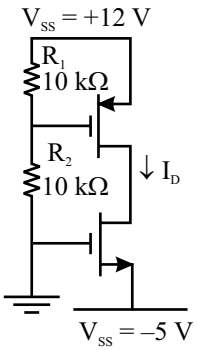
$$\Rightarrow \quad 2\ (4 - V_x) = V_x - 1$$

$$\Rightarrow \quad 3V_x = 9$$

$$\Rightarrow \quad V_x = 3V$$

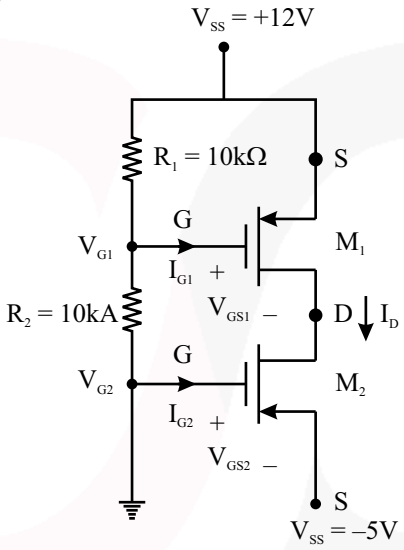
Example 8

For the MOSFETs shown in the figure, the threshold voltage $|V_t| = 2$ V and $k = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right) = 0.1$ mA/V^2. The value of I_D (in mA) is_____.



GATE(EC-II/2014/2 M)

Solution : Ans.(0.88 to 0.92)



For MOSFETs, $I_{G1} = 0$ and $I_{G2} = 0$

Voltage at gate of NMOS,

$$V_{GS2} = 0 - (-5) = 5V$$

For above circuit, the drain current is same for both NMOS & PMOS. The drain current for NMOS can be given as,

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS2} - V_t\right)^2$$

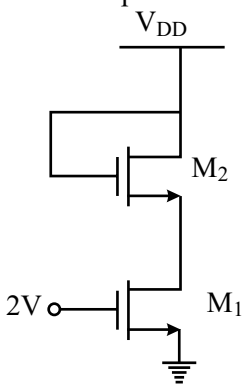
Given, $\frac{\mu_n C_{ox} W}{2L} = 0.1\ mA/V^2$ & $V_t = 2V$

$$\Rightarrow \quad I_D = 0.1 \times 10^{-3}\,(5-2)^2 = 0.9\ mA$$

Example 9

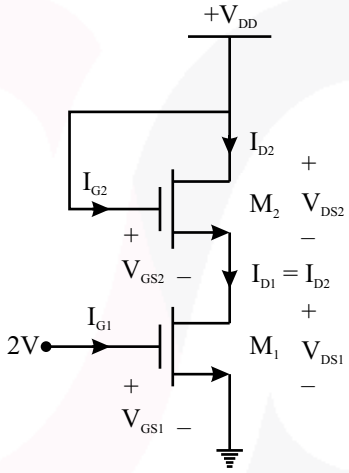
In the circuit shown, both the enhancement mode NMOS transistors have the following characteristics: $k_n = \mu_n C_{ox}\left(\frac{W}{L}\right) = 1\frac{mA}{V^2}$; $V_{TN} = 1V$. Assume that the channel length modulation parameter λ is zero and body is shorted to source. The minimum supply voltage V_{DD} (in volts) needed to ensure that

transistor M_1 operates in saturation mode of operation is .....



GATE(EC-III/2015/2 M)

Solution : **Ans. (2.9 to 3.1)**



Minimum drain to source voltage required for operating a NMOSFET in saturation region is given, by,

$$V_{DS} = V_{GS} - V_{TN}$$

Given, $V_{TN} = 1V$ for both MOSFETs

For MOSFET M_1, $V_{DS1} = V_{GS1} - V_{TN}$

From given circuit, $V_{GS1} = 2 - 0 = 2\ V$

$\Rightarrow$ $V_{DS1} = 2 - 1 = 1\ V$

Applying KVL in drain circuit of both MOSFETs we have,

$$V_{DD} - V_{DS2} - V_{DS1} = 0$$

$\Rightarrow$ $V_{DS2} = V_{DD} - V_{DS1} = V_{DD} - 1$

Since drain of M_2 is shorted with gate terminal, therefore,

$$V_{GS2} = V_{DS2}$$

$\Rightarrow$ $V_{GS2} = V_{DD} - V_{DS1} = V_{DD} - 1$

The drain current of a MOSFET for saturation region is given by

$$I_D = \frac{1}{2}\cdot\mu_n C_{ox}\cdot\frac{W}{L}\left(V_{GS} - V_{TN}\right)^2$$

Gate current for MOSFETs, $I_G = 0$

If both MOSFETs work in saturation region then

$$\therefore \quad I_{D1} = I_{D2} = I_D$$

$$\Rightarrow \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS1} - V_{TN}\right)^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS2} - V_{TN}\right)^2$$

$$\Rightarrow \quad V_{GS1} - V_{TN} = V_{GS2} - V_{TN}$$

$$\Rightarrow \quad 2 - 1 = (V_{DD} - 1) - 1$$

$$\Rightarrow \quad V_{DD} = 3V$$

3.4 Biasing Circuits of JFET

The concept of operating point and load line of JFET is exactly similar to that of a MOSFET amplifier circuit. The gate current of JFET is also zero and the drain current is given by,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{27}$$

When V_P is pinch of voltage of JFET and I_{DSS} is drain current when gate terminal is shorted with source terminal i.e. $V_{GS} = 0$.

3.4.1 Fixed Bias Configuration of JFET

The source terminal is directly connected to ground in a fixed bias circuit. Fig. 11 shows the fixed biased circuit of n-channel JFET.

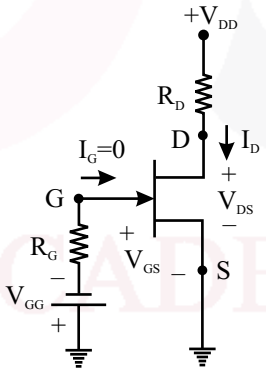


Fig. 11 Fixed biased circuit of n-channel JFET

The gate current in JFET is assumed to zero. Therefore, the voltage drop across the resistance R_G is zero.

$$\therefore \quad V_{GS} = -V_{GG} \tag{28}$$

Applying KVL in collector circuit, we have,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D R_D \tag{29}$$

Putting expression of V_{GS} from equation (26) the drain current of JFET in fixed bias circuit becomes,

$$\Rightarrow \quad I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1+\frac{V_{GG}}{V_P}\right)^2 \tag{30}$$

3.4.2 Self Bias Configuration of JFET

A self biased circuit if JFET consists of a resistance in series with the source terminal of JFET. This resistance provides a negative feedback in the input gate circuit of the amplifier.

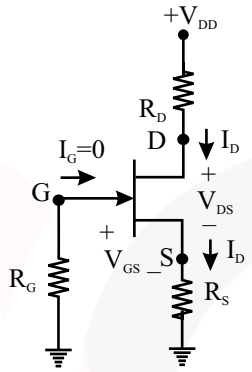


Fig. 12 Self biased circuit of n-channel JFET

Voltage at source terminal,

$$V_S = R_s I_D \tag{31}$$

Gate to source voltage,

$$V_{GS} = V_G - V_S = V_G - R_S I_D \tag{32}$$

Since gate current of JFET is zero, so, voltage drop across R_G is zero. Then the voltage at gate terminal is also zero.

$$\therefore \quad V_G = 0$$

$$\Rightarrow \quad V_{GS} = -R_S I_D \tag{33}$$

Applying KVL in drain circuit, we have,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D(R_D \ R_S) \tag{34}$$

By putting the expression of V_{GS} from equation (33) in equation (27), the drain current of JEFT becomes as,

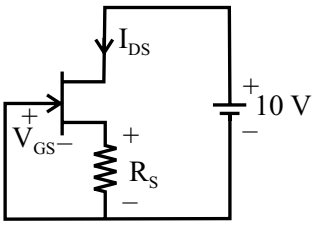
$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1-\frac{(-I_D R_S)}{V_P}\right)^2 \tag{35}$$

$$\Rightarrow \quad I_D = I_{DSS}\left(1+\frac{I_D R_S}{V_P}\right)^2 \tag{36}$$

Above equation can be solved for obtaining the drain current, I_D of the JFET.

Example 10

The JFET in the circuit shown in figure has an I_{DSS} = 10 mA and V_p = –5 V. The value of the resistance R_s for a drain current I_{DS} = 6.4 mA is (select the nearest value)

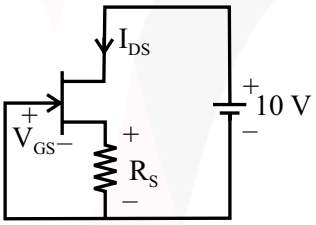


(a) 150 ohms (b) 470 ohms

(c) 560 ohms (d) 1 kilo ohm.

GATE(EC/1992/2M)

Solution : Ans.(a)



Given, $I_{DSS} = 10\ mA, V_P = -5V, I_{DS} = 6.4\ mA$

The drain current of JFET is given by,

$$I_{DS} = I_{DSS}\left[1-\frac{V_{GS}}{V_t}\right]^2$$

$$\Rightarrow \quad 6.4\times10^{-3} = 10\times10^{-3}\left[1-\frac{V_{GS}}{-5}\right]^2$$

$$\Rightarrow \quad 1-\frac{V_{GS}}{(-5)} = \sqrt{0.64}$$

$$\Rightarrow \quad \frac{V_{GS}}{5} = 0.8-1 = -0.2\ V$$

$$\Rightarrow \quad V_{GS} = -1V$$

From gate - source circuit,

$$V_{GS} + I_D R_S = 0$$

$$\Rightarrow \quad V_{GS} = -I_D R_S$$

$$\Rightarrow \quad R_S = \frac{-1.0}{-6.4}\times1000\,\Omega = \frac{10000}{64} = \frac{1250}{8} = 156.25\ \Omega$$

So, nearest value of R_s is 150 Ω. .

3.4.3 Potential Divider Bias Configuration of JFET

The potential divider bias configuration of JFET is shown in Fig. 13. The potential divider is used to supply bias voltage to the gate terminal of the JFET.

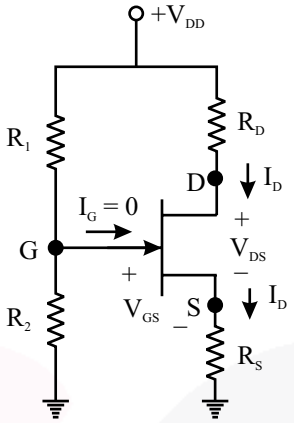


Fig. 13 Potential divider bais configuration of n-channel JFET

Voltage at source terminal,

$$V_S = R_s I_D \tag{37}$$

Since the gate current of JFET is zero, therefore, the voltage at the gate terminal can be given obtained by applying voltage divider rules as under,

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD} \tag{38}$$

Gate to source voltage,

$$V_{GS} = V_G - V_S = V_G - I_D R_S \tag{39}$$

Applying KVL in drain circuit, we have,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\Rightarrow \quad V_{DS} = V_{DD} - I_D (R_D + R_S) \tag{40}$$

Note : i. The biasing circuits of depletion type n-channel MOSFET are similar to JFET and the drain current is given by

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_t}\right]^2 \tag{41}$$

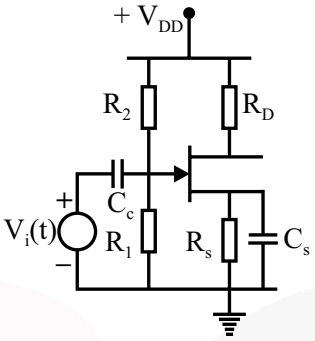
Where V_t is the pinch off voltage or threshold voltage and I_{DSS} is drain current when drain is shorted with the source terminal of MOSFET.

ii. The current I_{DSS} for depletion type n-channel MOSFET is given by,

$$I_{DSS} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_t^2 \tag{41a}$$

Example 11

For the circuit shown in figure I_{DSQ} (in mA) and V_{GSQ} (in V) are related through $2I_{DSQ} = (4 + V_{GSQ})^2$. The following data is given: $V_{DD} = 15$ V, $R_1 = 1.0$ MΩ, $R_2 = 6.5$ MΩ, $R_D = 2.0$ kΩ, $R_S = 1.0$ kΩ, $I_{DSS} = 8$mA. The value I_{DSQ}, assuming the gate current, is negligible, is approximately equal to

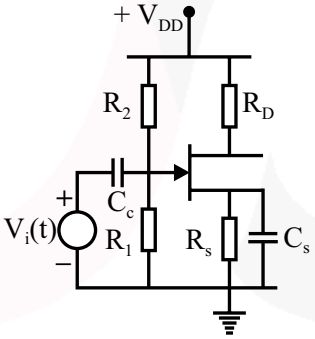


(a) 5 mA (b) 2.0 nA

(c) 2.3 μ A (d) 3.4 mA

GATE(IN/2005/2M)

Solution : Ans.(b)

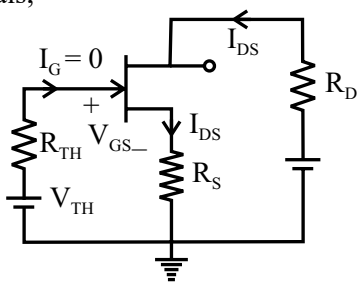


Given, $R_1 = 1\ \text{M}\Omega$, $R_2 = 6.5\ \text{M}\Omega$, $R_D = 2\ \text{k}\Omega$, $R_S = 1\ \text{k}\Omega$, $V_{DD} = 15$ V

and $2I_{DSQ} = (4 + V_{GSQ})^2$

$$\Rightarrow \quad I_{DSQ} = \frac{1}{2}(4 + V_{GSQ})^2 \qquad \text{.....(i)}$$

For DC analysis of amplifier the coupling and bypass capacitors are replaced by open circuits. Then equivalent circuit for DC signals,



where, $$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{1 \times 6.5}{1 + 6.5} = \frac{13}{15} M\Omega$$

$$V_{TH} = \frac{R_1}{R_1 + R_2} V_{DD} = \frac{1}{1 + 6.5} \times 15 = 2V \quad ...(ii)$$

Since gate current is negligible, so, current in source resistance R_S is same as I_{DS} and drop in R_{TH} is negligible, For gate circuit,

$$V_{TH} - V_{GSQ} = R_D I_{DSQ}$$

Putting V_{TH} and I_{DSQ} from (i) and (ii) in the above equation, we have,

$$\Rightarrow \quad 2 - V_{GSQ} = 2 \times \frac{1}{2}(4 - V_{GSQ})^2$$

$$\Rightarrow \quad 2 - V_{GSQ} = (4 - V_{GSQ})^2$$

$$\Rightarrow \quad 2 - V_{GSQ} = 16 + 8V_{GSQ} + V_{GSQ}^2$$

$$\Rightarrow \quad V_{GSQ}^2 + 9 V_{GSQ} + 14 = 0$$

$$\Rightarrow \quad V_{GSQ} = -2V, -7V$$

$$\therefore \quad I_{DSQ} = \frac{1}{2}(4-2)^2 \approx 2\,mA$$

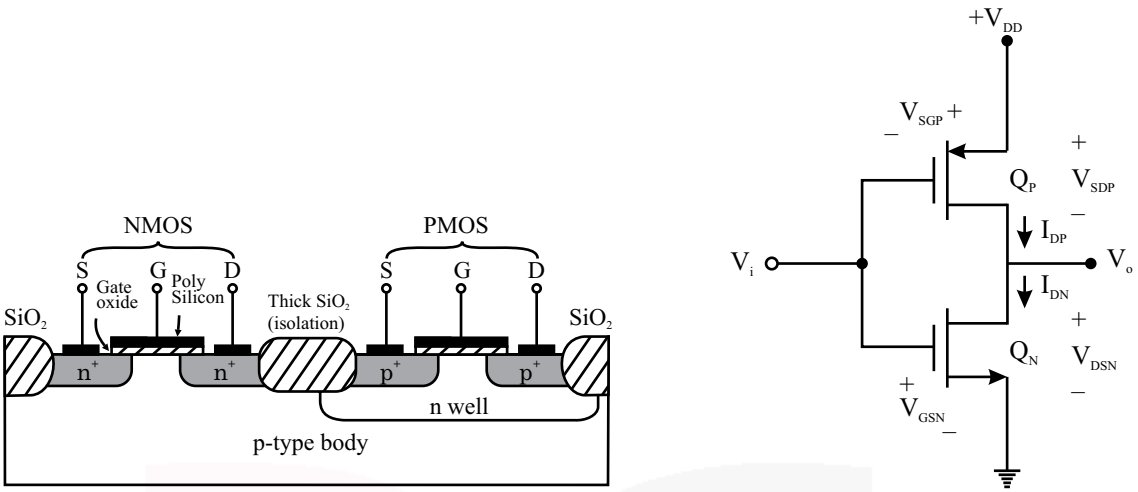
or $$I_{DSQ} = \frac{1}{2}(4-7)^2 \approx 4.5\,mA$$

3.5 Complementary MOS (CMOS) Logic Inverter

A CMOS is most widely used technology used in analog and digital circuit design. It has almost replaced the NMOS due to its inherent advantages like low power dissipation and high driving capability.

3.5.1 Construction of CMOS

A CMOS consists two matched enhancement n-channel (Q_N) and p-channel (Q_P) MOSFETs fabricated on same p-type substrate as shown in Fig.14a. The p-channel MOSFET or PMOS is fabricated on p-substrate in a specially created n-region called n-well. Both NMOS and PMOS transistors are separated from each other by a thick oxide layer that functions as an insulator. The source terminal of NMOS is connected to p-substrate body and source of PMOS is connected to n-well so that no body effect is observed. Fig. 14b shows the circuit of a CMOS inverter. Input signal is common to both NMOS and PMOS and output is taken from common drain terminals of both NMOS and PMOS as shown in Fig. 14b.



(a) Cross-section of CMOS (b) CMOS inverter circuit

Fig. 14 CMOS cross-section and inverter circuit

3.5.2 Circuit Operation of CMOS Inverter

Two levels of input voltage $V_i = 0$ and $V_i = V_{DD}$ will be considered for understanding of the operation of CMOS circuit shown in Fig. 14b. The transistors in CMOS inverter are used as switches. They are operated either in cutoff or ohmic region of operation. The lower NMOS transistor, Q_N , is assumed to be driving transistor and upper PMOS transistor, Q_P , is assumed to be the load. Let the magnitude of supply voltage (V_{DD}) is more than twice the magnitude of threshold voltage (V_T) of each MOSFET. For the CMOS circuit shown above,

$$V_o = V_{DSN}$$

or

$$V_o = V_{DD} - V_{DSP}$$

Case-I : When $V_i = V_{DD}$

Then

$$V_{SGP} = V_{DD} - V_i = V_{DD} - V_{DD} = 0$$

$$V_{GSN} = V_i - 0 = V_{DD} - 0 = V_{DD}$$

As V_{SGP} is zero which is definitely less than $|V_{TP}|$ and V_{GSN} is equal to V_{DD} which is more than V_{TN}, so transistor Q_P is OFF and transistor Q_N is ON. When Q_P is OFF and Q_N is ON, the output terminal of CMOS is connected to ground due to which V_{DSN} is small. The transistor Q_N operates in ohmic region due to small value of V_{DSN} and high value of V_{GSN} (= V_{DD}) and Q_P in cutoff. The resistance offered by Q_N is given by,

$$r_{DSN} = \frac{1}{\mu_n C_{ox} \cdot \frac{W}{L}(V_{GSN} - V_{TN})} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TN})} \quad (42)$$

The circuit diagram, I_DVs V_o curve and equivalent circuit for $V_i = V_{DD}$ are shown in Fig.15.

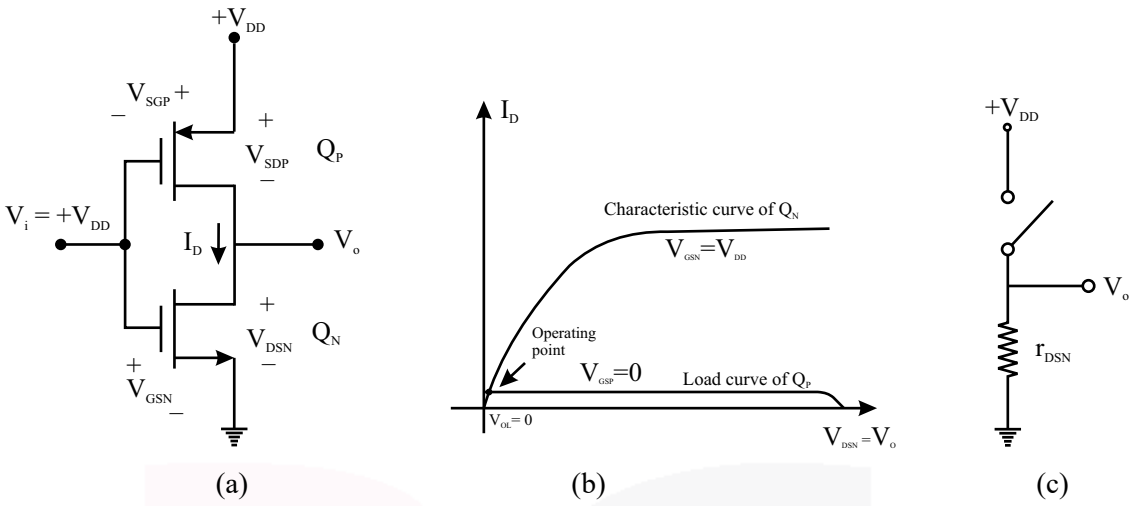


Fig. 15 (a) CMOS Circuit at $V_i = V_{DD}$ (b) I_D Vs V_o curve (c) Equivalent circuit

The load curve of Q_P is a straight line near $I_D = 0$ because transistor Q_P is off. Since both MOSFETs of CMOS inverter have same current so the intersection of characteristic curve of NMOS and load curve of PMOS gives the operating point of CMOS. For the NMOS transistor the output voltage V_o is same as V_{GSN} so the I_D Vs V_o variation is same as drain characteristics of NMOS. Where as for the PMOS, the output voltage $V_o = V_{DD} - V_{SDP}$. So, the I_D Vs V_o variation curve is named as load curve which is a mirror image of drain characteristics of PMOS about a vertical line. So, the load curve of PMOS is derived from drain characteristics of PMOS only. As the current in the circuit is negligible therefore, the power dissipation is negligible.

Case-II : When $V_i = 0$

Then
$$V_{SGP} = V_{DD} - 0 = V_{DD}$$
$$V_{GSN} = V_i - 0 = 0 - 0 = 0$$

As V_{GSN} is zero which is less than V_{TN} and V_{SGP} is equal to V_{DD} which is more than $|V_{TP}|$ so transistor Q_N is OFF and transistor Q_P is ON. When Q_P is ON, the supply voltage is connected to output terminal through Q_P and voltage V_{SDP} is small. Thus transistor Q_P operates in ohmic region due to small value of V_{SDP} and small high value of V_{SGP} and Q_N in cutoff. The resistance offered by Q_P is given by,

$$r_{DSP} = \frac{1}{\mu_P C_{ox} \cdot \frac{W}{L}\left(V_{SGP} - |V_{TP}|\right)} = \frac{1}{\mu_P C_{ox} \frac{W}{L}\left(V_{DD} - |V_{TP}|\right)} \quad (43)$$

The circuit diagram, I_DVs V_o curve and equivalent circuit for $V_i = 0$ are shown in Fig.16. When $V_i = 0$, the NMOS is in cutoff and drain current of Q_N is zero. The I_D Vs V_o characteristics of NMOS is a straight line with negligible drain current. Load curve for Q_P is straight line showing large current for small value of V_o and with negative slope for large value of V_o as shown in figure 16b.

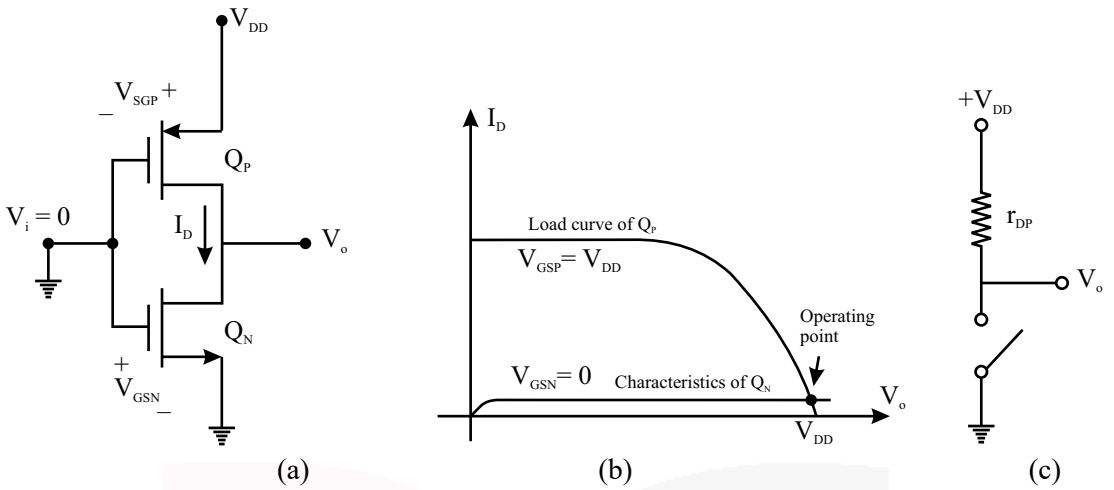


Fig. 16 (a) CMOS Circuit at $V_i = 0$ (b) I_D Vs V_o curve (c) Equivalent circuit

The intersection of two curves gives operating point Q with $V_o = V_{DD}$. The power dissipation is again negligible under static condition because drain current is negligible.

3.5.3 Voltage Transfer Characteristics of CMOS

The voltage transfer characteristics of CMOS gives variation of output voltage, V_o, when input voltage V_i is varied from 0 to V_{DD}. Fig.17 shows the voltage transfer characteristics curve of CMOS inverter.

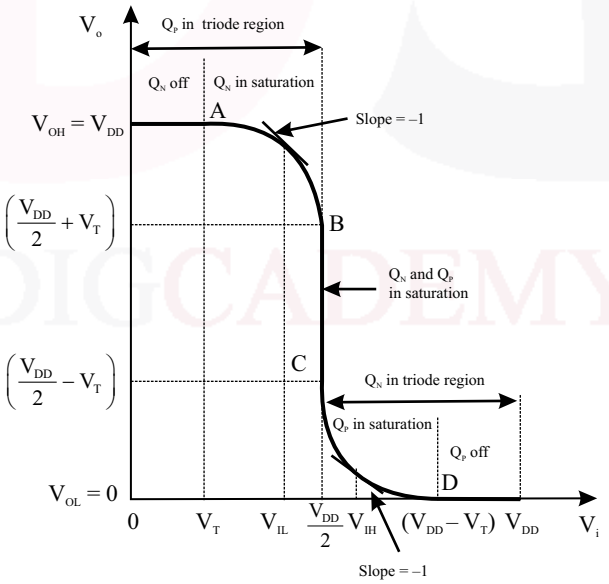


Fig.17 Voltage transfer characteristics curve of CMOS inverter

The CMOS is normally designed to have matched transistors with $|V_{TP}| = V_{TN} = V_T$ and $\mu_N C_{ox} \frac{W_n}{L_n} = \mu_P C_{ox} \frac{W_P}{L_P}$

Since mobility of electrons is 2 to 3 times the mobility of holes, therefore, width of p-channel, is kept 2 to 3 time the width of n-channel keeping same length of both channels.

$$\therefore \quad \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \tag{44}$$

Above condition enables the CMOS inverter to have symmetrical transfer characteristics and equal current driving capability in both directions.

The drain current of NMOS for operation in ohmic region can be given by

$$I_{DN} = \mu_n C_{ox} \cdot \frac{W}{L}\left[(V_{GSN} - V_{TN})V_{DSN} - \frac{1}{2}V_{DSN}^2\right] \; ; \; V_{DSN} \le V_{GSN} - V_{TN} \tag{45}$$

From the CMOS circuit voltages V_{GSN} and V_{DSN} can be written as,,

$$V_{GSN} = V_i$$

and $$V_{DSN} = V_o$$

The condition for operation of NMOS in ohmic region can be derived as under,

$$V_{DSN} \le V_{GSN} - V_{TN} \tag{46}$$

$$V_o \le V_i - V_{TN} \tag{47}$$

Putting above relations in equation (45), we have,

$$I_{DN} = \mu_n C_{ox} \cdot \frac{W}{L}\left[(V_i - V_{TN})V_o - \frac{1}{2}V_o^2\right] \; ; \; V_o \le V_i - V_{TN} \tag{48}$$

The drain current of NMOS for operation in saturation region can be given as,

$$I_{DN} = \frac{1}{2} \cdot \mu_n C_{ox} \cdot \frac{W}{L}(V_{GSN} - V_{TN})^2 \; ; \; V_{DSN} \ge V_{GSN} - V_{TN} \tag{49}$$

The condition for operation of NMOS in saturation region can be derived as under,

$$V_{DSN} \ge V_{GSN} - V_{TN} \tag{50}$$

$$V_o \ge V_i - V_{TN} \tag{51}$$

$$\Rightarrow \quad I_{DN} = \frac{1}{2} \cdot \mu_n C_{ox} \cdot \frac{W}{L}(V_i - V_{TN})^2 \; ; \; V_o \ge V_i - V_{TN} \tag{52}$$

The drain current of transistors PMOS for operation in ohmic region,

$$I_{DP} = \mu_p C_{ox} \cdot \frac{W}{L}\left[(V_{SGP} - |V_{TP}|)V_{SDP} - \frac{1}{2}V_{SDP}^2\right] ; V_{SDP} \le V_{SGP} - |V_{TP}|$$

(53)

From the CMOS voltages V_{SGP} and V_{SDP} can be written as,

$$V_{SGP} = V_{DD} - V_i \tag{54}$$

and $$V_{SDP} = V_{DD} - V_o \tag{55}$$

Then condition for operation of PMOS in ohmic region can be derived as under,

$$V_{SDP} \le V_{SGP} - |V_{TP}| \quad (56)$$

$$\Rightarrow \quad V_{DD} - V_o \le V_{DD} - V_i - |V_{TP}| \quad (57)$$

$$\text{or} \quad V_o \ge V_i + |V_{TP}| \quad (58)$$

Putting above relations in equation (53), we have,

$$\Rightarrow \; I_{DP} = \mu_p C_{ox} \cdot \frac{W}{L}\left[(V_{DD} - V_i - |V_{TP}|)(V_{DD} - V_o) - \frac{1}{2}(V_{DD} - V_o)^2\right] \; ; \; V_o \ge V_i + |V_{TP}| \quad (59)$$

The drain current of transistors PMOS for operation in saturation region can be given as,

$$I_{DP} = \frac{1}{2}\mu_p C_{ox} \cdot \frac{W}{L}(V_{SGP} - |V_{TP}|)^2 \quad ; \; V_{SDP} \ge V_{SGP} - |V_{TP}| \quad (60)$$

Then condition for operation of PMOS in saturation region can be derived as under,

$$V_{SDP} \ge V_{SGP} - |V_{TP}| \quad (61)$$

$$\Rightarrow \quad V_{DD} - V_o \ge V_{DD} - V_i - |V_{TP}| \quad (62)$$

$$\text{or} \quad V_o \le V_i + |V_{TP}| \quad (63)$$

$$\Rightarrow \quad I_{DP} = \frac{1}{2}\mu_p C_{ox} \cdot \frac{W}{L}(V_{DD} - V_i - |V_{TP}|)^2 \quad ; \; V_o \le V_i + |V_{TP}| \quad (64)$$

The transfer characteristics of CMOS inverter has five different segments which are discussed as follows,

Case-I : When $0 < V_i < V_T$

The gate to source voltage of NMOS of CMOS circuit,

$$V_{GSN} = V_i \quad (65)$$

For above range of input voltage the corresponding range of V_{GSN} becomes,

$$0 < V_{GSN} < V_T$$

For above range of V_{GSN}, the NMOS operates in cutoff region. Thus, the NMOS operates in cutoff region for $0 < V_i < V_T$.

When NMOS operates in cutoff region the current, $I_{DP} = I_{DN} = 0$.

Under such condition voltage drop across PMOS, $V_{SDP} = I_{DP} \times r_{DSP} = I_{DP} \times 0 = 0$

Output voltage of CMOS, $V_o = V_{DD} - V_{SDP} = V_{DD} - 0 = V_{DD}$

The source to gate voltage of PMOS,

$$V_{SGP} = V_{DD} - V_i \quad (66)$$

when $V_i = 0$, $V_{SGP} = V_{DD} - 0 = V_{DD}$

when $V_i = V_T$, $V_{SGP} = V_{DD} - V_T$

Range of V_{SGP} for given range on input voltage becomes,

$$V_{DD} - V_T < V_{SGP} < V_{DD} \quad (67)$$

Here the voltage V_{SGP} is more than threshold voltage with ideally zero voltage drop, V_{DSP}, from drain

to source. Under such condition the PMOS operates in ohmic region of operation behaving like a closed switch.

Case-II : When $V_T < V_i < \frac{V_{DD}}{2}$

As $V_{GSN} = V_i$, so, corresponding range of V_{GSN} becomes,

$$V_T < V_{GSN} < \frac{V_{DD}}{2} \tag{68}$$

The moment V_{GSN} becomes more than threshold voltage, the drain current of NMOS starts building up and voltage , V_{SDP} , ($= I_{DP} \times r_{DSP}$) starts increasing and output voltage V_o ($= V_{DD} - V_{SDP}$) starts decreasing from V_{DD}.

When the input voltage, $V_T < V_i < \frac{V_{DD}}{2}$, the NMOS operates in saturation region till output voltage is in the following range,

$$V_o > \frac{V_{DD}}{2} - V_T \tag{69}$$

The region of operation of PMOS for above range of input voltage can be derived by using equation (58).The PMOS operates in ohmic region till the output voltage has following range,

$$V_o > \frac{V_{DD}}{2} + V_T \tag{70}$$

Case-III : When $V_i = \frac{V_{DD}}{2}$

Then $$V_{SGN} = V_i = \frac{V_{DD}}{2} \tag{71}$$

and $$V_{SGP} = V_{DD} - V_i = V_{DD} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} \tag{72}$$

From equation (69) it observed that the NMOS operates at boundary of saturation and ohmic regions when the output voltage becomes,

$$V_o = \frac{V_{DD}}{2} - V_T \tag{73}$$

The operation of NMOS changes from saturation region to ohmic region when output voltage V_o becomes less than $\frac{V_{DD}}{2} - V_T$.

Similarly, it is observed from equation (70) that the PMOS operates at boundary of ohmic and saturation regions when the output voltage becomes,

$$V_o = \frac{V_{DD}}{2} + V_T \tag{74}$$

The operation of PMOS changes from ohmic region to saturation region when output voltage V_o becomes less than $\frac{V_{DD}}{2} + V_T$.

Thus both transistors operate in saturation regions for $V_i = \frac{V_{DD}}{2}$ with output voltage in the following range,

$$\frac{V_{DD}}{2} - V_T < V_o < \frac{V_{DD}}{2} + V_T \tag{75}$$

Case-IV : When $\frac{V_{DD}}{2} < V_i < V_{DD} - V_T$

Then $$\frac{V_{DD}}{2} < V_{GSN} < V_{DD} - V_T \tag{76}$$

and $$V_T < V_{SGP} < \frac{V_{DD}}{2} \tag{77}$$

It is seen from case-II & case-III that when input voltage becomes more than $\frac{V_{DD}}{2}$ the operation of NMOS changes form saturation region to ohmic region and operation of PMOS changes from ohmic region to saturation region.

Case-V : When $V_{DD} - V_T < V_i < V_{DD}$

Then $$V_{DD} - V_T < V_{GSN} < V_{DD} \tag{78}$$

and $$0 < V_{SGP} < V_T \tag{79}$$

For above range of V_{GSN} and V_{SGP} the transistor Q_P operates in cutoff and transistor Q_N operates in ohmic region.

3.5.4 Noise Margins of CMOS

The noise margins of CMOS inverter depends on input and output voltage levels for logic '0' and logic '1'. Fig. 18 shows the voltage levels of CMOS inverter at input and output for logic '0' and logic '1'.

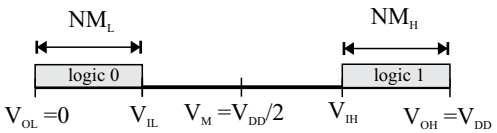


Fig. 18 Input and output voltage levels and noise margins of CMOS

In the Fig. 18 the voltage level V_{IL} is highest input voltage for logic '0' and V_{IH} is lowest input voltage for logic '1'. V_{OH} is highest voltage level for logic '1' at output and V_{OL} is lowest logic level at output for logic '0'.

A. Noise Margin for High Input

If a noise is super imposed an output (V_{OH}) of a driving inverter then the output driven inverter is not affected so long as input of driven inverter does not decrease below V_{IH}. This margin of safety is called noise margin for high input, NH_H

$$NM_H = V_{OH} - V_{IH} \tag{80}$$

B. Noise Margin for Low Input

If output of driving inverter is low at V_{OL} and driven inverter provides high output even if a noise is super-imposed on output of driving inverter, raising it up to V_{IL}. This margin of safety is called noise margin for low input.

$$NM_L = V_{IL} - V_{OL} \tag{81}$$

C. Derivation of Noise Margins of CMOS

The voltage V_{IH} can be determined by considering NMOS operation in triode region and PMOS in saturation region. As both devices are in series so their current is same.

$$I_{DN} = I_{DP}$$

$$\mu_n C_{ox} \cdot \frac{W_n}{L_n}\left[(V_{GSN} - V_T)V_{DSN} - \frac{1}{2}V_{DSN}^2\right] = \mu_p C_{ox} \cdot \frac{W_p}{L_p}(V_{SGP} - |V_T|)^2 \tag{82}$$

For CMOS inverter with matched MOSFETs.

$$\mu_n C_{ox} \cdot \frac{W_n}{L_n} = \mu_p C_{ox} \cdot \frac{W_p}{L_p}$$

From CMOS circuit, $V_{GSN} = V_i$,

$V_{DSN} = V_o$,

$V_{SGP} = V_{DD} - V_i$

$V_{SDP} = V_{DD} - V_o$

Putting above relations in equation (82), we have,

$$(V_i - V_T)V_o - \frac{1}{2}V_o^2 = \frac{1}{2}(V_{DD} - V_i - V_T)^2 \tag{83}$$

Differentiating both sides w.r.t. V_i, we have.

$$(V_i - V_T)\cdot\frac{dV_o}{dV_i} + V_o - V_o\frac{dV_o}{dV_i} = -(V_{DD} - V_i - V_T) \tag{84}$$

The voltage level V_{IL} is highest input voltage level for logic '0' and V_{IH} lowest input voltage level for logic '1'. The slope of transfer characteristics $\frac{dV_o}{dV_i} = -1$ at both liming operation levels $V_i = V_{IL}$ and

$V_i = V_{IH}$. Then equation (84) becomes,

$$\Rightarrow \quad -(V_{IH} - V_T) + V_o + V_o = -V_{DD} + V_{IH} + V_T$$

$$V_o = V_{IH} - \frac{V_{DD}}{2} \tag{85}$$

Putting $V_i = V_{IH}$ and V_o from (85) in equation (83), we have,

$$\boxed{V_{IH} = \frac{1}{8}(5V_{DD} - 2V_T)} \tag{86}$$

The input voltage level V_{IL} can be determined from transfer characteristics by using following relation,

$$V_{IH} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} - V_{IL} \tag{87}$$

$$\Rightarrow \quad V_{IL} = V_{DD} - V_{IH} \tag{88}$$

From equations (86) and (88), we have,

$$V_{IL} = V_{DD} - \frac{1}{8}(3V_{DD} + 2V_T)$$

$$\Rightarrow \quad \boxed{V_{IL} = \frac{1}{8}(3V_{DD} + 2V_T)} \tag{89}$$

From the transfer characteristics of CMOS, $V_{OH} = V_{DD}$, $V_{OL} = 0$.

The noise margin of CMOS for high input can be obtained as under,

$$NM_H = V_{OH} - V_{IH} \tag{90}$$

Putting expression of V_{IH} from equation (86) and $V_{OH} = V_{DD}$ in above equation, we have,

$$NM_H = V_{DD} - \frac{1}{8}(3V_{DD} + 2V_T) \tag{91}$$

$$\Rightarrow \quad \boxed{NM_H = \frac{1}{8}(3V_{DD} + 2V_T)} \tag{92}$$

The noise margin of CMOS for low input can be obtained as under,

$$NM_L = V_{IL} - V_{OL} \tag{93}$$

Putting expression of V_{IL} from equation (89) and $V_{OL} = 0$ in above equation, we have,

$$NM_L = \frac{1}{8}(3V_{DD} + 2V_T) - 0 \tag{94}$$

$$\Rightarrow \quad \boxed{NM_L = \frac{1}{8}(3V_{DD} + 2V_T)} \tag{95}$$

Effects of PMOS and NMOS parameters on Noise Margins:

i. The noise margin NM_L increases and NM_H decreases with increase in (W/L) ratio of PMOS

ii. The noise margin NM_L decreases and NM_H increases with increase in (W/L) ratio of NMOS

3.5.5 Dynamic Operation of CMOS

Dynamic operation is important for study of transient behaviour of CMOS. Rise time, fall time and propagation delays are important parameters used for transient analysis of a CMOS. A time delay between switching on of input and corresponding charge in output of CMOS is called propagation delay. The rise time, fall time and propagation delay of CMOS inverter can be determined by analyzing switching operation of CMOS. Consider a RC model of CMOS inverter as shown in Fig. 19. The capacitance 'C' in circuit represents sum of appropriate drain capacitances of PMOS and NMOS, the lead capacitances and input gate capacitances of driven gates. Let inverter is given a square pulse input as shown in waveform in Fig. 19.

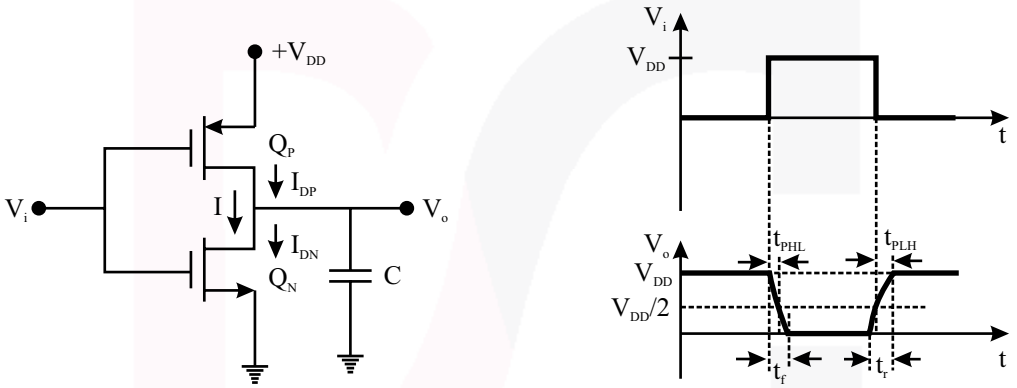


Fig.19 Capacitor loaded CMOS inverter and its input and output waveforms

Fall time (t_f):

Fall time is the time required to fall the output from its 90% to 10 % value of output. Fall time is associated when input changes from low to high and output changes from high ($+V_{DD}$) to low (0). During this period the PMOS is turned off and NMOS is turned on. The capacitance C is now connected to ground through NMOS which offers resistance r_{DSN}. The capacitances represented by C which are charged at voltage level V_{DD} now starts discharging through resistance r_{DSN} exponentially to ground with a time constant $\tau_n = Cr_{DSN}$.

The fall time is given by,

$$t_f = 2.2\,\tau_n = 2.2Cr_{DSN} \tag{96}$$

where,

$$r_{DSN} = \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n}(V_{GSN} - V_{TN})} \tag{97}$$

During fall time input applied to the CMOS is V_{DD} so the voltage $V_{GSN} = V_{DD}$ so r_{DSN} becomes,

$$r_{DSN} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TN})} \tag{98}$$

Rise time (t_r):

Rise time is the time required to rise the output from its 10% to 90 % value of output. Rise time is associated when input changes from high to low and output changes from low (0) to high($+V_{DD}$). During this period the PMOS is turned on and NMOS is turned off. The capacitor C is now connected to supply voltage through PMOS which offers resistance r_{DSP}. The capacitor which is fully discharged at 0V now starts charging through resistance r_{DSN} exponentially with a time constant $\tau_p = Cr_{DSP}$.

The rise time is given by,

$$t_r = 2.2\,\tau_p = 2.2Cr_{DSP} \tag{99}$$

where,
$$r_{DSP} = \frac{1}{\mu_p C_{ox}\frac{W_p}{L_p}(V_{SGP} - |V_{TP}|)} \tag{100}$$

During rise time input applied to the CMOS is '0' so the votlage $V_{SGP} = V_{DD}$ so r_{DSP} becomes,

$$r_{DSP} = \frac{1}{\mu_p C_{ox}\frac{W}{L}(V_{DD} - |V_{TP}|)} \tag{101}$$

The rise and fall time gives the maximum switching frequency of a CMOS inverter as under,

$$f_{max} = \frac{1}{t_r + t_f} = \frac{1}{2.2C(r_{DSN} + r_{DSP})} \tag{102}$$

Propagation Delay (t_p):

There are two time delays associated with fall of output signal for high to low and with rise of signal from low to high. The propagation delay during fall time is given by,

$$t_{pf} = \tau_n \ln 2 = 0.69\tau_n = 0.69\ Cr_{DSN} \tag{103}$$

The propagation delay during fall time is given by,

$$t_{pr} = \tau_p \ln 2 = 0.69\tau_p = 0.69\ Cr_{DSP} \tag{104}$$

Total propagation delay is average of rise and fall propagation delays. So, total propagation delay is given by,

$$t_p = (t_{pf} + t_{pr})/2 = 0.35(\tau_n + \tau_p) = 0.35C(r_{DSN} + r_{DSP}) \tag{105}$$

Methods of reduction propagation delay :

It observed from equation (105) that the propagation of CMOS can be reduced by reducing the drain capacitances, input gate capacitance and resistances of NMOS and PMOS which can be reduced by adopting following techniques,

(i) By reducing the internal capacitances of NMOS and PMOS and connecting lead capacitances.

(ii) By increasing C_{ox} or by reducing thickness of oxide layer.

(iii) By increasing width and reducing length of the channels of PMOS and NMOS.

(iv) By increasing power supply voltage.

3.5.6 Current flow and power dissipation in CMOS Inverter

The current in CMOS is negligible under static condition. However, it varies with input voltage depending on value of input voltage. Fig.20 shows the variation of CMOS current with input voltage.

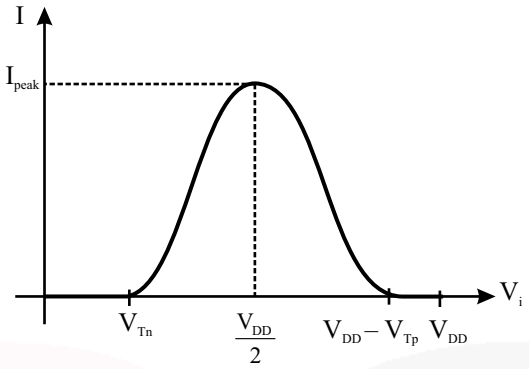


Fig.20 Variation of CMOS inverter current w.r.t. change in input voltage

The current in CMOS is maximum when input voltage is equal to $V_{DD}/2$. The peak current gives rise to dynamic power dissipation of CMOS.

The peak current of CMOS can be given by

$$I_{peak} = \frac{H_n C_{ox}}{2} \cdot \frac{W_n}{L_n} \left(\frac{V_{DD}}{2} - V_{Tn} \right)^2 \quad (106)$$

Corresponding dynamic power dissipation is given by,

$$P_D = fCV_{DD}^2 \quad (107)$$

where, f is switching frequency of the inverter.

Delay-Power Product (DP) :

$$DP = P_D t_p \quad (108)$$

Lower is propagation delay higher is frequency of operation and higher is power dissipation. So, the delay-power product is important figure of merit of an IC technology. It is constant for a particular technology. It is used to compare different IC circuit technologies.

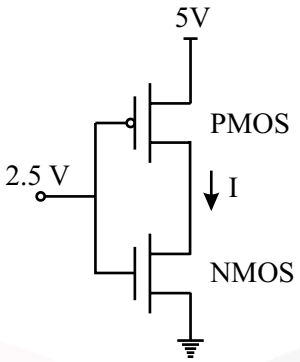
3.5.7 Advantages of CMOS inverter

i. The signal swing is maximum from '0' to V_{DD}.
ii. Static power dissipation is almost zero.
iii. There is low resistant path between output and ground or V_{DD}. Low resistance path makes output independent of $\frac{W}{L}$ & makes inverter less sensitive to noise.
iv. It has high output driving capability in both directions.
v. Input impedance is infinite so it can drive large number of similar inverters without loss of signal.

Example 12

In the CMOS inverter circuit shown, if the transconductance parameters of the NMOS and PMOS

transistors are $k_n = k_p = \mu_n C_{ox} \frac{W_n}{L_n} = \mu_p C_{ox} \frac{W_p}{L_p} = 40$ m A/V^2 and their threshold voltages are $V_{THn} = |V_{THp}| = 1$ V, the current I is

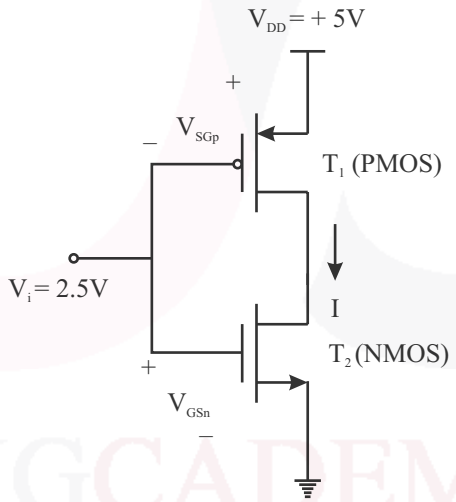


(a) 0A (b) 25 μA

(c) 45 μA (d) 90 μA

GATE(EC/2007/2M)

Solution : Ans.(d)



When input voltage V_i is $\frac{V_{DD}}{2}$ both PMOS and NMOS operate in saturation region. Therefore, both MOSFETs operate in saturation region in the given circuit. The drain current of MOSFET in saturation region is given as,

$$I_{Dn} = \frac{\mu_n C_{ox}}{2} \frac{W_n}{L_n} (V_{GSn} - V_{Tn})^2 \quad ; \quad \text{For NMOS} \qquad ....(i)$$

$$I_{Dp} = \frac{\mu_p C_{ox}}{2} \frac{W_p}{L_p} (V_{SGp} - |V_{Tp}|)^2 \quad ; \quad \text{For PMOS} \qquad ....(ii)$$

As both P-MOS and N-MOS are in series in C-MOS inverter so,

$I_{Dp} = I_{Dn} = I$

From given circuit, $V_{SGp} = V_{DD} - V_i$ and $V_{GSn} = V_i$

Also, $\mu_p C_{ox} \frac{W_P}{L_P} = \mu_n C_{ox} \frac{W_n}{L_n} = 40\ \mu A/ms$ and $V_{Tn} = |V_{Tp}| = 1\ V$

Putting above values in equation (i), we have,

$$\Rightarrow \quad I = \frac{40}{2}(5 - V_i - 1)^2$$

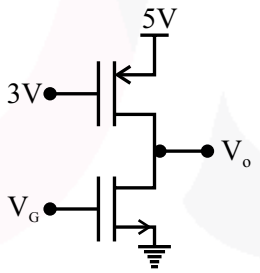
Given, $V_i = 2.5\ V$

$$\Rightarrow \quad I = \frac{40}{2}(5 - 2.5 - 1)^2\ \mu A = \frac{40}{2} \times 2.25\ \mu A = 45\ \mu A$$

Example 13

Statement for Linked Answer Questions (i) and (ii) :

Consider the CMOS circuit shown, where the gate voltage V_G of the n-MOSFET is increased from zero, while the gate voltage of the p-MOSFET is kept constant at 3 V. Assume that, for both transistors, the magnitude of the threshold voltage is 1 V and the product of the transconductance parameter and the (W/L) ratio, i.e. the quantity $\mu C_{ox}(W/L)$, is 1 mAV^{-2}.



(i) For small increase in V_G beyond 1 V, which of the following gives the correct description of the region of operation of each MOSFET?

(a) Both the MOSFETs are in saturation region

(b) Both the MOSFETs are in triode region

(c) n-MOSFET is in triode and p-MOSFET is in saturation region

(d) n-MOSFET is in saturation and p-MOSFET is in triode region

GATE(EC/2009/2M)

(ii) Estimate the output voltage V_0 for $V_G = 1.5$ V. [Hint: Use the appropriate current-voltage equation for each MOSFET, based on the answer of previous question.]

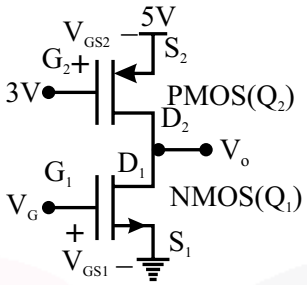
(a) $4 - \frac{1}{\sqrt{2}}V$ (b) $4 + \frac{1}{\sqrt{2}}V$

(c) $4-\frac{\sqrt{3}}{2}$V (d) $4+\frac{\sqrt{3}}{2}$V

GATE(EC/2009/2M)

Solution :

(i) Ans.(a)



For PMOS, $V_{DD} = 5V$

$V_{SG2} = V_{S2} - V_{G2} = 5 - 3 = 2V$

$V_{DD} - V_T = 5 - 1 = 4$ V

Input voltage, $V_{i2} = V_{G2} = 3V$

When $V_{SG2} > |V_T|$, the PMOS is either in saturation or in triode(ohmic) region.

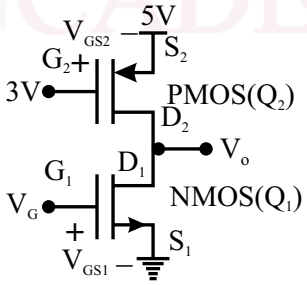
From voltage transfer characteristics of CMOS it is observed that the PMOS operates in saturation region when input voltage of PMOS is more than $V_{DD}/2$ and less than $V_{DD} - V_T$. For the given circuit V_i lies between $V_{DD}/2$ and $V_{DD} - V_T$ so the PMOS must be operating in saturation region of operation.

For NMOS, Input voltage, $V_{i1} = V_{GS1} = V_{G1} - V_{S1} = V_G - 0 = V_G = 1.5$ V

When $V_{SG1} > V_T$, the NMOS is either in saturation or in triode(ohmic) region.

From transfer characteristics of CMOS it is observed that the NMOS operates in saturation region when input gate voltage is more than V_T and less than $V_{DD}/2$. Here, V_G lies between V_T and $V_{DD}/2$ so the NMOS must be operating in saturation region.

(ii) Ans.(d)



Given, $V_G = 1.5$ V, $V_T = 1V$

$\therefore$ $V_{GS1} = 1.5$ V, $\mu C_{ox}\left(\frac{W}{L}\right) = 1 mA/V^2$

As V_{GS1} is slightly more than V_T so NMOS must be operating in saturation region. The drain current

of NMOS is given by,

$$I_{D1} = \frac{\mu C_{ox}}{2}\cdot\frac{W}{L}(V_{GS1} - V_T)^2$$

$$\Rightarrow \quad I_{D1} = \frac{1}{2}(1.5-1)^2 = \frac{1}{8}\text{mA} \qquad ...(i)$$

As PMOS is operating in ohmic region. The drain current of PMOS for ohmic region is given by,

$$I_{D2} = \mu_p C_{ox}\frac{W}{L}\left[(V_{SG2} - |V_T|)V_{SD2} - \frac{1}{2}V_{SD2}^2\right] \qquad ...(ii)$$

From circuit diagram, $V_{SG2} = 2V$

Also, $V_T = -1$ for PMOS,

$V_{SD2} = 5 - V_o$

Putting above values in equation (ii), we have,

$$I_{D2} = 1\left[(2-1)(5-V_o) - \frac{1}{2}(5-V_o)^2\right]\text{mA} \qquad ...(iii)$$

As both MOSFETs are in series, so, $I_{D2} = I_{D1}$

$$\Rightarrow \quad 5 - V_o - \frac{1}{2}(5-V_o)^2 = \frac{1}{8}$$

$$\Rightarrow \quad V_0^2 - 8V_o + \frac{61}{4} = 0$$

$$\Rightarrow \quad V_o = \frac{8 \pm \sqrt{64 - 4\times\frac{61}{4}}}{2}\text{V} = 4 \pm \frac{\sqrt{3}}{2}\text{V}$$

When PMOS is working in ohmic region the voltage V_{SD2} is small so output volt V_o is close to the voltage V_{DD}. So, output voltage of circuit is,

$$V_o = 4 + \frac{\sqrt{3}}{2}\text{V}$$

3.6 NMOS Pass Transistor

A pass transistor passes the information at input to output when the gate control signal is high. Fig. 21 shows pass transistor of NMOS transistor.

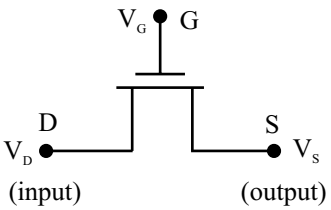


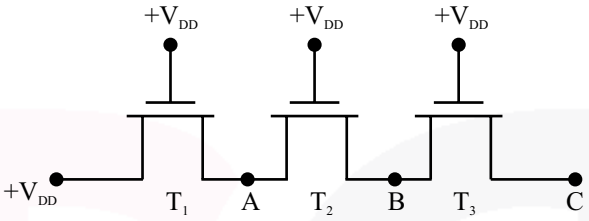
Fig.21 NMOS Transistor

The output of NMOS pass transistor is taken from the source terminal and input is applied at drain terminal. The output of the transistor is given by,

$$V_S = V_D \quad ; \text{ if } V_D \le V_G - V_T$$
$$= V_G - V_T \quad ; \text{ if } V_D > V_G - V_T$$

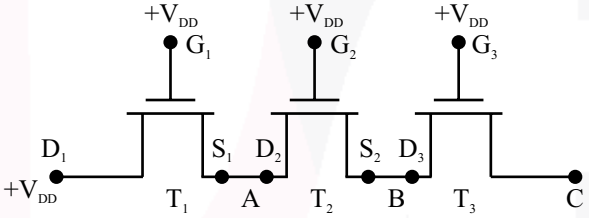
Example 14

Find the output voltage at A, B and C of pass transistors shown below. The transistors are identical having threshold voltage of V_T.



Ignore the body effect.

Solution :



Given $V_{G1} = V_{G2} = V_{G3} = +V_{DD}$

$V_{D1} = +V_{DD}$

Transistor T_1 :

From given circuit, $V_{G1} = V_{DD}$

$V_{G1} - V_T = V_{DD} - V_T$

$V_{D1} = V_{DD}$

From above relations it is found that,

$V_{D1} > V_{G1} - V_T$

$\therefore \quad V_{S1} = V_{G1} - V_T = V_{DD} - V_T$

$\Rightarrow \quad V_A = V_{S1} = V_{DD} - V_T$ .....(i)

Transistor T_2 :

$V_{D2} = V_A = V_{DD} - V_T$

$V_{G2} = V_{DD}$

$V_{G2} - V_T = V_{DD} - V_T$

From a relations it is found that,

$V_{G2} - V_T = V_{D2}$

$\therefore \quad V_{S2} = V_{D2} = V_{DD} - V_T$

$\Rightarrow$ $V_B = V_{S2} = V_{DD} - V_T$ .....(ii)

Transistor T_3 :

$$V_{D3} = V_B = V_{DD} - V_T$$
$$V_{G3} = V_{DD}$$
$$V_{G3} - V_T = V_{DD} - V_T$$

From a relations it is found that,

$$V_{G3} - V_T = V_{D3}$$
$\therefore$ $V_{S3} = V_{D3} = V_{DD} - V_T$

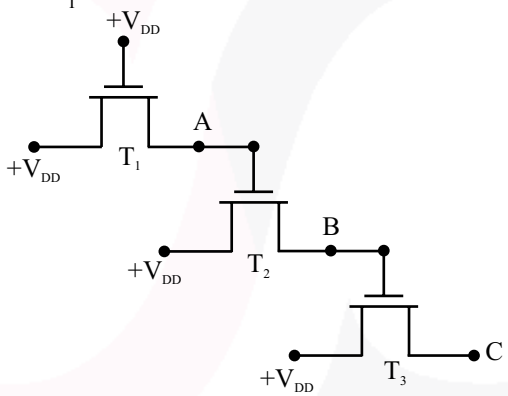
$\Rightarrow$ $V_C = V_{S3} = V_{DD} - V_T$ .....(iii)

From equation (i), (ii) and (iii), we have,

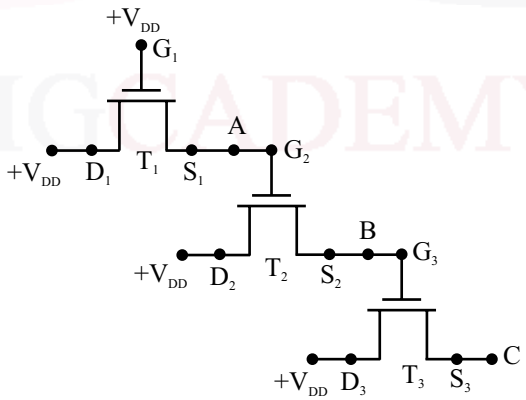
$$V_A = V_B = V_C = V_{DD} - V_T$$

Example 15

Find the voltages at A, B and C in the circuit of pass transistors shown below, transistor are identical having threshold voltage of V_T.



Solution :



Transistor T_1 :

$$V_{G1} = +V_{DD}$$
$$V_{D1} = V_{DD}$$
$$V_{G1} - V_T = V_{DD} - V_T$$

$\Rightarrow \quad V_{G1} - V_T < V_D$

Voltage at source of T_1, $V_{S1} = V_{G1} - V_T = V_{DD} - V_T$

$\therefore \quad V_A = V_{S1} = V_{DD} - V_T$

Transistor T_2 :

$V_{G2} = V_A = V_{DD} - V_T$

$V_{G2} - V_T = V_{DD} - 2V_T$

$V_{D2} = V_{DD}$

$\Rightarrow \quad V_{GS2} - V_T < V_{D2}$

Voltage at source of T_2, $V_{S2} = V_{G2} - V_T = V_{DD} - V_T - V_T = V_{DD} - 2V_T$

$\Rightarrow \quad V_B = V_{S2} = V_{DD} - 2V_T$

Transistor T_3 :

$V_{G3} = V_B = V_{DD} - 2V_T$

$V_{G3} - V_T = V_{DD} - 3V_T$

$V_{D3} = V_{DD}$

$\Rightarrow \quad V_{G3} - V_3 < V_{D3}$

Voltage at source T_3, $V_{S3} = V_{G3} - V_T = V_{DD} - 2V_T - V_T = V_{DD} - 3V_T$

$\Rightarrow \quad V_C = V_{S3} = V_{DD} - 3V_T$

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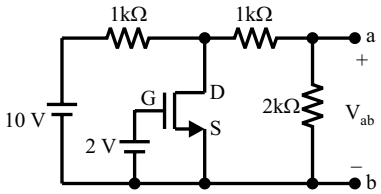
GATE QUESTIONS

Q. 1 Assume that the N-channel MOSFET shown in figure is ideal and that its threshold voltage is +1.0 V. The voltage V_{ab} between nodes a and b is

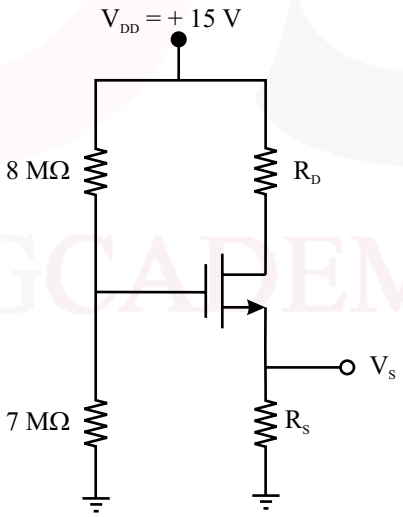


(a) 5 V (b) 2 V

(c) 1 V (d) 0 V

GATE(EE/2005/1 M)

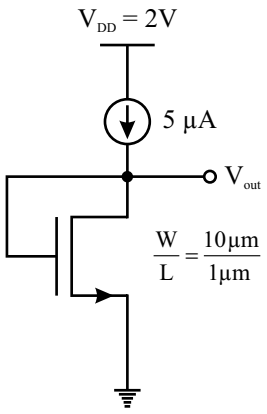
Q. 2 In the circuit, shown in the figure, the MOSFET is operating in the saturation zone. The characteristics of the MOSFET is given by $I_D = \frac{1}{2}(V_{GS} - 1)^2$ mA, where V_{GS} is in V. If $V_s = +5V$, then the value of R_S in kΩ is _____.



GATE(IN/2017/2 M)

Q. 3 The enhancement type MOSFET in the circuit below operates according to the square law.

$\mu_n C_{ox}$ = 100 μA/V², the threshold voltage (V_T) is 500 mV. Ignore channel length modulation. The output voltage Vout is

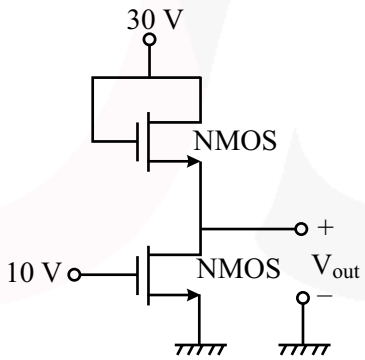


(a) 100 mV (b) 500 mV

(c) 600 mV (d) 2V

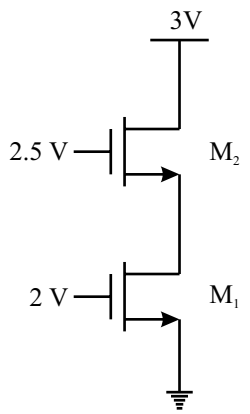
GATE(EE/2019/2M)

Q. 4 In the circuit shown in the figure, both the NMOS transistors are identical with their threshold voltages being 5V. Ignoring channel length modulation, the output voltage V_{out} in volt is ..... V.



GATE(IN/2015/2 M)

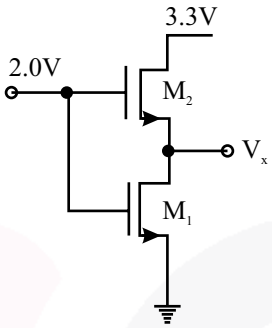
Q. 5 Assuming that transistors M_1 and M_2 are identical and have a threshold voltage of 1V, the state of transistors M_1 and M_2 are respectively.



(a) Saturation, Saturation
(b) Linear, Linear
(c) Linear, Saturation
(d) Saturation, Linear

GATE(EC-II/2017/2 M)

Q. 6 In the circuit shown below, the (W/L) value for M_2 is twice that for M_1. The two nMOS transistors are otherwise identical. The threshold voltage V_T for both transistors is 1.0 V. Note that V_{GS} for M_2 must be > 1.0 V.



Current through the nMOS transistors can be modeled as

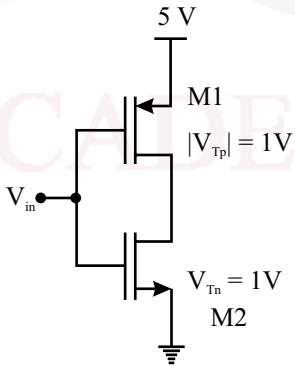
$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right) \quad \text{for } V_{DS} \le V_{GS} - V_T$$

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 / 2 \quad \text{for } V_{DS} \ge V_{GS} - V_T$$

The voltage (in volts, accurate to two decimal places) at V_x is _____.

GATE(EC/2018/2 M)

Q. 7 In the CMOS circuit shown, electron and hole mobilities are equal, and M1 and M2 are equally sized The device M1 is in the linear region if



(a) $V_{in} < 1.875$ V
(b) $1.875V < V_{in} < 3.125V$
(c) $V_{in} > 3.125$ V
(d) $0 < V_{in} < 5$ V

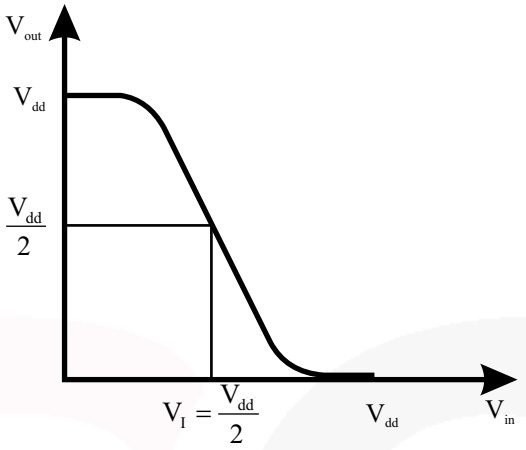
GATE(EC/2012/2M)

Q. 8 A CMOS inverter, designed to have a mid-point voltage V_I equal to half of V_{dd}, as shown in the figure, has the following parameters:

$\mu_n C_{ox} = 100\ \mu A/V^2$; $V_{tn} = 0.7$ V for nMOS

$\mu_p C_{ox} = 40\ \mu A/V^2$; $V_{tp} = 0.9$ V for pMOS and $V_{dd} = 3$ V

The ratio of $\left(\frac{W}{L}\right)_n$ to $\left(\frac{W}{L}\right)_p$ is equal to _____ (rounded off to 3 decimal places).



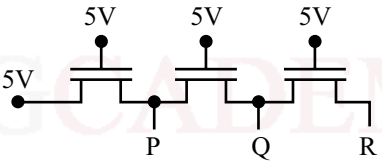
GATE(EC/2019/2M)

Q. 9 A standard CMOS inverter is designed with equal rise and fall times ($\beta_n = \beta_p$). If the width of the pMOS transistor in the inverter is increased, what would be the effect on the LOW noise margin (NM_L) and the HIGH noise margin NM_H?

(a) NM_L increases and NM_H decreases.
(b) NM_L decreases and NM_H increases.
(c) Both NM_L and NM_H increase.
(d) No change in the noise margins.

GATE(EC/2019/1M)

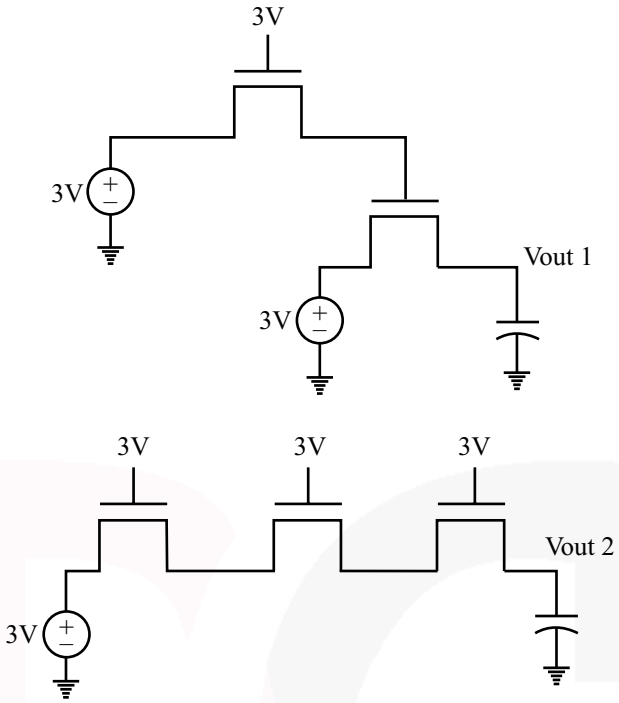
Q. 10 In the following circuit employing pass transistors are identical with a threshold voltage of 1 V. Ignoring the body-effect, the output voltages at P, Q and R are,



(a) 4 V, 3 V, 2 V
(b) 5 V, 5 V, 5 V
(c) 4 V, 4 V, 4 V
(d) 5 V, 4 V, 3 V

GATE(EC-I/2014/1 M)

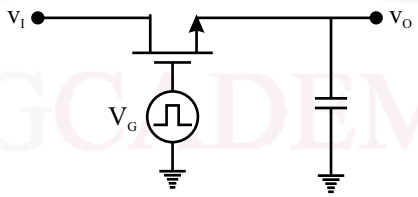
Q. 11 In the circuits shown, the threshold voltage of each nMOS transistor is 0.6 V. Ignoring the effect of channel length modulation and body bias, the values of .Vout1 and Vout2, respectively, in volts, are



(a) 1.8 and 1.2
(b) 2.4 and 2.4
(c) 1.8 and 2.4
(d) 2.4 and 1.2

GATE(EC/2019/2M)

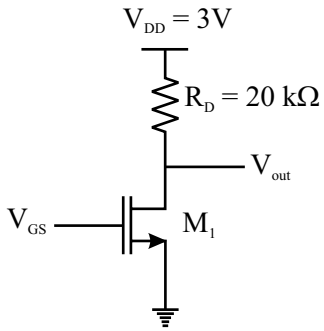
Q. 12 An enhancement MOSFET of threshold voltage 3 V is being used in the sample and hold circuit given below. Assume that the substrate of the MOS device is connected to –10 V. If the input voltage v_i lies between ±10 V. the minimum and the maximum values of v_G required for proper sampling and holding respectively, are



(a) 3 V and –3 V
(b) 10 V and –10 V
(c) 13 V and –7 V
(d) 10 V and –13 V

GATE(EC/2020/2M)

Q. 13 For the transistor M_1 in the circuit shown in the figure, $\mu_n C_{0X} = 100\ \mu A/V^2$ and (W/L) = 10, where is the mobility of electron, C_{ox} is the oxide capacitance per unit area, W is the width and L is the length.



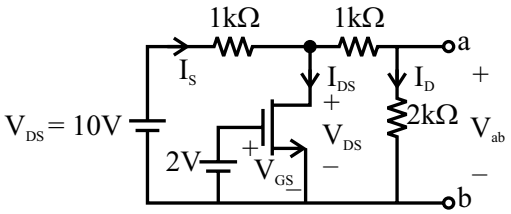
The channel length modulation coefficient is ignored. If the gate-to-source voltage V_{GS} is 1 V to keep the transistor at the edge of saturation, then the threshold voltage of the transistor (rounded off to one decimal place) is _____V.

GATE(EC/2021/2M)

❐❐❐

ANSWERS & EXPLANATIONS

Q. 1 Ans.(d)



Given, threshold voltage of MOSFET, $V_T = 1V$

KCL of node A

$$\frac{V_{DS}-10}{1K} - I_D + \frac{V_{DS}}{3K} = 0$$

$$\frac{4}{3}V_{DS} = 10 + I_D$$

$$\Rightarrow \quad V_{DS} = 7.5 + 0.75\, I_D$$

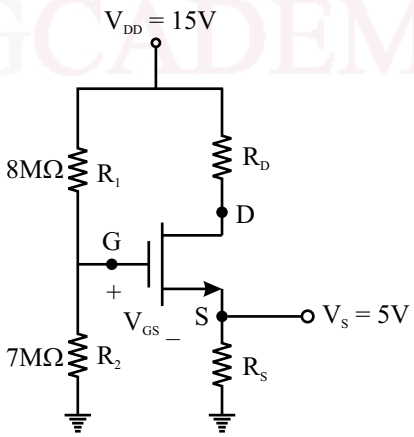
For saturation region, $V_{DS} > (V_{GS} - V_T)$

Here, $V_{GS} - V_T = 2 - 1 = 1V$

As, $V_{DS} > V_{GS} - V_T$ so MOSFET operates in saturation region .

The resistance offered by the MOFET in saturation region is zero ideally. So MOSFET behaves like a short circuit and whole of the supply current is passed through the MOSFET. Thus current through 2 kΩ resistance is zero. Therefore, voltage V_{ab} is zero.

Q. 2 Ans. : 9.9 to 10.1



Given, $I_D = \frac{1}{2}(V_{GS}-1)^2$ mA and $V_s = 5V$

Voltage at gate terminal, $V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{7}{7+8} \times 15 = 7\ V$

Voltage, $V_{GS} = V_G - V_S = 7 - 5 = 2V$

Drain current, $I_D = \frac{1}{2}(2-1)^2 = \frac{1}{2}mA$

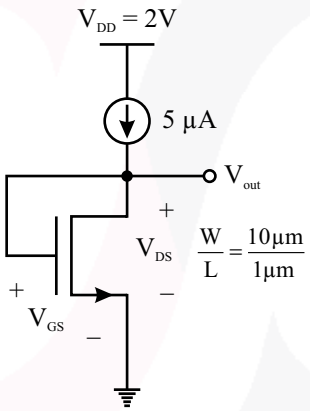
Voltage at source terminal,

$$V_S = R_S I_D$$

$$\Rightarrow \quad 5 = R_S \times \frac{1}{2} \times 10^{-3}$$

$$\Rightarrow \quad R_S = 10k\Omega$$

Q. 3 Ans.(c)



A MOSFET works is saturation mode when drain terminal is shorted with gate terminal. The drain current for saturation region of operator of enhancement NMOS is given by,

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

Given, $\mu_n C_{ox} = 100\ \mu A/V^2$

$$\frac{W}{L} = \frac{10\mu m}{1\mu m}$$

$$V_T = 500\ mV = 0.5V$$

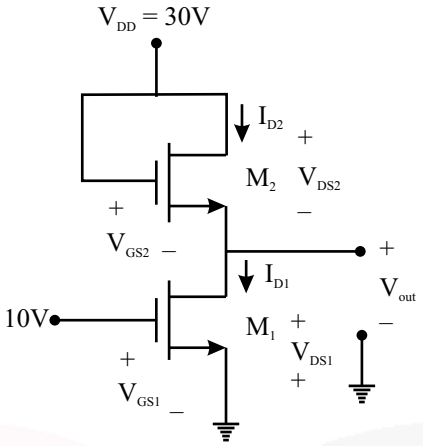
From given circuit, $V_{GS} = V_{out}$

The drain current, $I_D = 5\mu A$

$$\therefore \quad 5 \times 10^{-6} = \frac{100 \times 10^{-6}}{2} \cdot \frac{10}{1}(V_{out} - 0.5)^2$$

$$\Rightarrow \quad V_{out} = 0.6\ V = 600\ mV$$

Q. 4 Ans.: 20



Given, threshold voltage, $V_T = 5$ V

From above circuit, $V_{GS1} = 10 - 0 = 10V$

and $V_{DS1} = V_{out}$

For upper MOSFET, M_2

$$V_{GS2} = V_{DD} - V_{out} = 30 - V_{out}$$

For given combination of identical MOSFETs.

$$I_{D1} = I_{D2}$$

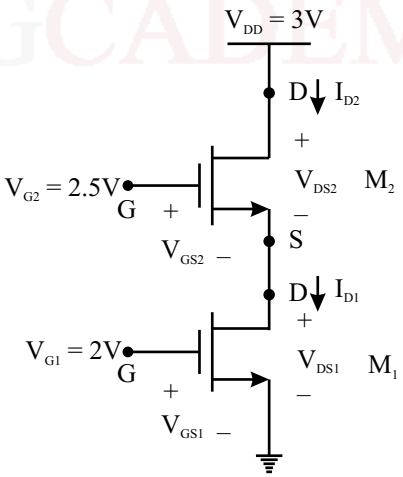
$$\frac{\mu_n C_{ox} W}{2L}(V_{GS1} - V_T)^2 = \frac{\mu_n C_{ox} W}{2L}(V_{GS2} - V_T)^2$$

$$\Rightarrow \quad V_{GS1} - V_T = V_{GS2} - V_T$$

$$\Rightarrow \quad 10 - 5 = (30 - V_{out} - 5)$$

$$\Rightarrow \quad V_{out} = 20V$$

Q. 5 Ans.(c)



Both transistors are identical with,

$$V_T = 1V$$

From MOSFET M_1, $V_{GS1} = 2.0 - 0 = 2.0$ ....(i)

From MOSFET M_2, $V_{GS2} = V_{G2} - V_{DS1} = 2.5 - V_{DS1}$ .....(ii)

Drain current of M_1 & M_2

$$I_{D1} = K_1 (V_{GS1} - V_{T1})$$

$$I_{D2} = K_2 (V_{GS2} - V_{T2})$$

For given combination,

$$I_{D1} = I_{D2}$$

$$\Rightarrow \quad K_1(V_{GS1} - V_{T1}) = K_2 (V_{GS2} - V_{T2})$$

If both transistor are identical then,

$$K_1 = K_2 = K$$

$$V_{T1} = V_{T2} = V_T = 1V$$

$$\therefore \quad K(V_{GS1} - 1) = K(V_{GS2} - 1)$$

$$\Rightarrow \quad V_{GS1} - 1 = V_{GS2} - 1 \quad .....(iii)$$

From (i), (ii) and (iii), we hvae,

$$2 - 1 = 2.5 - V_{DS1} - 1$$

$$\Rightarrow \quad V_{DS1} = 0.5V$$

Also, $V_{DD} = V_{DS2} + V_{DS1}$

$$\Rightarrow \quad V_{DS2} = V_{DD} - V_{DS1} = 3 - 0.5$$

$$\Rightarrow \quad V_{DS2} = 2.5V$$

$$\therefore \quad V_{GS2} = V_{G2} - V_{DS1} = 2.5 - 0.5 = 2V$$

A MOSFET works in saturation region if $V_{DS} > V_{GS} - V_T$ and it works in ohmic region if $V_{DS} < V_{GS} - V_s$

For MOSFET M_2,

$$V_{DS1} = 0.5V$$

and $V_{GS1} - V_T = 2 - 1 = 1V$

$$\therefore \quad V_{DS1} < V_{GS1} - V_T$$

So M_1 operation in ohmic or linear region.

For MOSFET M_2

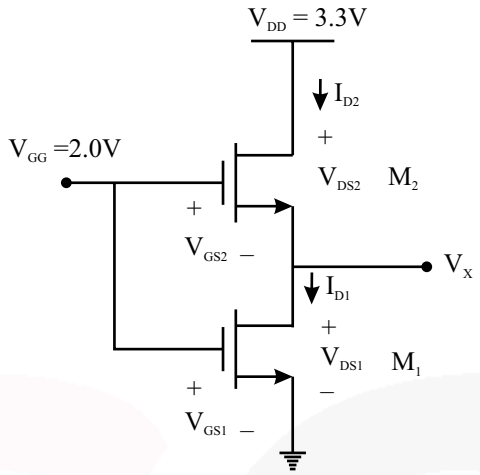
$$V_{DS2} = 2.5V$$

$$V_{GS2} - V_T = 2.0 - 1 = 1V$$

$$\therefore \quad V_{DS2} > V_{GS2} - V_T$$

So, M_2 operates in saturation region.

Q. 6 Ans.(0.41 to 0.435)



Threshold voltage of both MOSFETS, $V_T = 1V$

For NMOS M_2, $V_{GS2} = V_{GG} - V_X = 2 - V_X$

and $V_{DS2} = V_{DD} - V_X = 3.3 - V_X$

$V_{GS2} - V_T = 2 - V_X - 1 = 1 - V_X$

A MOSFET operates in saturation region if $V_{DS} > V_{GS} - V_T$. For NMOS M_2 , $V_{DS2} > V_{GS2} - V_T$, therefore, NMOS M_2 works in saturation.

The drain current of NMOS M_2 can be given by,

$$I_{DS2} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2$$

$$\Rightarrow \quad I_{DS2} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (1 - V_x)^2$$

For NMOS, M_1 $V_{GS1} = 2V$

$V_{GS1} - V_T = 2 - 1 = 1$

$V_{DS1} = V_X$

NMOS M_1 works in saturation if

$V_{DS1} > (V_{GS1} - V_T)$

$\Rightarrow \quad V_X > 1$

If V then the voltage becomes negative and NMOS M_2 no more operates saturation. Therefore, V_X must be less than 1 V and NMOS M_1 operates in linear or ohmic region. The drain current of NMOS M_1 can be given by,

$$I_{DS1} = \mu C_{ox}\left(\frac{W}{L}\right)_1 \left((V_{GS1} - V_T)V_{DS1} - \frac{1}{2}V_{DS1}^2\right)$$

$$\Rightarrow \quad I_{DS1} = \mu C_{ox}\left(\frac{W}{L}\right)_1\left(1\times V_x - \frac{1}{2}V_x^2\right)$$

$$\Rightarrow \quad I_{DS1} = \mu C_{ox}\left(\frac{W}{L}\right)_1\left(V_x - \frac{1}{2}V_x^2\right)$$

For the given circuit, $I_{D1} = I_{D2}$

$$\mu C_{ox}\left(\frac{W}{L}\right)_1\left(V_x - \frac{1}{2}V_x^2\right) = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (1 - V_x)^2$$

$$\Rightarrow \quad \left(\frac{W}{L}\right)_1\left(V_x - \frac{1}{2}V_x^2\right) = \frac{1}{2}\left(\frac{W}{L}\right)_2 (1 - V_x)^2$$

Given, $$\left(\frac{W}{L}\right)_2 = 2\left(\frac{W}{L}\right)_1$$

$$\Rightarrow \quad V_x - \frac{1}{2}V_x^2 = (1 - V_x)^2$$

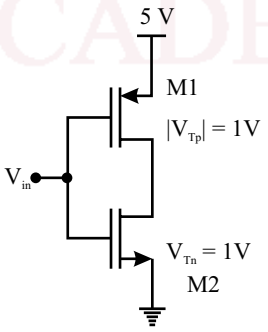
$$\Rightarrow \quad 2V_x - V_x^2 = 2 - 4V_x + 2V_x^2$$

$$\Rightarrow \quad 3V_x^2 - 6V_x + 2 = 0$$

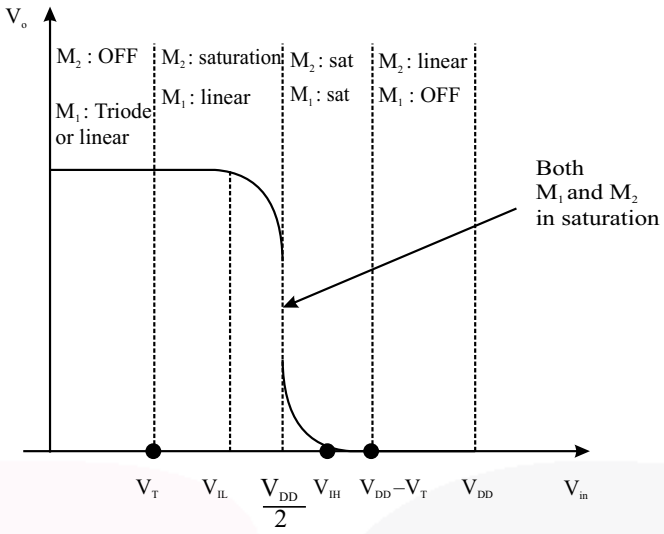
$$\Rightarrow \quad V_x = 0.422 \text{ V}, 1.577 \text{ V}$$

As discussed earlier that the voltage V_x is less than 1 V so correct answer is $V_x = 0.422$ V.

Q. 7 Ans.(a)

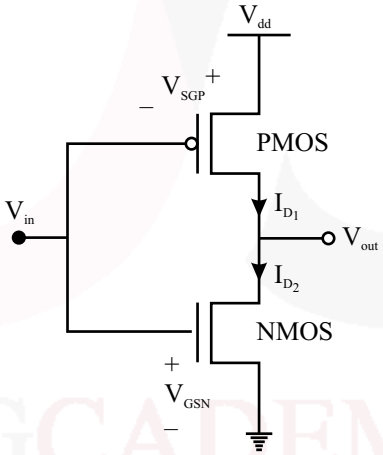


Given circuit is a CMOS inverter. The voltage transfer characteristic of CMOS inverter is as shown below,



From voltage transfer characteristics it clear that PMOS M_1, is in triode region for $0 < V_{in} < 2.5$. From given options the range $0 < V_{in} < 1.875$ is correct answer.

Q. 8 Ans.(0.210 to 0.230)



When a CMOS circuit is biased at Mid point of voltage transfer characteristics, both PMOS and NMOS operate in saturation region of operation.

In that case

$$I_{D_1} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p \left(V_{SGP} - |V_{tp}|\right)^2$$

and

$$I_{D_2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n \left(V_{GSN} - V_{tn}\right)^2$$

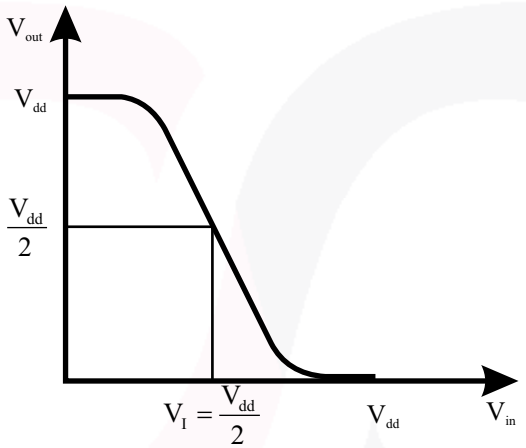
For a CMOS, $I_{D_1} = I_{D_2}$

$$\Rightarrow \quad \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p \left(V_{SGP} - |V_{tp}|\right)^2 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n \left(V_{GSN} - V_{tn}\right)^2$$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\frac{\mu_p C_{ox}}{2}\left(V_{SGP} - |V_{tp}|\right)^2}{\frac{\mu_n C_{ox}}{2}\left(V_{GSN} - V_{tn}\right)^2}$$

A mid point of voltage transfer character,

$$V_{in} = \frac{V_{dd}}{2} = V_{GSN}$$



$$\therefore \quad V_{SGP} = V_{dd} - V_{in} = V_{dd} - \frac{V_{dd}}{2} = \frac{V_{dd}}{2}$$

$$\therefore \quad \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p C_{ox}\left(\frac{V_{dd}}{2} - |V_{tp}|\right)^2}{\mu_n C_{ox}\left(\frac{V_{dd}}{2} - V_{tn}\right)^2}$$

Given, $V_{dd} = 3V$, $\mu_n C_{ox} = 100\ \mu A/V^2$, $\mu_p C_{ox} = 40\ \mu A/V^2$, $V_{tn} = 0.7V$, $|V_{tp}| = 0.9V$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{40 \times \left(\frac{3}{2} - 0.9\right)^2}{100 \times \left(\frac{3}{2} - 0.7\right)^2} = 0.225$$

Q. 9 Ans.(a)

Noise margins of CMOS are given by,

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

For a CMOS, $V_{OL} \approx 0$

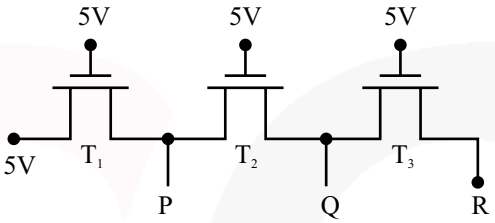
and $V_{OH} \approx V_{DD}$

$\therefore$ $NM_L = V_{IL}$

and $NM_H = V_{DD} - V_{IH}$

Both V_{IL} and V_{IH} increase with increase in width of PMOS, therefore, NM_L increases and NM_H decreases with increase in width of PMOS.

Q. 10 Ans.(c)



Given, $V_{T1} = V_{T2} = V_{T3} = V_T = 1V$

Output of a pass transistor at source is given by

$$V_S = V_D \quad ; \text{if } V_D < V_{GS} - V_T$$
$$= V_G - V_T \; ; \text{if } V_D \geq V_{GS} - V_T$$

From transistor T_1,

$$V_{G1} = 5V$$
$$V_{D1} = 5V$$
$$V_{G1} - V_T = 5 - 1 = 4V$$

Here $V_{D1} > V_{G1} - V_T$

$\therefore$ Output of T_1 at source terminal,

$$V_P = V_{G1} - V_T = 4V$$

From transistor T_2,

$$V_{G2} = 5V$$
$$V_{D2} = V_P = 4V$$
$$V_{G2} - V_T = 5 - 1 = 4V$$

Here $V_{D2} = V_{G2} - V_T$

$\therefore$ Output of T_2,

$$V_Q = V_{D2} = 4V$$

From transistor T_3,

$$V_{G3} = 5V$$

$$V_{D3} = V_Q = 4V$$

$$V_{G3} - V_T = 5 - 1 = 4V$$

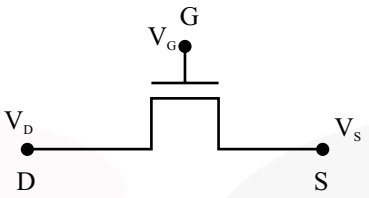
Here $V_{D3} = V_{G3} - V_T$

$\therefore$ Output of transistor T_3,

$$V_R = V_{D3} = 4V$$

Q. 11 Ans.(c)

Output of a pass transistor shown below is given by

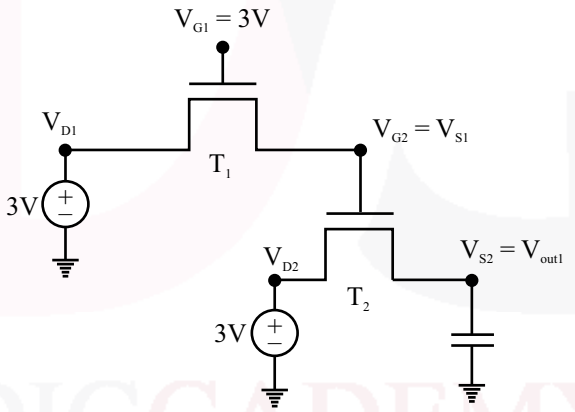


$$V_S = V_D \quad ; \; V_G - V_T \geq V_D$$

$$= V_G - V_T \; ; \; V_G - V_T < V_D$$

Where V_T is threshold voltage of MOSFET.

Circuit-1 :



Given,

$V_T = 0.6V$, $V_{G1} = 3V$, $V_{D1} = 3V$ and $V_{D2} = 3V$

From transistor T_1,

$$V_{G1} - V_T = 3 - 0.6 = 2.4\ V$$

$\Rightarrow \; V_{G1} - V_T < V_{D1}$

$\therefore \quad V_{S1} = V_{G1} - V_T = 3 - 0.4 = 2.4V$

From transistor T_2,

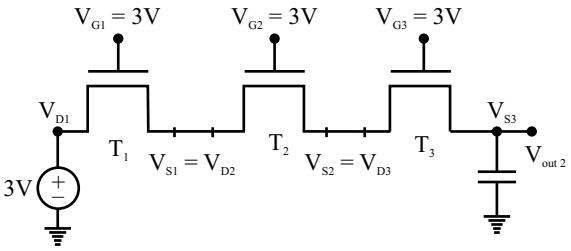
$\therefore \quad V_{G2} = V_{S1} = 2.4V$

$\therefore \quad V_{G2} - V_T = 2.4 - 0.6 - 1.8$

$\Rightarrow \quad V_{G2} - V_T < V_{D2}$

$\therefore \quad V_{out} = V_{S2} = V_{G2} - V_T = 1.8V$

Circuit-2



Given, $V_{G1} = 3V, V_{G2} = 3V, V_{G3} = 3V$

From transistor T_1,

$V_{G1} - V_T = 3 - 0.6 = 2.4V$

$\Rightarrow \quad V_{G1} - V_T < V_{D1}$

$\therefore \quad V_{S1} = V_{G1} - V_T = 2.4V$

$V_{D2} = V_{S1} = 2.4V$

From transistor T_2, $V_{G2} - V_T = 3 - 0.6 = 2.4\ V = V_{D2}$

$\therefore \quad V_{S2} = V_{G2} - V_T = 2.4\ V$

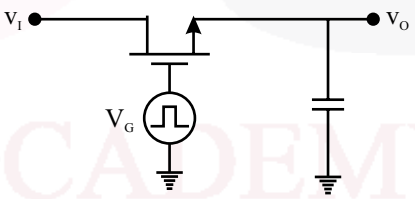
$V_{D3} = V_{S2} = 2.4\ V$

From transistor T_3, $V_{G3} - V_T = 3 - 0.6 = 2.4V = V_{D3}$

$\therefore \quad V_{S3} = V_{G3} - V_T = 2.4\ V$

$\Rightarrow \quad V_{out} = V_{S3} = 2.4\ V$

Q. 12 Ans(c)



Given threshold voltage of MOSFET, $V_{th} = 3V$

The output of MOSFET in sampler circuit is given by,

$v_o = v_i$; if $v_i < v_G - V_{th}$ or $v_G > v_i + V_{th}$

$= v_G - V_{th}$; if $v_i > v_G - V_{th}$ or $v_G < v_i + V_{th}$

In other words input is sampled when $v_G > v_i + V_{th}$ and output is hold when $v_G < v_i + V_{th}$

Case-I : $v_i = +10V$

For sampling: $v_G > v_i + V_{th}$

or $v_G > 10 + 3$

or $v_G > 13V$

For holding: $v_G < v_i + V_{th}$

$v_G < 10 + 3$

$v_G < 13V$

Case-II : $v_i = -10$

For sampling: $v_G > v_i + V_{th}$

$\Rightarrow$ $v_G > -10 + 3$

$\Rightarrow$ $v_G > -7V$

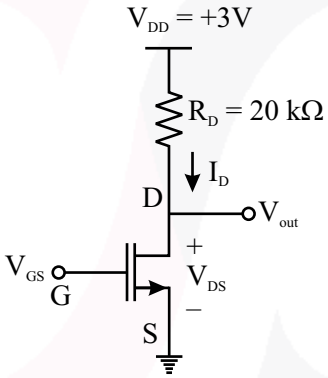
Fro holding: $v_G < v_i + V_{th}$

$\Rightarrow$ $v_G < -10 + 3$

or $v_G < -7V$

$\therefore$ For sampling minimum gate voltage is 13V and for holding maximum gate voltage is –7V.

Q. 13 Ans.(0.5 to 0.5)



Drain current of NMOSFET is given by,

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_T)^2$$

Given, $\mu_n C_{ox} = 100\mu A/V^2, \frac{W}{L} = 10$

$\Rightarrow$ $$I_D = \frac{100 \times 10^{-3}}{2} \times 10(V_{GS} - V_T)^2 \text{ mA}$$

$\Rightarrow$ $I_D = 0.5(V_{GS} - V_T)^2$ .....(i)

For drain to source circuit,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$\Rightarrow$ $V_{DS} = 3 - 20I_D$

Putting expression of I_D in above equation, we have,

$$V_{DS} = 3 - 20 \times 0.5 (V_{GS} - V_T)^2$$

At the edge of saturation region,

$$V_{DS} = V_{GS} - V_T \quad \text{.....(ii)}$$

$$\Rightarrow \quad V_{DS} = 3 - 20 \times 0.5\ V_{DS}^2$$

$$\Rightarrow \quad 10V_{DS}^2 + V_{DS} - 3 = 0$$

$$\Rightarrow \quad V_{DS} = 0.5\ V, -0.6V$$

V_{DS} cannot be negative,

$$\therefore \quad V_{DS} = 0.5V$$

Putting $V_{DS} = 0.5$ V in equation (ii) we ahve,

$$0.5 = V_{GS} - V_T$$

Given, $V_{GS} = 1V$

$$\Rightarrow \quad V_T = V_{GS} - 0.5 = 1 - 0.5 = 0.5\ V$$

❐❐❐

Ch 4 Small Signal Analysis of BJT

4.1 Introduction

The signals whose amplitude is very small in comparison to magnitude of biasing signals and have low frequency are classified as small signals. The study of behavioral characteristics of BJT amplifier with small signals is called an AC analysis and study of biasing characteristics of BJT with DC biasing signals is called DC analysis. A BJT amplifier require both AC as well as DC analysis for small signal analysis of the amplifier.

DC Analysis:

The DC analysis is performed to find bias current I_B, I_E and I_C and collector to emitter voltage V_{CE}. These DC signals are then used to determine the following,

(a) the operating point

(b) the thermal stability

(c) parameters of BJT like r_e , r_π, r_o and g_m

The DC analysis is performed by opening the input and output coupling capacitors as well as emitter bypass capacitors.

AC or Small Signal Analysis:

The AC or small signal analysis of BJT is performed to find out voltage gain, current gain, input impedance and output impedance of the amplifier. For AC analysis of the amplifier, the DC basing voltage sources are grounded or short circuited, the DC biasing current sources are open circuited, coupling and bypass capacitors are replaced by short circuit and BJT is replaced by its small signal model.

4.2 h-parameter model of BJT

Small signal analysis of BJT is applicable for low frequency and low level of the signals. A bipolar junction transistor (BJT) has three terminals with one terminal used as input, another used as output terminal and third terminal as common between input and output. Therefore, a BJT behaves like a two port network. A two port network with input and output ports can be drawn as shown in Fig.1.

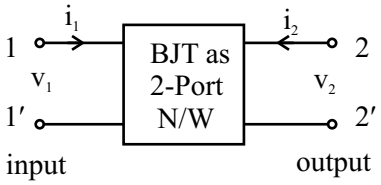


Fig. 1 BJT represented as a two port network

The input and output signals of a 2-port network can be related to each other in terms of h-parameters of the network as under,

$$v_1 = h_{11} i_1 + h_{12} v_2 \quad (1)$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \quad (2)$$

where, $h_{11} = \left.\frac{v_1}{i_1}\right|_{V_2 = 0}$ = Short circuited input impedance $= h_i$

$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1 = 0}$ = Open circuited reverse voltage gain $= h_r$

$h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2 = 0}$ = Short circuited forward current gain $= h_f$

$h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1 = 0}$ = Open circuited output admittance $= h_o$

Therefore, the input and output signals can also be related as under,

$\therefore$ $$v_1 = h_i i_1 + h_r v_2 \quad (3)$$

$$i_2 = h_f i_1 + h_o v_2 \quad (4)$$

Equivalent circuit of the two port network shown in Fig. 1 can be drawn in terms of h-parameters of the network as shown in Fig.2.

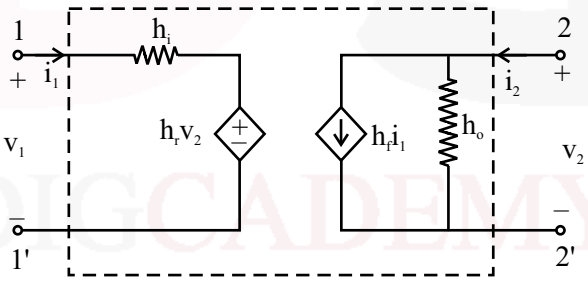


Fig. 2 Equivalent circuit of BJT as two port network

A BJT is represented by *h*-parameter model because it is a single parameter model which gives all important parameters of BJT amplifier i.e. input impedance, output admittance, voltage gain and current gain.

4.2.1 h-parameter Model of Common Emitter Configuration

The emitter terminal is common between input and output terminals in common emitter configuration of a BJT. The equivalent circuit in terms of h-parameters of common emitter configuration of BJT is shown in Fig.3.

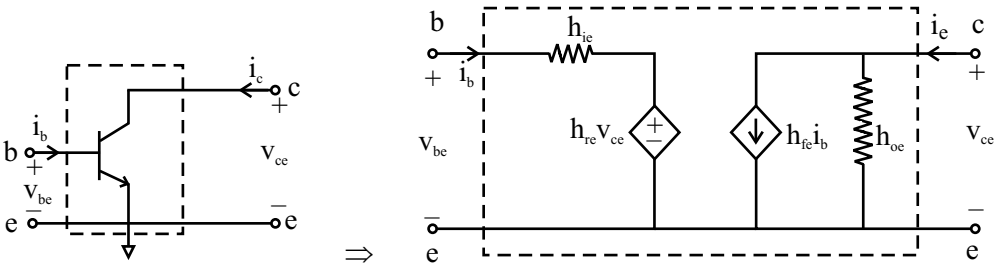


Fig. 3 Equivalent circuit of common emitter configuration of BJT as two port network

The input and output signals of common emitter configuration can be related in terms of h-parameter of the configuration as under,

$$v_{be} = h_i i_b + h_r v_{ce} \quad (5)$$

$$i_c = h_f i_b + h_o v_{ce} \quad (6)$$

4.2.2 h-parameter Model of Common Base Configuration

The base terminal is common between input and output terminals in common base configuration of a BJT. The equivalent circuit in terms of h-parameters of common base configuration of BJT is shown in Fig. 4.

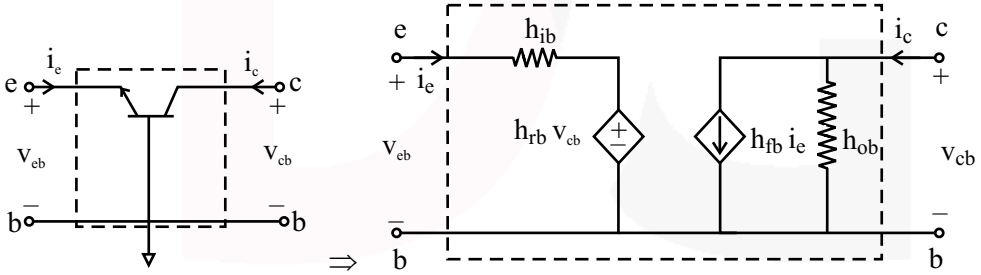


Fig. 4 Equivalent circuit of common base configuration of BJT as two port network

The input and output signals of common base configuration can be related in terms of h-parameter of the configuration as under,

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb} \quad (7)$$

$$i_c = h_{fb} i_e + h_{ob} v_{cb} \quad (8)$$

4.2.3 h-parameter Model of Common Collector Configuration

The collector terminal is common between input and output terminals in common collector configuration of a BJT. The equivalent circuit in terms of h-parameters of common collector configuration of BJT is shown in Fig. 5.]

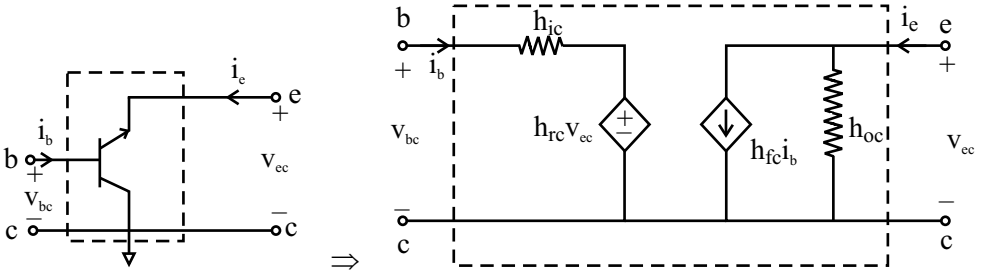


Fig. 5 Equivalent circuit of common collector configuration of BJT as two port network

The input and output signals of common collector configuration can be related in terms of h-parameter of the configuration as under,

$$v_{bc} = h_{ic} i_b + h_{rc} v_{ec} \quad (9)$$

$$i_e = h_{fc} i_b + h_{oc} v_{ec} \quad (10)$$

4.2.4 Relation between h-parameters

Case-I : he *h*-parameters of common-collector configuration in terms of *h*-parameters of common emitter configuration is given as under,

i) $h_{ic} = h_{ie}$ (11)

ii) $h_{rc} = 1$ (12)

iii) $h_{fc} = -(1 + h_{fe})$ (13)

iv) $h_{oc} = h_{oe}$ (14)

Case-II: The h-parameters of common base configuration in terms of h-parameters of common-emitter configurations are given as under,

i) $$h_{ib} = \frac{h_{ie}}{1 + h_{fe}} \quad (15)$$

ii) $$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re} \quad (16)$$

iii) $$h_{fb} = -\frac{h_{fe}}{1 + h_{fe}} \quad (17)$$

iv) $$h_{ob} = \frac{h_{oe}}{1 + h_{fe}} \quad (18)$$

4.2.5 Graphical Method of measurement of h-parameters

The h-parameter model of BJT are related to input and output signals. The h-parameters of CE configuration can be given as under,

$$h_{ie} = \frac{\partial v_{be}}{\partial i_b} \approx \frac{\Delta v_{be}}{\Delta i_b}\bigg|_{V_{CE}=\text{fixed}} \tag{19}$$

$$h_{re} = \frac{\partial v_{be}}{\partial v_{ce}} \approx \frac{\Delta v_{be}}{\Delta v_{ce}}\bigg|_{I_B=\text{fixed}} \tag{20}$$

$$h_{fe} = \frac{\partial i_c}{\partial i_b} \approx \frac{\Delta i_c}{\Delta i_b}\bigg|_{V_{CE}=\text{fixed}} \tag{21}$$

$$h_{oe} = \frac{\partial i_c}{\partial v_{ce}} \approx \frac{\Delta i_c}{\Delta v_{ce}}\bigg|_{I_B=\text{fixed}} \tag{22}$$

The input characteristics of BJT give relation between v_{be}, i_b and v_{ce} which are used for determination of h_{ie} and h_{re} The output characteristics give relation between i_c, v_{ce} and i_b, which are used for determination of h_{fe} and h_{oe}.

Case-I : Determination of h_{fe}

Consider the output characteristics shown in Fig.6. Let, base current is varies from I_{B1} to I_{B2} for a fixed collector to emitter voltage V_{CE} , then corresponding variation in collector current is from I_{C1} to I_{C2}.

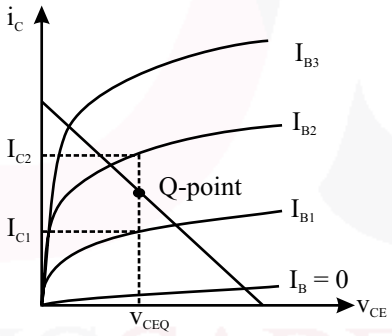


Fig. 6 Determination of the parameter h_{fe} with output characteristics of BJT

For small signal variation,

$$\Delta i_b = I_{B2} - I_{B1}$$

$$\Delta i_c = I_{C2} - I_{C1}$$

Then,
$$h_{fe} = \frac{\Delta i_c}{\Delta i_b}\bigg|_{V_{CB}=\text{fixed}} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} \tag{23}$$

Case-II : Determination of h_{oe}

Consider output characteristics of BJT shown in Fig. 7. Let base current is fixed at I_{BQ}. Let voltage v_{ce} is varied from V_{CE1} to V_{CE2} and the corresponding variation in collector current i_C is from I_{C1} to I_{C2}.

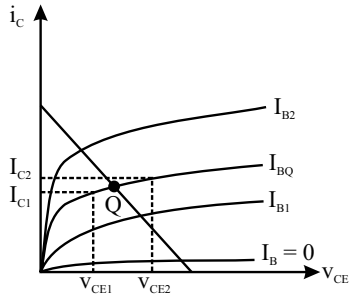


Fig. 7 Determination of the parameter h_{oe} with output characteristics of BJT

For small signal variations,

$$\Delta v_{ce} = V_{CE2} - V_{CE1}$$

$$\Delta i_c = I_{C2} - I_{C1}$$

Then,
$$h_{fe} = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{V_{CB}=\text{fixed}} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}} \qquad (24)$$

Case-III : Determination of h_{ie}

Consider input characteristics of BJT as shown in Fig.8. Let,voltage V_{CE} is kept constant and base to emitter voltage is varied from V_{BE1} to V_{BE2} and corresponding change in base current is from I_{B1} and I_{B2}.

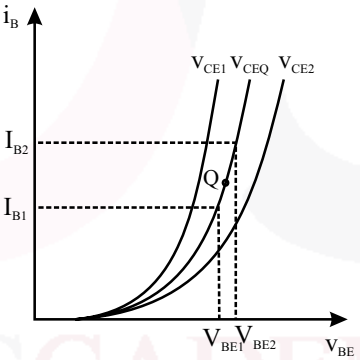


Fig. 8 Determination of the parameter h_{ie} with input characteristics of BJT

For small signal variation,

$$\Delta v_{be} = V_{BE2} - V_{BE1}$$

$$\Delta i_b = I_{B2} - I_{B1}$$

$\therefore$
$$h_{ie} = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE}=\text{fixed}} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}} \qquad (25)$$

Case-IV : Determination of h_{re}

Consider input characteristics of BJT as shown in Fig. 9. Let, the base current s fixed and voltage v_{CE} is varied from V_{CE1} to V_{CE2} and corresponding variation in v_{BE} is from V_{BE1} to V_{BE2}.

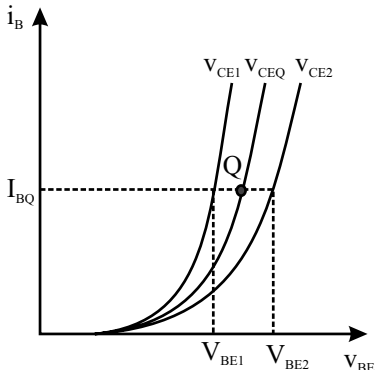


Fig. 9 Determination of the parameter h_{re} with input characteristics of BJT

For small signal variation,

$$\Delta v_{CE} = V_{CE2} - V_{CE1}$$

$$\Delta v_{BE} = V_{BE2} - V_{BE1}$$

Then meter,

$$h_{re} = \left.\frac{\Delta v_{BE}}{\Delta v_{CE}}\right|_{I_B=\text{fixed}} = \frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}} \quad (26)$$

As input and output characteristics of BJT can be determined experimentally so the h-parameters can be measured experimentally.

4.2.6 Variations of h-parameter of BJT

The h-parameters of BJT are sensitive to variations in collector current, collector to emitter voltage and temperature.

Case-I : Variation with respect to collector current magnitude

The variations of h-parameters with collector current for fixed value of V_{CE}, frequencies temperature are shown in Fig.10

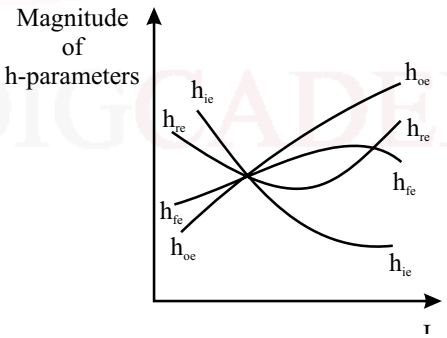


Fig. 10 Variations in h-parameters with collector current

Observations :

i. h_{ie} decreases with increase in collector current.

ii. h_{oe} increases with increase in collector current .

iii. h_{ie} first decreases then increases with increases collector current.

iv. h_{fe} first increases then decreases with increase in collector current.

v. h_{fe} is least sensitive and h_{oe} is most sensitive to variation in collector current.

Case-II : Variation with collector to emitter voltage (V_{CE})

The variation in h-parameter with voltage V_{CE} are shown in Fig. 11. It is observed that h_{oe} & h_{re} are must more sensitive to variation in V_{CE}. and h_{ie} & h_{fe} are less sensitive to variations in V_{cc}. The parameter h_{fe} in least sensitive to variations in I_C as well at V_{CE} so it is assumed to be constant for small signal variations.

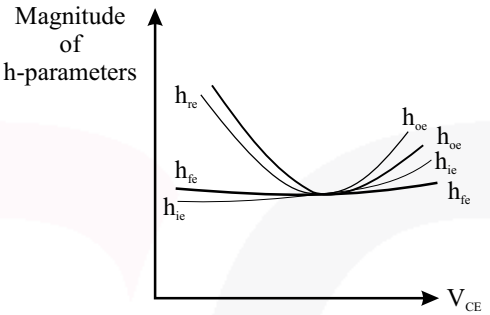


Fig. 11 Variations in h-parameters with collector to emitter voltage

Case-III : Variation of h-parameters with temperature.

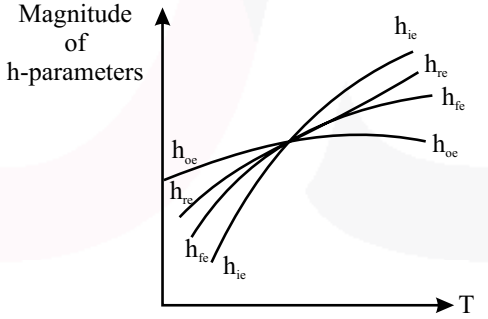


Fig. 12 Variations in h-parameters with temperature

Observations :

i. h_{ie} is most sensitive to temperature

ii. h_{oe} is least sensitive to temperature.

iii. All the parameter increase with increase in temperature.

4.2.7 Values of *h*-parameters of various configuration

The values of h-parameters for different configurations of BJT are given in Table 1 below.

Table 1 : Values of h-parameters

	Parameter	Common Emitter	Common Collection	Common Base
1.	h_i	1100 Ω	1100 Ω	21.6 Ω
2.	h_r	$+2.5\times10^{-4}$	1	2.9×10^{-4}
3.	h_f	+50	–51	–0.98
4.	h_o	24μ A/ V	25μ A/ V	0.49μ A/ V
5.	$\frac{1}{h_o}$	40 kΩ	40 kΩ	2.04 MΩ

Note : *i. h-parameters of a BJT can be measured directly using simple experiments. The h-parameters of BJT can be determined from static characteristics of BJT.*

ii. h-parameters vary over wide range with variation in temperature.

iii. h-parameters are functions of biasing currents. The parameter h_{fe} , first increases, reaches at peak and then decreases with increase in emitter current.

iv. h-parameters are real numbers at audio frequencies.

4.3 Analysis of an amplifier with h-parameters model

Consider a BJT amplifier connected to a source having impedance Z_S and load with impedance Z_L as shown in Fig. 13(a). The source is connected to the BJT amplifier through an input coupling capacitor C_{Ci} and load is connected to amplifier output through an output coupling capacitor C_{Co}. The coupling capacitors are used to couple the input and output AC signals with DC biasing circuit of BJT. These capacitors are designed to pass the AC signals and block DC biasing signals of BJT from entering into input and output circuits of the amplifier. The coupling capacitors are replaced with open circuit for DC analysis and by short circuit for AC analysis of the amplifier. The emitter resistance of the BJT is bypassed with a capacitor called emitter bypass capacitor. The emitter bypass capacitor is replaced by short circuit for AC analysis and by an open circuit for DC analysis of the amplifier. The BJT amplifier behaves like a two port network. It can be replaced by a block diagram representing two port network as shown in Fig. 13(b). The input voltage and output current of the amplifier, acting as a two port network, are given in terms of h-parameters of the amplifier a under

$$v_1 = h_i i_1 + h_r v_2 \quad (27)$$

$$i_2 = h_f i_1 + h_o v_2 \quad (28)$$

The voltage at output port can be given by,

$$v_2 = Z_L i_L = -Z_L i_2 \quad (29)$$

Current gain :

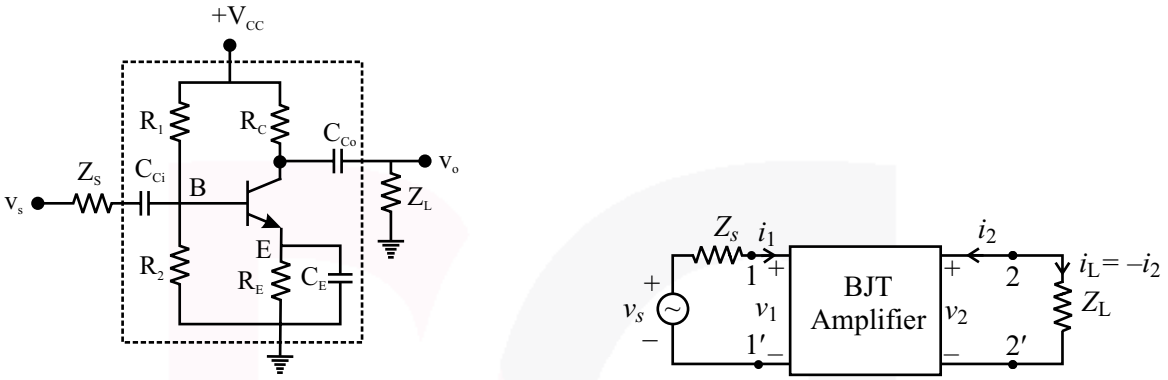
Putting expression of v_2 from (29) in equation (28), we have,

$$i_2 = h_f i_1 + h_o(-Z_L i_2)$$

$$\Rightarrow \quad \frac{i_2}{i_1} = \frac{h_f}{h_o Z_L + 1}$$

Current gain, $$A_I = \frac{i_L}{i_1} = -\frac{i_2}{i_1} \quad (30)$$

$$\Rightarrow \boxed{A_I = -\frac{h_f}{1 + h_o Z_L}} \quad (31)$$



(a) BJT amplifier circuit **(b) Block diagram of BJT amplifier as 2-port network**

Fig. 13 BJT amplifier as two port network connected to load

Input Impedance :

From equation (27), input impedance can be given as,

$$Z_i = \frac{v_1}{i_1} = h_i + h_r \frac{v_2}{i_1} \quad (32)$$

but, $$v_2 = -Z_L i_2$$

$$\Rightarrow Z_i = h_i + h_r \times \left(-Z_L \frac{i_2}{i_1}\right) = h_i + h_r Z_L \cdot \left(\frac{-i_2}{i_1}\right)$$

$$\Rightarrow \boxed{Z_i = h_i + h_r Z_L A_I} \quad (33)$$

Putting expression of A_I from equation (31) in above equation, we have,

$$Z_i = h_i - \frac{h_r h_f}{1 + Z_L h_o} Z_L \quad (34)$$

$$\Rightarrow \boxed{Z_i = h_i - \frac{h_r h_f}{Y_L + h_o}} \quad (35)$$

where, $Y_L = 1/Z_L =$ admittance of the load.

Voltage gain :

$$A_v = \frac{v_2}{v_1} = \frac{v_2}{(-i_2)} \cdot \frac{(-i_2)}{i_1} \cdot \frac{i_1}{v_1} \tag{36}$$

$$\boxed{A_v = \frac{Z_L \cdot A_I}{Z_i}} \tag{37}$$

Putting expression of A_I from equation (23) in above equation, we have,

$$\boxed{A_v = \frac{-Z_L}{Z_i} \cdot \frac{h_f}{1 + h_o Z_L}} \tag{38}$$

Voltage gain with source impedance taken into account:

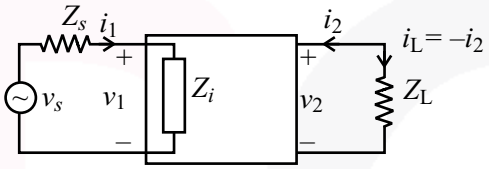


Fig. 14 Effect of Source impedance on voltage gain of BJT amplifier as two port network

The voltage gain of the amplifier can be given as,

$$A_{vs} = \frac{v_2}{v_s} = \frac{v_2}{v_1} \cdot \frac{v_1}{v_s} = A_v \cdot \frac{v_1}{v_s} \tag{39}$$

Putting expression of voltage gain , A_v, from equation (29) in above equation,

$$\Rightarrow \quad A_{vs} = \frac{Z_L}{Z_i} \cdot A_I \cdot \frac{v_1}{v_s} \tag{40}$$

Applying voltage divider rule on input side, we have,

$$v_1 = \frac{Z_i}{Z_i + Z_s} \cdot v_s$$

$$\Rightarrow \quad \frac{v_1}{v_s} = \frac{Z_i}{Z_i + Z_s} \tag{41}$$

From equations (39) and (41), we have,

$$\Rightarrow \quad A_{vs} = \frac{Z_i}{Z_i + Z_s} \cdot A_v \tag{42}$$

From equations (37) and (41), we have,

$$\Rightarrow \quad A_{vs} = \frac{Z_i}{Z_i + Z_s} \cdot \frac{Z_L}{Z_i} \cdot A_I \tag{43}$$

$$\Rightarrow \quad \boxed{A_{vs} = \frac{Z_L}{Z_i + Z_s} . A_I} \tag{44}$$

Current gain with source impedance taken into account:

Let input to the amplifier is a current source. Then the circuit of the amplifier can be drawn as shown in Fig.7.

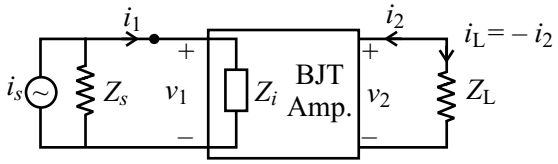


Fig. 15 Effect of Source impedance on current gain of BJT amplifier as two port network

Current gain of the amplier can be given by,

$$A_{Is} = \frac{-i_2}{i_s} = -\frac{i_2}{i_1} . \frac{i_1}{i_s} = \frac{i_1}{i_s} . A_I \tag{45}$$

Applying current divider rule on input side, we have,

$$i_1 = \frac{Z_s}{Z_s + Z_i} . i_s \tag{46}$$

$$\therefore \quad \boxed{A_I \quad \frac{}{Z_s \quad Z_i} . A_I} \tag{47}$$

Output admittance:

Output admittance can be obtained in terms of source impedance by replacing load impedance by an ideal source and input source by its internal impedance as shown in Fig.8. The port signals of the network shown in Fig.8 can be given as,

$$v_1 = h_i i_1 + h_r v_2 \tag{48}$$

$$i_2 = h_f i_1 + h_o v_2 \tag{49}$$

$$v_1 = -Z_s i_1 \tag{50}$$

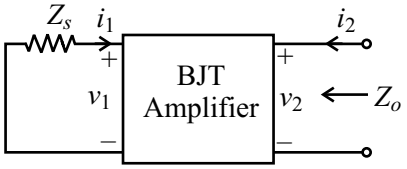


Fig. 16 Output impedance of BJT amplifier as two port network

From equation (48) and (50), we have,

$$-Z_s i_1 = h_i i_1 + h_r v_2$$

$$\Rightarrow \qquad i_1 = -\frac{h_r}{Z_s + h_i} . v_2 \qquad (51)$$

From equations (49) and (51), we have,

$$i_2 = \left[h_f \times \frac{-h_r}{h_i + Z_s} + h_o \right] v_2$$

Output admittance, $\boxed{Y_O = \frac{i_2}{v_2} = h_O - \frac{h_f h_r}{h_i + Z_s}}$ (52)

Summary :

i) Current gain,

(a) With out source impedance,

$$A_I = \frac{-h_f}{1 + Z_L h_o}$$

(b) with source impedance

$$A_{Is} = \frac{Z_s}{Z_s + Z_i} . A_I$$

ii) Input Impedance

$$Z_i = h_i + h_r Z_L A_I = h_i - \frac{h_r h_f}{Y_L + h_o}$$

iii) Voltage gain

(a) Without source impedance,

$$A_v = \frac{Z_L}{Z_i} . A_I$$

(b) With source impedance,

$$A_{vs} = \frac{Z_L}{Z_i + Z_s} A_I = \frac{Z_i}{Z_i + Z_s} . A_v$$

iv) Output Admittance

$$Y_o = h_o - \frac{h_f h_r}{h_i + Z_s}$$

4.4 Approximate h-parameter model and Amplifier Analysis

A BJT can also be represented by its approximate h-parameter model having $h_r = 0$ and $h_o = 0$. The port signals of the two network represented by approximated h-parameter mode of BJT can be given as,

$$v_1 = h_i i_1 \quad (53)$$

$$i_2 = h_f i_1 \quad (54)$$

The equivalent circuit of BJT amplifier using approximate h-parameter model can be drawn as shown in Fig. 17.

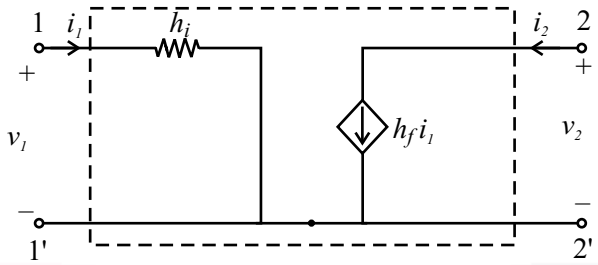


Fig. 17 Approximate h-parameter model of BJT

The parameters of amplifier using approximate h-parameter model can be given as under,

Current gain:

(a) Current gain without considering source resistance is given by,

$$A_I = \frac{-h_f}{1 + Z_L h_o} \quad (55)$$

For approximate h-parameter model, $h_o = 0$

$$\therefore \quad \boxed{A_I = -h_f} \quad (56)$$

(b) Current gain by considering source resistance is given by,

$$A_{Is} = \frac{Z_s}{Z_s + Z_i} . A_I \quad (57)$$

Putting expression of A_I from equation (48) in above equation, we have,

$$\therefore \quad \boxed{A_{Is} = -\frac{Z_s}{Z_s + h_i} h_f} \quad (58)$$

Input Impedance:

The input impedance of B JT amplifier is given by,

$$Z_i = h_i - \frac{h_r h_f}{Y_L + h_o} \quad (59)$$

Putting $h_r = 0$ and $h_o = 0$, we have,

$$\boxed{Z_i = h_i} \quad (60)$$

Voltage gain:

(a) Voltage gain without considering source resistance is given by,

$$A_v = \frac{Z_L}{Z_i} A_I \tag{61}$$

Putting expression of A_I from equation (48) in above equation, we have,

$$\boxed{A_v = -\frac{Z_L}{h_i} h_f} \tag{62}$$

(b) Voltage gain by considering source resistance is given by,

$$A_{vs} = \frac{Z_i}{Z_i + Z_s} A_v = \frac{Z_L}{Z_i + Z_s} A_I \tag{63}$$

$$\Rightarrow \quad A_{vs} = \frac{h_i}{h_i + Z_s} \times \frac{-Z_L h_f}{h_i} = -\frac{Z_L h_f}{h_i + Z_s} \tag{64}$$

$$\Rightarrow \quad \boxed{A_{vs} = -\frac{Z_L h_f}{h_i + Z_s}} \tag{65}$$

Output Admittance:

The output admittance of BJT amplifier is given by,

$$Y_o = h_o - \frac{h_r h_f}{Z_s + h_i} \tag{66}$$

Putting $h_r = 0$ and $h_o = 0$, we have,

$$Y_o = 0 \tag{67}$$

4.5 Diode model of BJT

The diode model of BJT is shown in Fig. 18. The diode in the model represents the emitter to base pn junction of BJT. It is not a commonly used model for analysis of BJT amplifier.

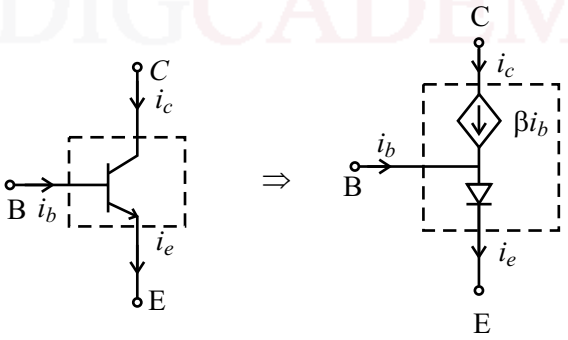


Fig. 18 BJT and its diode model

4.6 r_e, r_π, r_o and g_m parameters of BJT

The parameters r_e, r_π and g_m are used for small signal analysis of BJT. However, these parameters are

determined using DC analysis of the BJT.

i) Transconductance of BJT

The transconductance of BJT is defined as,

$$g_m = \frac{\partial i_c}{\partial v_{be}} \tag{68}$$

The collector current in terms of voltage V_{BE} is given by,

$$i_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{69}$$

The transconductance can be given in terms of DC bias collector current as under,

$$\boxed{g_m = \frac{I_C}{V_T}} \tag{70}$$

where, V_T is thermal voltage and I_c is DC bias collector current.

The thermal voltage is given as,

$$V_T = \frac{T}{11600} = \frac{kT}{q} \tag{71}$$

Where T is temperature in Kelvin.

At T = 300 K $V_T = 26$ mV

and $g_m = \frac{I_C}{26}$; where I_C is in mA (72)

ii) Emitter Resistance (r_e)

It is resistance seen from emitter terminal of BJT. The emitter resistance is similar to dynamic resistance of a pn junction diode. Mathematically,

$$\boxed{r_e = \frac{V_T}{I_E}} \tag{73}$$

where, I_E is DC bias emitter current.

iii) Base resistance (r_π)

It is resistance seen from base terminal of BJT. The base resistance of BJT is defined as,

$$r_b = \frac{\partial v_{be}}{\partial i_b}$$

The base current is also denoted by symbol r_π. The base resistance can be given in terms of DC bias base current as under,

$$\boxed{r_\pi = \frac{V_T}{I_B}} \tag{74}$$

where, I_B is DC bias base current.

iii) Output resistance (r_o)

The output resistance of BJT is resistance seen from collector terminal with emitter terminal grounded. The output resistance is observed due to early effect or base width modulation effect of BJT. If the early effect is taken into account the collector current of BJT becomes,

$$I_C = I_S e^{V_{BE}/V_T}\left(1+\frac{V_{CE}}{V_A}\right) \tag{75}$$

Where V_A is early voltage of BJT.

The early effect gives rise to the output resistance of a BJT which is given by,

$$r_o = \left(\frac{\partial I_C}{\partial V_{CE}}\right)^{-1} \tag{76}$$

$$\Rightarrow \quad r_0 = \left(I_S e^{V_{BE}/V_T} \times \frac{1}{V_A}\right)^{-1} = \frac{V_{CE}+V_A}{I_C} \tag{77}$$

$$r_0 = \frac{V_A}{I_C'} \tag{78}$$

Where, $I_C' = I_S e^{V_{BE}/V_T}$ = collector current without early effect

Relation between g_m and r_e

From equations (70) and (73), we have,

$$g_m r_e = \frac{I_C}{I_E} = \alpha$$

$$\Rightarrow \quad g_m r_e = \alpha \tag{79}$$

Relationship between g_m and r_π

From equations (70) and (74), we have,

$$g_m r_\pi = \frac{I_C}{I_B} = \beta$$

$$\Rightarrow \quad g_m r_\pi = \beta \tag{80}$$

Relationship between r_π and r_e

The emitter resistance given by equation (73) can be modified as under,

$$r_e = \frac{V_T}{I_B + I_C} = \frac{V_T}{I_B\left(1+\frac{I_C}{I_B}\right)} \tag{81}$$

$$\Rightarrow \qquad r_e = \frac{r_\pi}{1+\beta} \tag{82}$$

$$\Rightarrow \qquad \boxed{r_\pi = (1+\beta)\, r_e} \tag{83}$$

4.6.1 r_e-model or T-model of BJT

For small signal analysis a forward biased diode, of diode model of BJT shown in Fig. 18, can be replaced by its dynamic resistance. Than the diode model can be redrawn as r_e model, as shown in Fig. 19.

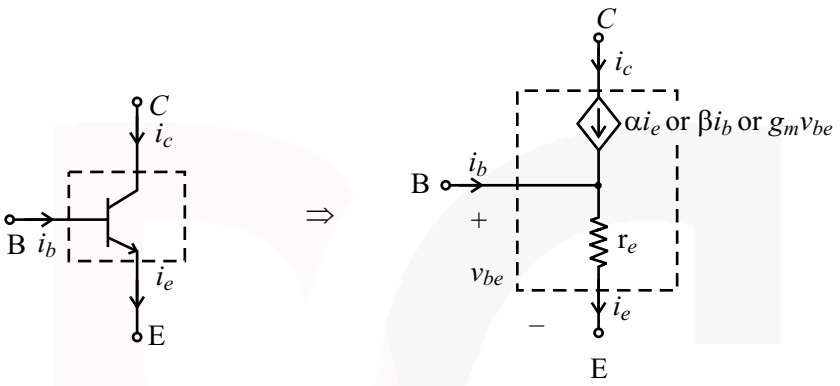


Fig. 19 BJT and its r_e- model

Note : *r_e-model of transistor is also called T-model.*

4.6.2 π -model of BJT

Case-I : Neglecting Early Effect

The π-model of BJT consists of base or input resistance of the BJT and dependent current source on collector side as shown in Fig. 20. It is a most commonly used model for analysis of a BJT amplifier.

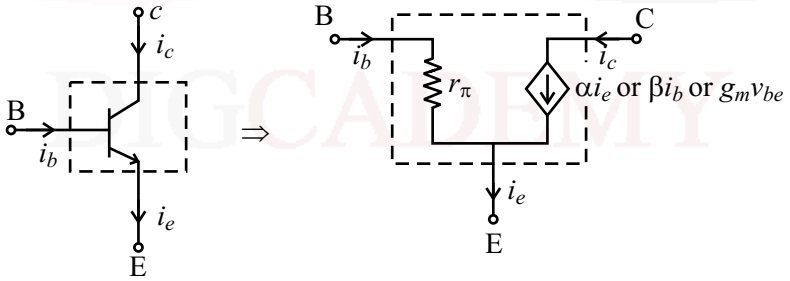


Fig. 20 BJT and its π-model without output resistance

Case-II : With Early Effect

The early effect gives rise to the output resistance of BJT seen from capacitor terminal. The output resistance of BJT is connected between collector and emitter terminals in π-model of BJT with early effect taken into account. The π-model of BJT with early effect taken into account is as shown in Fig. 21.

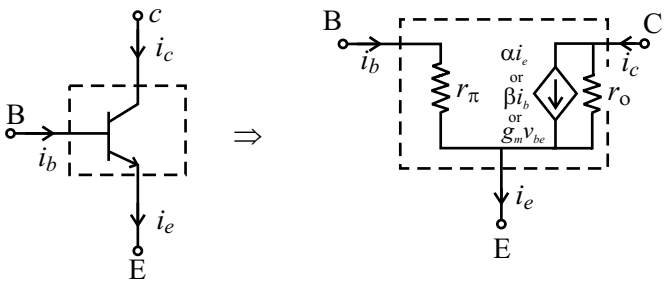


Fig. 21 BJT and its π-model with output resistance

Example 1

A bipolar transistor is operating in the active region with a collector current of 1 mA. Assuming that the β of the transistor is 100 and the thermal voltage (V_T) is 25 mV, the transconductance (g_m) and the input resistance (r_π) of the transistor in the common emitter configuration, are

(a) $g_m = 25$ mA/V and $r_\pi = 15.625$ kΩ

(b) $g_m = 40$ mA/V and $r_\pi = 4.0$ kΩ

(c) $g_m = 25$ mA/V and $r_\pi = 2.5$ kΩ

(d) $g_m = 40$ mA/V and $r_\pi = 2.5$ kΩ

GATE(EC/2004/2M)

Solution : Ans.(d)

Given, $I_C = 1$ mA, $V_T = 25$ mV and $\beta = 100$

Transconductance of BJT, is given by,

$$g_m = \frac{I_C}{|V_T|}$$

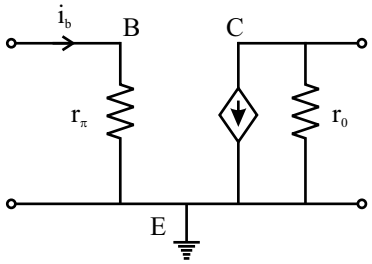
$$\Rightarrow \quad g_m = \frac{1}{25} = 40 \text{ mA/V}$$

Input resistance is given by,

$$r_{be}' = r_\pi = \frac{\beta}{g_m} = \frac{100}{40}\text{k}\Omega = 2.5 \text{ k}\Omega$$

Example 2

The current i_b through the base of a silicon npn transistor is $1 + 0.1 \cos(10000\pi t)$ mA.At 300 K, the r_π in the small signal model of the transistor is



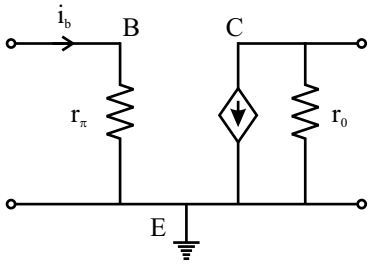
(a) 250 Ω

(b) 27.5 Ω

(c) 25 Ω (d) 22.5 Ω

GATE(EC/2012/1M)

Solution : Ans.(c)



The r_π resistance of CE configuration of BJT is given as

$$r_\pi = \frac{V_T}{I_B}$$

where I_B = DC bias base current

and $V_T = \frac{T}{11600}$ = Thermal voltage

T = Temperature in K

At T = 300 K, $V_T = \frac{300}{11600}$

Given, $i_b = 1 + 0.1 \cos 10000\pi t$ mA

From given base current,

$$I_B = 1 \text{ mA}$$

$$\Rightarrow \quad r_\pi = \frac{300}{11600} \times \frac{1}{1\times10^{-3}} = 25.8\ \Omega$$

Example 3

A BJT is biased in forward active mode. Assume V_{BE} = 0.7 V, kT/q = 25 mV and reverse saturation current $I_s = 10^{-13}$ A. The transconductance of the BJT (in mA/V) is _____

GATE(EC-I/2014/2M)

Solution : Ans.: 5.7 to 5.9

Given, $V_{BE} = 0.7\text{V}$

$$\frac{kT}{q} = 25 \text{ mV} = V_T$$

Reverse saturation current, $I_s = 10^{-13}$ A

The collector current of BJT in forward active mode is given by

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$\Rightarrow \qquad I_C = 10^{-13} e^{\frac{0.7}{25\times10^{-3}}} = 0.145A$$

The transconductance of BJT ,

$$g_m = \frac{I_C}{V_T} = \frac{0.145}{25\times10^{-3}} = 5.8 \text{ A/V}$$

4.7 Comparison of approximate *h*-parameter model and π model of BJT

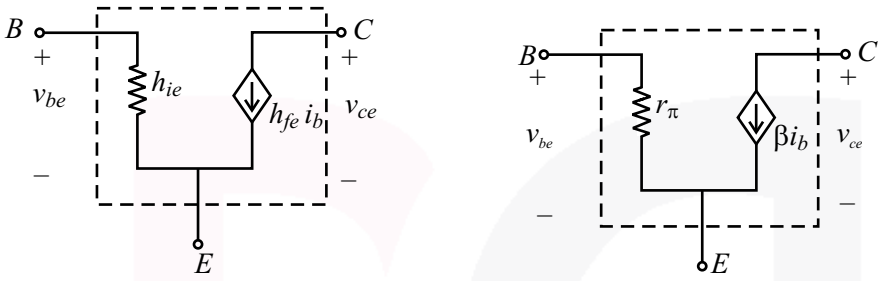


Fig. 22 Comparison of approximate h-parameter model and π-model of BJT

Comparing above two models,

$$\boxed{r_\pi = h_{ie}} \tag{84}$$

and

$$\boxed{\beta = h_{fe}} \tag{85}$$

4.8 Small Signal Analysis of Potential Divider Biased CE Amplifier

The potential divider bias arrangement of common emitter amplifier normally consists of potential divider circuit used to provide biasing voltage at base terminal of the BJT. An resistance is connected in series with the emitter terminal is to provide self bias characteristics of BJT. However, emitter resistance reduces the gain, increases the input impedance and increases the bandwidth of the amplifier. It also provides negative feedback in the base-emitter circuit and reduces the non-linear distortion of the amplifier. A bypass capacitor is sometimes connected across the emitter resistance to compensate the effect of emitter resistance on input impedance, gain and bandwidth of the amplifier in small signal applications. Following sections discusses the CE amplifier with and without emitter bypass capacitor.

4.8.1 Small Signal Analysis of Potential Divider Biased CE Amplifier Without Emitter Bypass Capacitor

The common emitter potential divider bias amplifier with input and output bypass capacitors and emitter resistance is shown in the Fig. 23. The emitter resistance provides negative feedback in the input base circuit. The emitter resistance increase the input impedance, reduces the gain, increases the bandwidth and reduces the non-linear distortion of the amplifier. The small signal analysis of

the amplifier can be done using different small signal models of BJT which are discussed in the following sections.

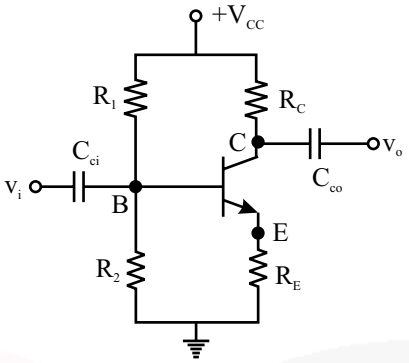


Fig. 23. Common emitter potential divider bias amplifier with emitter resistance

Case-I : Analysis Using Approximate h-parameter Model of BJT

The small signal equivalent circuit of the above amplifier can be drawn by replacing coupling capacitors by the short circuit, the biasing supply VCC by ground and BJT by its approximate h-parameters model as shown in Fig 24

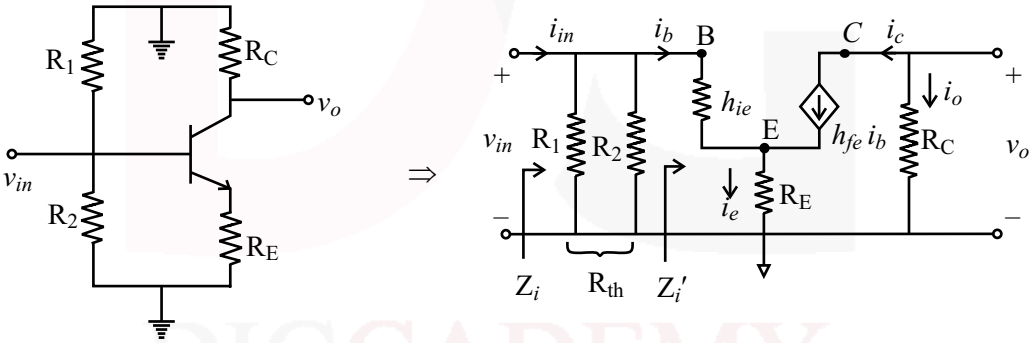


Fig. 24. Common emitter potential divider bias amplifier with emitter resistance

Input Impedance :

Applying KCL at emitter terminal in above circuit, we have,

$$i_e = i_c + i_b = h_{fe}\, i_b + i_b = (1 + h_{fe})\, i_b$$

Applying KVL in base circuit,

$$v_{in} = h_{ie}\, i_b + R_E\, i_e = [h_{ie} + (1 + h_{fe})R_E]\, i_b \qquad (86)$$

Input impedance seen from base terminal can be given by,

$$Z_i' = \frac{v_{in}}{i_b} = h_{ie} + (1 + h_{fe})\, R_E \qquad (87)$$

Total impedance of amplifier.

$$\boxed{Z_i = R_{th} \parallel Z_i'} \quad (88)$$

where, $R_{th} = \dfrac{R_1 R_2}{R_1 + R_2}$ = Thenvenin's equivalent resistance of potential divider (89)

Note : When, R_E =0, $Z_i' = h_{ie}$, thus, input impedance of amplifier increases by (1 + h_{fe})R_E when R_E is connected in emitter ckt.

Voltage Gain :

From collector circuit, $v_o = -i_c R_C = -h_{fe} i_b R_C$

From eq.(86), $i_b = \dfrac{v_{in}}{h_{ie} + (1 + h_{fe}) R_E}$

$$\frac{v_o}{v_{in}} = \frac{-R_C h_{fe}}{h_{ie} + (1 + h_{fe}) R_E}$$

Voltage gain, $\boxed{\dfrac{v_o}{v_{in}} = A_v = -\dfrac{R_C h_{fe}}{h_{ie} + (1 + h_{fe}) R_E}}$ (90)

Note : i. Here negative sign indicates that the output signal has a phase shift of 180° with respect to the phase of input signal. Because of this characteristic CE amplifier is used as phase inverter.

ii. When R_E = 0, voltage gain,

$$A_v = \boxed{A_I = \frac{i_o}{i_{in}} = -\frac{R_{th}}{R_{th} + h_{ie}} . h_{fe}} \quad . \quad (90a)$$

Thus, the voltage gain of the amplifier increases if emitter resistance is bypassed

Current Gain :

Considering the load connected at collector with $R_L = R_C$

$$i_o = -i_c = -h_{fe} i_b$$

From input circuit,

$$i_b = \frac{R_{th}}{R_{th} + Z_i'} . i_{in} \quad (91)$$

$$\Rightarrow \quad i_o = -h_{fe} . \frac{R_{th}}{R_{th} + Z_i'} . i_{in}$$

Current gain, $A_i = \dfrac{i_o}{i_{in}} = -\dfrac{h_{fe} R_{th}}{R_{th} + Z_i'}$

$$\Rightarrow \quad \boxed{A_I = -\frac{h_{fe} R_{th}}{R_{th} + h_{ie} + (1 + h_{fe}) R_E}} \tag{92}$$

Note : When $R_E = 0$, $A_i = -\dfrac{R_C h_{fe}}{R_C + h_{fe}}$ (93)

Thus, current gain of the amplifier increases if emitter resistance is bypassed.

Output Impedance :

Output impedance is obtained by setting $v_{in} = 0$. The base current becomes zero when input is zero. The collector current, $i_c = \beta i_b$, also becomes zero when base current is zero and current dependent current source in collector circuit behaves as open circuit. The equivalent circuit for obtaining output impedance becomes as shown in Fig. 25.

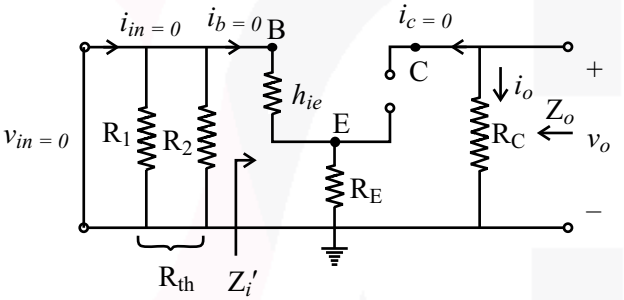


Fig. 25. Equivalent circuit of potential divider bias CE amplifier for obtaining output impedance

The output impedance of the circuit becomes,

$$Z_o = R_C \tag{94}$$

Case-II : Analysis using π- model of BJT

The AC equivalent circuit of amplifier, with BJT replaced by its π - model, becomes as shown in Fig.26.

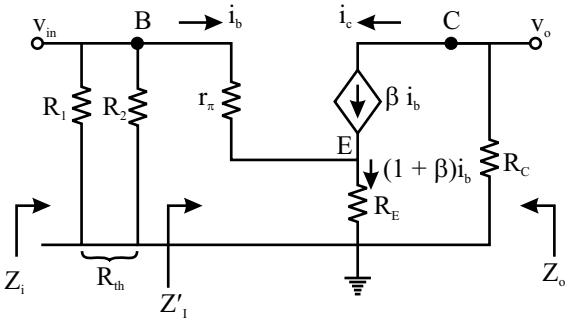


Fig. 26. Equivalent circuit of potential divider bias CE amplifier using p-model

Input Impedance :

From input circuit, $v_{in} = r_\pi i_b + (1+\beta) R_E i_b$ (95)

$$Z'_i = \frac{v_{in}}{i_b} = r_\pi + (1+\beta) R_E \quad (96)$$

Input impedance, $Z_i = R_1 \| R_2 \| Z'_i = R_{th} \| Z'_i = \frac{R_{th} Z'_i}{R_{th} + Z'_i}$ (97)

Where, $R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$ (98)

Note : i. When, $R_E = 0$, $Z_i' = r_\pi$ and $Z_i = \frac{R_{th} r_\pi}{R_{th} + r_\pi}$

ii. When R_E is connected in emitter circuit, the input impedance, Z_i', of amplifier increases by $(1 + \beta)R_E$.

Voltage gain :

Output voltage, $v_o = R_C i_c = -\beta R_C i_b$ (99)

Putting expression of i_b from equation (95) in above equation, we have,

$$v_o = -\frac{\beta R_C}{r_\pi + (1+\beta) R_E} v_{in} \quad (100)$$

Voltage gain, $A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi + (1+\beta) R_E}$ (101)

Note : When, $R_E = 0$, $A_v = -\frac{\beta R_C}{r_\pi}$ (102)

Thus, the voltage gain of the amplifier increases if emitter resistance is bypassed

Current gain :

Output current, $i_o = -i_c = -\beta i_b$

From input circuit, $i_b = \frac{R_{th}}{R_{th} + Z'_i} \times i_{in}$

$\Rightarrow$ $i_0 = -\frac{\beta R_{th}}{R_{th} + Z'_i} \times i_{in}$

Current gain, $$A_i = \frac{i_o}{i_{in}} = -\frac{\beta R_{th}}{R_{th} + Z_i'} \quad (103)$$

$$\Rightarrow \quad \boxed{A_i = -\frac{\beta R_{th}}{R_{th} + r_\pi + (1+\beta)R_E}} \quad (104)$$

Output Impedance :

Output impedance is obtained by setting $v_{in} = 0$. The base current becomes zero when input is zero. The collector current $i_c = \beta i_b$ becomes zero when base current is zero and dependent current source behaves like an open circuit. Then, output impedance of the circuit becomes,

$$Z_o = R_c \quad (105)$$

4.8.2 Small Signal Analysis of Potential Divider Biased CE Amplifier With Emitter Bypass Capacitor

Fig. 27 shows a common emitter amplifier with potential divider bias and emitter bypass capacitor. The emitter bypass capacitor increases the gain, reduces the input impedance and reduces the bandwidth of the amplifier. The small signal analysis of the amplifier can be done using different small signal models of BJT which are discussed in the following sections.

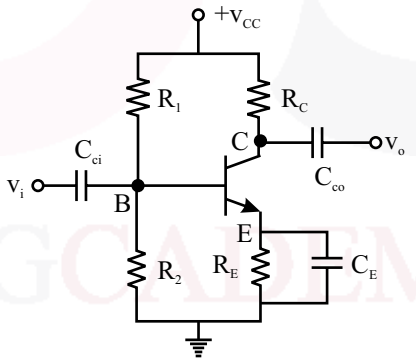


Fig. 27 Potential divider bias CE amplifier with emitter bypass capacitor

Case-I : Analysis using approximate h-parameter model.

The AC equivalent circuit of the amplifier is obtained by short circuiting the coupling and bypass capacitors, replacing DC biasing voltage source by ground and replacing BJT by its approximate h-parameter model as shown in Fig. 28,

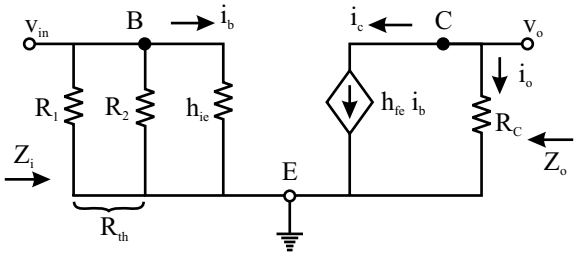


Fig. 28. AC equivalent circuit of potential divider bias CE amplifier with emitter bypass capacitor using h-parameter

Input Impedance :

From input circuit, $Z_i = R_1 \| R_2 \| h_{ie} = R_{th} \| h_{ie}$

$$\Rightarrow \quad Z_i = \frac{R_{th}\, h_{ie}}{R_{th} + h_{ie}} \tag{106}$$

Where, $$R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{107}$$

Voltage Gain :

Output voltage, $$v_o = -R_C\, i_c = -\, h_{fe}\, R_C\, i_b \tag{108}$$

Base current, $$i_b = \frac{v_{in}}{h_{ie}}$$

$$\therefore \quad v_o = -\frac{h_{fe}\, R_C}{h_{ie}} v_{in}$$

Voltage gain, $$\boxed{A_v = \frac{v_o}{v_{in}} = -\frac{h_{fe}\, R_C}{h_{ie}}} \tag{109}$$

Current Gain :

Output current, $$i_o = -i_c = -\, h_{fe}\, i_b$$

From input circuit, $$i_b = \frac{R_{th}}{R_{th} + h_{ic}} \times i_{in}$$

$$\Rightarrow \quad i_o = -\frac{h_{fe}\, R_{th}}{R_{th} + h_{ie}} \times i_{in} \tag{110}$$

Current, gain, $$\boxed{A_i = \frac{i_o}{i_{in}} = -\frac{h_{fe} R_{th}}{h_{ie} + R_{th}}} \tag{111}$$

Output Impedance :

The impedance seen across output terminal with input set zero,

$$Z_o = R_c \tag{112}$$

Case-II : Analysis using π-model of BJT

The AC equivalent circuit of the amplifier is obtained by short circuiting the coupling and bypass capacitors, replacing DC biasing voltage source by ground and replacing BJT by its approximate h-parameter model as shown in Fig. 29.

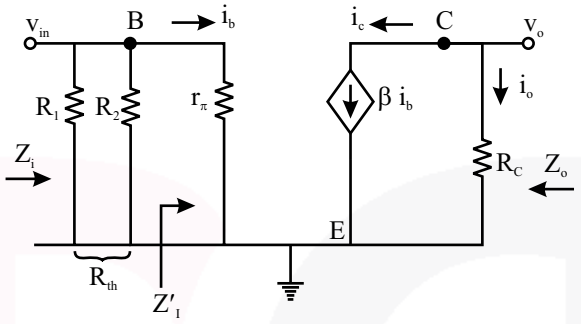


Fig. 29. AC equivalent circuit of potential divider bias CE amplifier with emitter bypass capacitor using h-parameter

Input Impedance :

Input impedance of the circuit,

$$Z_i = R_1 \| R_2 \, r_\pi = R_{th} \| r_\pi = \frac{R_{th} r_\pi}{R_{th} + r_\pi} \tag{113}$$

Where,
$$R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{114}$$

Voltage Gain :

Base current, $i_b = \dfrac{v_{in}}{r_\pi}$

Output voltage, $v_o = -\beta \, i_b \, R_C$

$\Rightarrow$ $v_o = \dfrac{\beta R_C}{r_\pi} v_{in}$

Voltage gain,
$$A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi} \tag{115}$$

Current Gain :

Base current, $i_b = \dfrac{R_{th}}{R_{th} + r_\pi} \times i_{in}$

Output current, $i_o = -i_c = -\beta i_b$

$$\Rightarrow \qquad i_o = -\frac{\beta R_{th}}{R_{th} + r_\pi} \times i_{in}$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = -\frac{\beta R_{th}}{R_{th} + r_\pi} \qquad (116)$$

Output Impedance :

The impedance seen across output terminals with input v_{in} set to zero is,

$$Z_o = R_C \qquad (117)$$

Case-III : Analysis using π-model of BJT with output resistance

The AC equivalent circuit of amplifier, with BJT replaced by its π-model with output resistance of BJT, becomes as under,

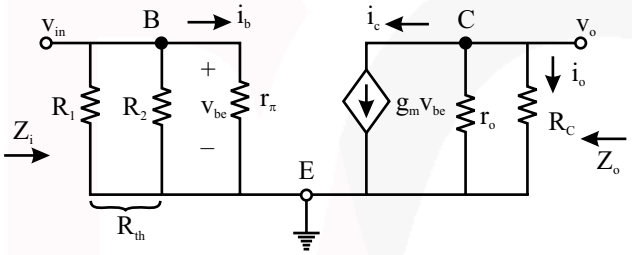


Fig. 30 AC equivalent circuit of potential divider bias CE amplifier with emitter bypass capacitor using p-model and output resistance of BJT

Input Impedance:

From input circuit, $$Z_i = R_1 \| R_2 \| r_\pi = R_{th} \| r_\pi = \frac{R_{th}\, r_\pi}{R_{th} + r_\pi} \qquad (118)$$

When $$R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \qquad (119)$$

Voltage Gain :

Output voltage, $$v_o = -\, g_m v_{be} \times \frac{r_o R_C}{R_o + R_C} \qquad (120)$$

From input circuits, $$v_{be} = v_{in}$$

$$\therefore \qquad v_o = -\frac{g_m r_o R_C}{r_o + R_C} \times v_{in} \qquad (121)$$

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = -\frac{g_m r_o R_C}{r_o + R_C} \qquad (122)$$

Current Gain :

Output current, $$i_o = -\frac{r_o}{r_o + R_C} \times g_m v_{be} \quad (123)$$

From input circuit, $$v_{be} = Z_i i_{in}$$

$$\Rightarrow \quad i_o = \frac{r_o g_m Z_i}{r_o + R_C} \times i_{in} \quad (124)$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = -\frac{g_m r_o Z_i}{r_o + R_C} \quad (125)$$

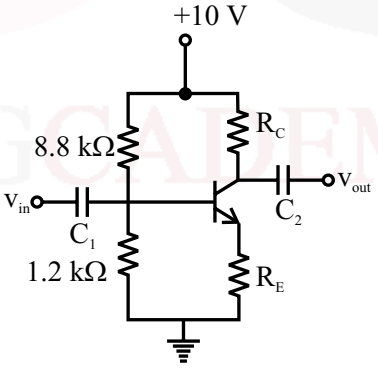
Output impedance :

Output impedance is obtained by setting $v_{in} = 0$. The voltage v_{be} becomes zero when v_{in} is zero and voltage dependent current source $g_m v_{be}$ behaves like open circuit. Under such condition, the impedance seen across output terminals becomes,

$$Z_o = r_o \| R_C = \frac{r_o R_C}{r_o + R_C} \quad (126)$$

Example 4

In the amplifier circuit shown below,assume V_{BE}= 0.7V and the β of the transistor and the values of C_1 and C_2 are extremely high. If the amplifier is designed such that at the quiescent point its V_{CE}= $\frac{V_{CC}}{2}$, where V_{CC} is the power supply voltage, its small signal voltage gain $\left|\frac{v_{out}}{v_{in}}\right|$ will be

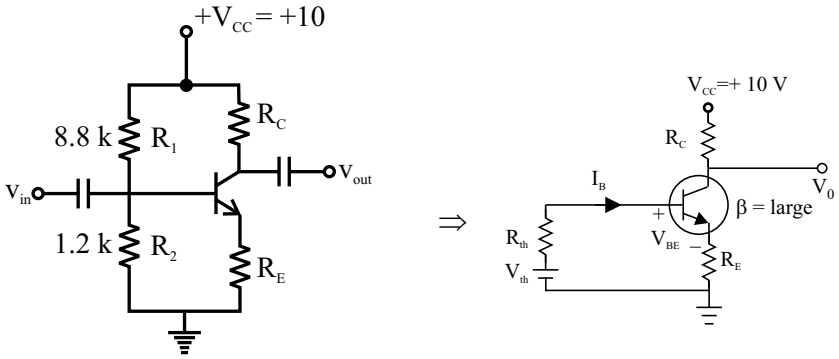


(a) 3.75 (b) 4.5

(c) 9 (d) 19

GATE(IN/2008/2M)

Solution : Ans.(c)



Thevenin's equivalent voltage and resistance seen from the base,

$$R_{th} = \frac{1.2 \times 8.8}{1.2 + 8.8} = 1.056 \text{ k}$$

$$V_{th} = \frac{1.2}{1.2 + 8.8} \times 10 = 1.2 \text{ V}$$

From the collector circuit, we have,

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

Emitter current of BJT, $I_E = \left(1 + \frac{1}{\beta}\right) I_C$

when β is large, $I_E = I_C$

$\Rightarrow$ $I_E(R_C + R_E) = V_{CC} - V_{CE}$

Given, $V_{CE} = V_{CC}/2 = 10/2 = 5$ V

$\Rightarrow$ $I_E(R_C + R_E) = 10 - 5 = 5$ V ....(i)

From the base circuit, we have,

$$V_{th} - I_B R_{th} - I_E R_E - V_{BE} = 0$$

when β is large the base current is negligible.

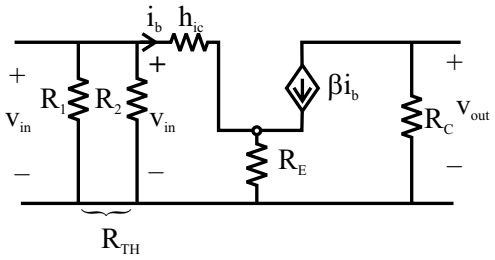
$\Rightarrow$ $I_E R_E = V_{th} - V_{BE} = 1.2 - 0.7 = 0.5$ V

$\Rightarrow$ $I_E = 0.5 / R_E$ .....(ii)

Rrom (i) and (ii) we have,

$$R_C/R_E = 9 \quad \text{.....(iii)}$$

A.C. equivalent circuit of amplifiers,



$$R_{TH} = \frac{1.2 \times 8.8}{1.2 + 8.8} = 1.056 \text{ k}$$

Thevenin's equivalent voltage at the base,

$$V_{th} = \frac{1.2}{8.8 + 1.2} \times 10 = 1.2\text{V}$$

Base current, $$i_b = \frac{V_i}{h_{ie} + (1+\beta)R_E}$$

Since, β is very large, so $$i_b \approx \frac{V_i}{\beta R_E}$$

From output circuit, $$V_o = -\beta i_b \times R_C = -\frac{R_C}{R_E} \cdot V_i$$

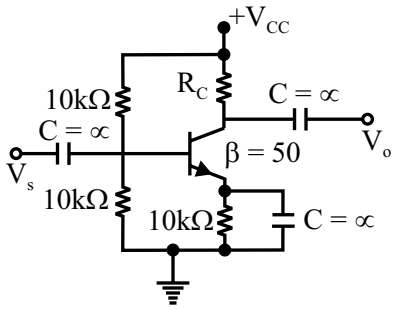
$$\Rightarrow \quad \frac{V_o}{V_i} = -\frac{R_C}{R_E}$$

$$\Rightarrow \quad \left|\frac{V_o}{V_i}\right| = \frac{R_C}{R_E} \qquad \text{.....(iv)}$$

From (iii) and (iv), $$\left|\frac{V_o}{V_i}\right| = 9$$

Example 5

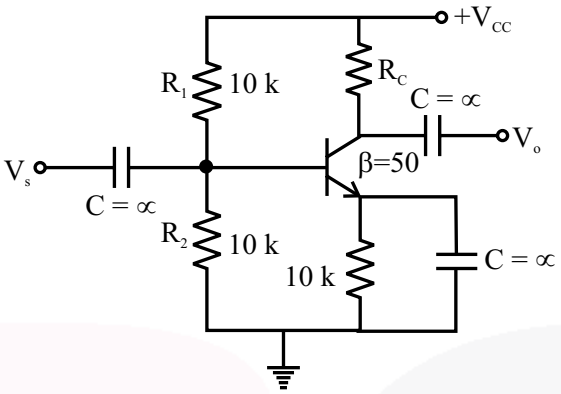
The transconductance g_m of the transistor shown in figure is 10 mS. The value of the input resistance R_{IN} is



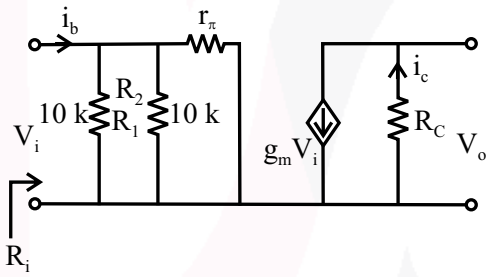
(a) 10.0 kΩ (b) 8.3 kΩ
(c) 5.0 kΩ (d) 2.5 kΩ

GATE(EE/2004/2 M)

Solution : Ans.(d)



Replacing BJT by is equivalent π model the ac equivalent circuit of amplifier becomes, (capacitances are short circuit for a.c. equivalent circuit),



The parameter r_π is given by,

$$r_\pi = \frac{V_T}{|I_B|} = \frac{\beta}{g_m}$$

Given, $g_m = 10 \text{ ms}$

$$\Rightarrow \quad r_\pi = \frac{50}{10 \times 10^{-3}}$$

$$\Rightarrow \quad r_\pi = 5000\ \Omega = 5\text{k}$$

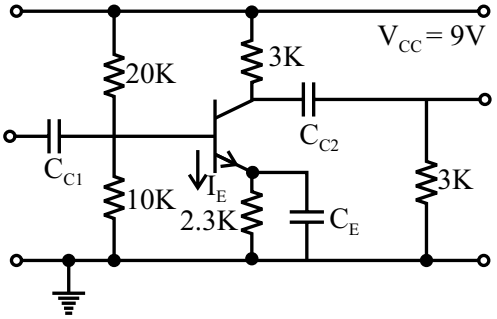
Input resistance of amplifier,

$$R_i = R_1 | |R_2| |r_\pi = 10\ \text{k}\Omega \,||10\ \text{k}\Omega \,||5\ \text{k}\Omega$$

$$\Rightarrow \quad R_i = 2.5\ \text{k}\Omega$$

Example 6

Statement for Linked to part (i) & part (ii) :



In the following transistor circuit, $V_{BE} = 0.7$ V, $r_e = 25$ mV/I_E, and β and all the capacitances are very large.

(i) The value of DC current I_E is

(a) 1 mA (b) 2 mA

(c) 5 mA (d) 10 mA

GATE(EC/2008/2M)

(ii) The mid-band voltage gain of the amplifier is approximately.

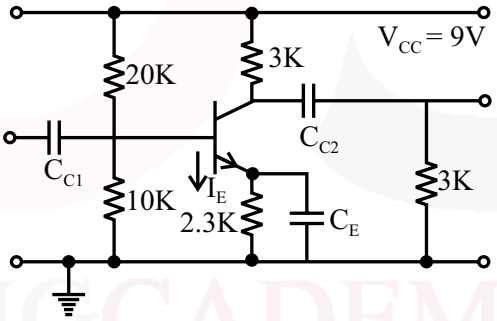
(a) –180 (b) – 120

(c) – 90 (d) – 60

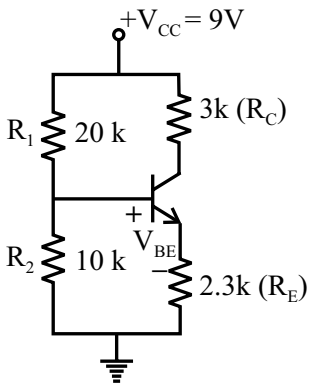
GATE(EC/2008/2M)

Solution :

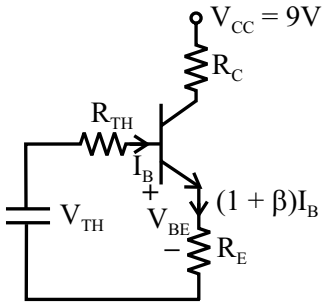
(i) Ans.(a)



The capacitances behave like open circuit for D.C. So D.C. biasing circuit becomes as under,



Above circuit can be redrawn as under,



where, $$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{10 \times 20}{10 + 20} = \frac{20}{3}\text{k}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{1}{3} \times 9 = 3$$

Base current, $$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

Emitter current, $$I_E = (1 + \beta)\, I_B$$

$$I_E = (1+\beta)\frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

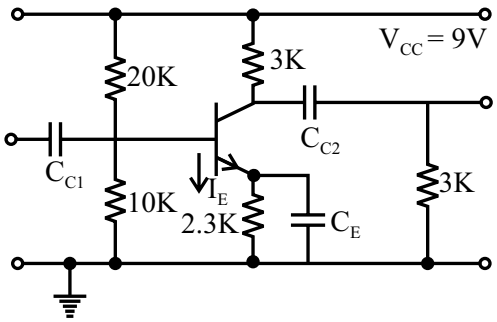
Since β is large

$$R_{TH}+(1+\beta)\, R_E \approx (1 + \beta)\, R_E$$

$$\Rightarrow \quad I_E = (1+\beta)\cdot\frac{V_{TH} - V_{BE}}{(1+\beta)R_E} = \frac{V_{TH} - V_{BE}}{R_E}$$

$$\Rightarrow \quad I_E = \frac{3 - 0.7}{2.3} = 1\text{mA}$$

(ii) Ans.(d)



$V_{TH} = 3V,$

$$R_{TH} = \frac{20}{3}k$$

Emitter current, $$I_E = (1+\beta)\cdot\frac{V_{TH}-V_{BE}}{R_{TH}+(1+\beta)R_E}$$

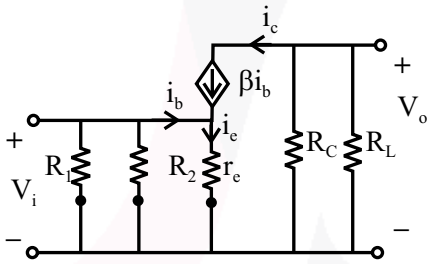
As β is large so emitter current can be approximated as under,

$$\Rightarrow \quad I_E = \frac{V_{TH}-V_{BE}}{R_E} = 1\,mA$$

Given, $$r_e = \frac{25mV}{I_E}$$

$$\Rightarrow \quad r_e = \frac{25}{1} = 25\Omega$$

Replacing BJT by its r_e model, and short circuiting the bypass and coupling capacitors the ac equivalent circuit of amplifier can be drawn as under,



Emitter current, $$i_e = (1+\beta)i_b = \frac{V_i}{r_e}$$

Base current, $$i_b = \frac{V_i}{(1+\beta)r_e}$$

$$V_o = -\frac{R_C R_L}{R_C+R_L}\cdot\frac{\beta}{(1+\beta)r_e}V_i$$

voltage gain, $$\frac{V_o}{V_i} = -\frac{R_C R_L}{R_C+R_L}\cdot\frac{\beta}{(1+\beta)r_e}$$

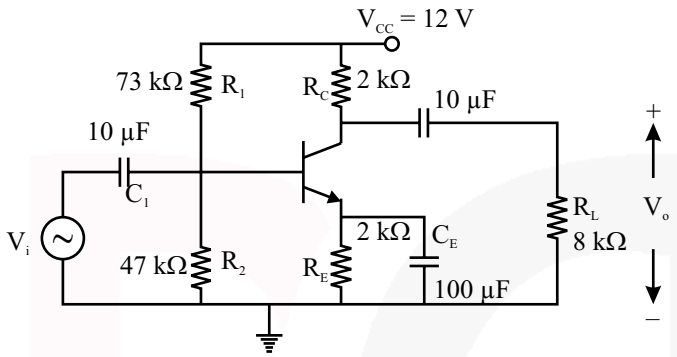
For large β, $$\frac{\beta}{1+\beta} \approx 1$$

$$\Rightarrow \quad \frac{V_o}{V_i} = -\frac{R_C R_L}{R_C+R_L}\cdot\frac{1}{r_e}$$

$$\Rightarrow \quad \frac{V_o}{V_i} = -\frac{3\times10^3}{2}\cdot\frac{1}{25} = -60$$

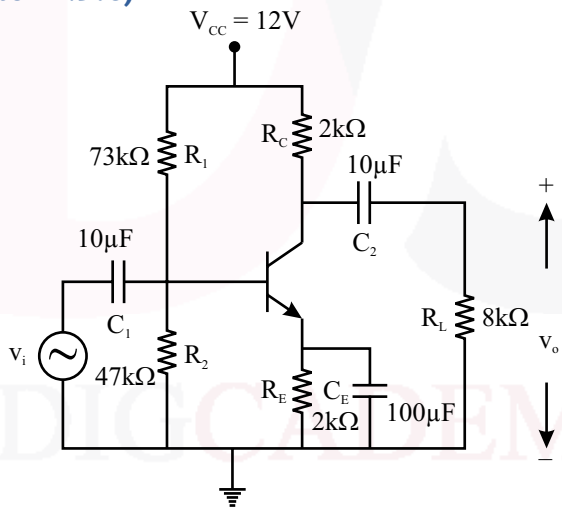
Example 7

For the DC analysis of the Common-Emitter amplifier shown, neglect the base current and assume that the emitter and collector current are equal. Given that $V_T = 25mV$, $V_{BE} = 0.7V$, and the BJT output resistance r_0 is practically infinite. Under these conditions, the midband voltage gain magnitude. $A_c = |V_0/V_i|$ V/V, is _____.



GATE(EC-I/2017/2M)

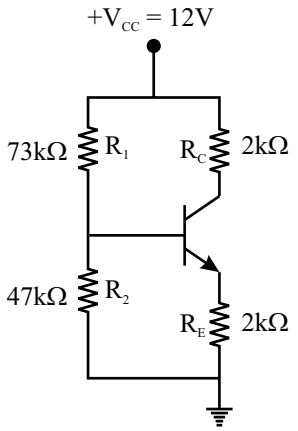
Solution : Ans. (127.0 to 129.0)



The transistor parameter for ac analysis for finding the voltage gain of the amplifier can be obtained using DC analysis as follows.

Case -I : DC Analysis

For DC analysis the coupling and emitter bypass capacitor are replaced by optn circuit as under,



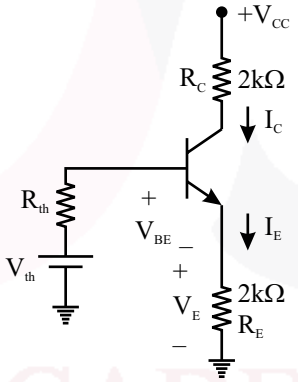
Above circuit can be drawn by replacing potential divider by its Thevenin's, equivalent as follows,

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{cc} = \frac{47}{73+47} \times 12$$

$$\Rightarrow \quad V_{th} = 4.7\ V$$

And

$$R_{th} = \frac{47 \times 73}{47 + 73}$$



When base current is neglected,

$$V_E = V_{th} - V_{BE} = 4.7 - 0.7 = 4V$$

Emitter current, $I_E = \frac{V_E}{R_E} = \frac{4}{2k} = 2mA$

Collector current, $I_C = I_E = 2mA$

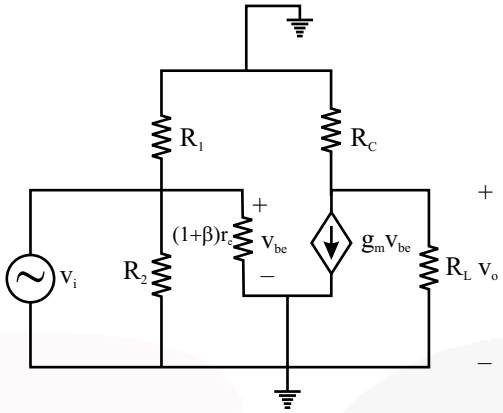
Transconductance of BJT,

$$g_m = \frac{I_C}{V_T} = \frac{2}{25} = 0.08$$

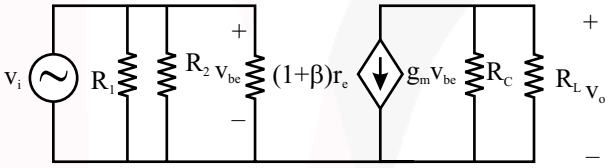
Emitter resistance, $r_e = \frac{V_T}{I_E} = \frac{25}{2} = 12.5\Omega$

Case-II : AC Analysis

Replacing coupling and bypass capacitors by short circuit, biasing voltage by short circuit or ground and BJT by its small signal model, the AC equivalent circuit becomes as under,



Above circuit can be redrawn as under,



Output voltage, $v_o = -(R_C \| R_L)\, g_m\, v_{be}$

From input circuit, $v_i = v_{be}$

$\Rightarrow$ $v_o = -(R_C \| R_L)\, g_m\, v_i$

Voltage gain,

$$|A_v| = \left|\frac{v_o}{v_{in}}\right| = \frac{R_C R_L}{R_C + R_L} \times g_m$$

$\Rightarrow$ $$|A_v| = \frac{2\times 8}{2+8} \times 0.08 \times 10^3 = 128$$

4.9 Small Signal Analysis of Base Bias Amplifier

The biasing of base of BJT in base bias circuit is provided directly at base through a resistance connected between supply voltage and base terminal as shown in Fig. 31. An resistance is connected in series with the emitter terminal is to provide self bias characteristics of BJT.

4.9.1 Small Signal Analysis of Base Bias Amplifier with Emitter Resistance

Fig. 31 shows a base bias common emitter amplifier with emitter resistance. The input and output signals are connected to the amplifier through the input and output coupling capacitors. The small signal analysis of the amplifier can be done using different small signal models of BJT which are discussed in the following sections

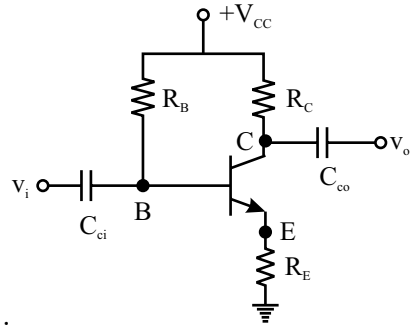


Fig. 31 Base bias amplifier with emitter resistance

Case I : Analysis of Using Approximate h-parameter Model of BJT

Replacing coupling capacitor C_{ci} and C_{co} by short circuit, power supply $+V_{cc}$ by ground and BJT by its approximate h-parameter model, the small signal equivalent of the amplifier becomes as shown in Fig. 32.

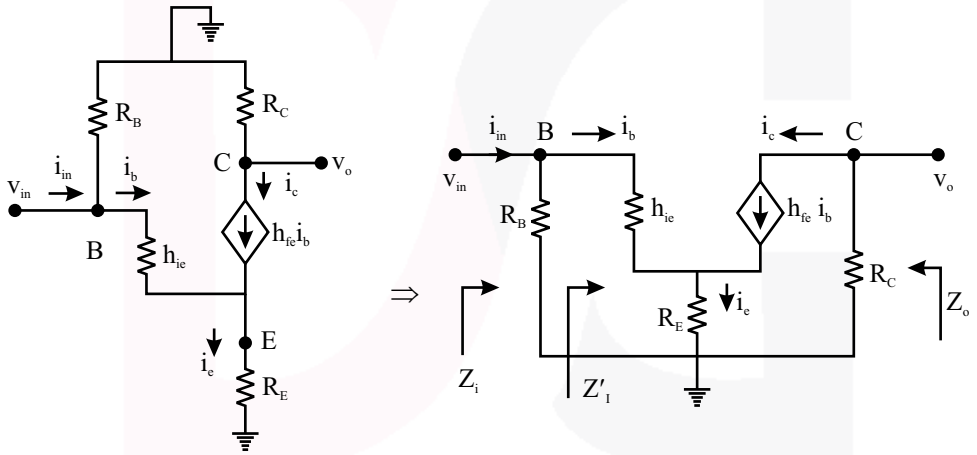


Fig. 32. AC equivalent circuit of base bias CE amplifier with emitter resistance using h-parameters

Input impedance :

Applying KVL on input side we have,

$$v_{in} = h_{ie}\, i_b + R_E\, i_e \tag{127}$$

Emitter current, $$i_E = i_b + i_c = i_b + h_{fe}\, i_b = (1 + h_{fe})\, i_b \tag{128}$$

$\Rightarrow$ $$v_{in} = h_{ie}\, i_b + (1 + h_{fe})\, i_b R_E \tag{129}$$

$$Z_i' = \frac{v_{in}}{i_b} = h_{ie} + R_E\,(1 + h_{fe})\, i_b \tag{130}$$

$\Rightarrow$ $$Z_i = R_B \,||\, Z_i' = \frac{R_B Z_i'}{R_B + Z_i'} \tag{131}$$

Voltage gain:

Let, the load is connected in collector.

Then output voltage $v_o = -R_C i_c = -R_C h_{fe} i_b$ (132)

Putting expression of base current from equation (129) in above equation, we have,

$$v_o = -\frac{R_C h_{fe}}{h_{ie} + (1 + h_{fe}) R_E} v_{in} \quad (133)$$

$$\Rightarrow \quad A_v = \frac{v_o}{v_{in}} = -\frac{R_C h_{fe}}{h_{ie} + (1 + h_{fe}) R_E} \quad (134)$$

Output Impedance

Output resistance of an amplifier is resistance seen from output terminals by setting input supply to zero. Connect independent source at output when input supply is set to zero or grounded the ac equivalent circuit of the amplifier become as under,

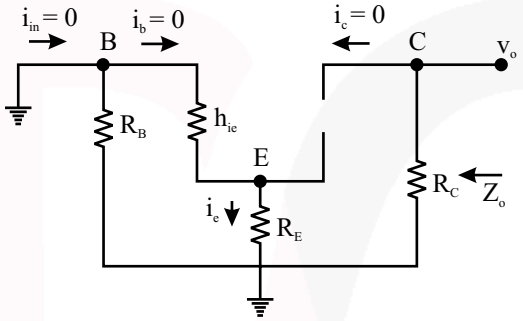


Fig. 33. AC equivalent circuit of base bias CE amplifier for output resistance

The resistance seen across output terminals,

$$Z_o = R_C \quad (135)$$

Case-II Analysis using π– model

Replacing coupling capacitors by short circuit, DC supply source by ground and BJT by its p – model, the small signal equivalent circuit of amplifier becomes as shown in Fig. 34.

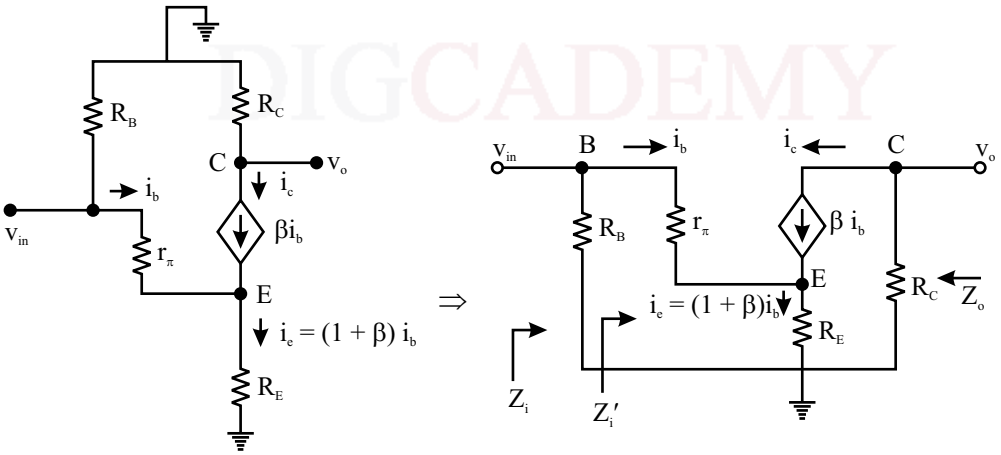


Fig. 34. AC equivalent circuit of base bias CE amplifier with emitter resistance using p-parameters

Input Impedance :

From input circuit, $v_{in} = r_\pi i_b + (1+\beta)R_E i_b$ (136)

$$Z_i' = \frac{v_{in}}{i_b} = r_\pi + (1+\beta)R_E \quad (137)$$

Input impedance, $Z_i = R_B \| Z_i' = \frac{R_B Z_i'}{R_B + Z_i'}$ (138)

Voltage Gain :

Output voltage $v_o = -h_{fe} R_C i_b$ (139)

Putting expression of base current from equation (136) in above relation, we have,

$$v_o = -\frac{h_{fe} R_C}{r_\pi + (1+\beta)R_E} v_{in} \quad (140)$$

Voltage, gain, $$\boxed{A_v = \frac{v_o}{v_i} = -\frac{h_{fe} R_C}{r_\pi + (1+\beta)R_E}} \quad (141)$$

Output Impedance :

Output Impedance is obtained by setting $v_i = 0$ and connecting a source across output terminals as in case-I.

When $v_i = 0$, base current, $i_b = 0$ and the output impedance becomes, ∴

$$\boxed{Z_o = R_C} \quad (142)$$

4.9.2 Analysis of Base Bias CE Amplifier with Emitter Bypass Capacitor

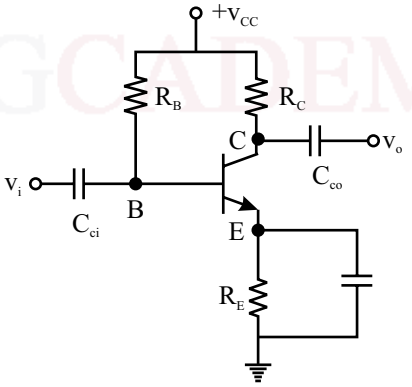


Fig. 35 Base bias amplifier with emitter bypass capacitor

When emitter resistance is by passed with a by pass capacitor, it is replaced by a short circuit for AC analysis.

Case-I : Analysis using approximate h-parameter model

Replacing coupling capacitors emitter by pass capacitor by short circuit, power supply by ground and BJT by its approximate h-parameters model the equivalent circuit for small signal analysis becomes as shown in Fig.36.

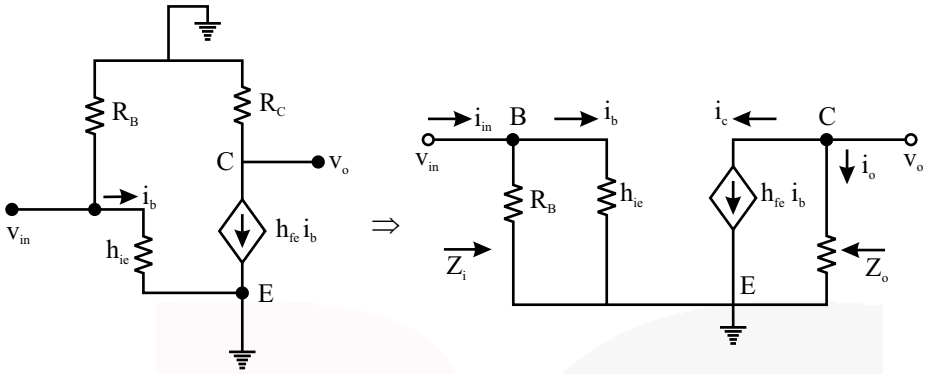


Fig. 36. AC equivalent circuit of base bias CE amplifier with emitter bypass capacitor using h-parameters

Input Impedance :

From input circuit, $$\boxed{Z_i = R_B \,||\, h_{ie} = \frac{R_B\, h_{ie}}{R_B + h_{ie}}} \qquad (143)$$

Voltage Gain :

Output voltage, $$v_o = -R_C\, i_o = -R_C\, h_{fe}\, i_b \qquad (144)$$

Base current, $$i_b = \frac{v_{in}}{h_{ie}} \qquad (145)$$

$$\Rightarrow \quad v_o = \frac{R_C\, h_{fe}}{h_{ie}} \cdot v_{in} \qquad (146)$$

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = -\frac{R_C\, h_{fe}}{h_{ie}} \qquad (147)$$

Current Gain :

Output current, $$i_o = -i_c = -h_{fe}\, i_b \qquad (148)$$

Base current, $$i_b = \frac{R_B}{R_B + h_{ie}} \cdot i_{in} \qquad (149)$$

$$\Rightarrow \quad i_o = -\frac{h_{fe}\, R_B}{h_{ie} + R_B} \cdot i_{in} \qquad (150)$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = -\frac{R_B h_{fe}}{h_{ie} + R_B} \quad (151)$$

Output Resistance :

Output resistance of amplifier is obtained by setting input $v_{in} = 0$ and then finding resistance seen across output terminals of the amplifier. When input is set to zero, the base current, $i_b = 0$

$\therefore \quad i_c = \beta i_b = 0$

Then equivalent circuit of amplifier becomes as shown in Fig. 37.

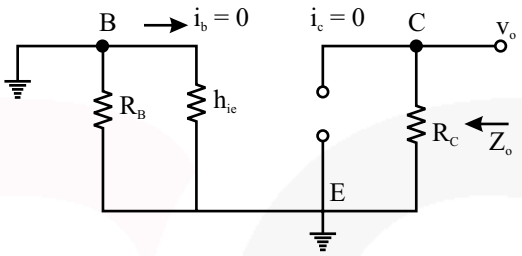


Fig. 37 AC equivalent circuit of base bias CE amplifier with h-parameter for output resistance

Output resistance, $$Z_o = R_C \quad (152)$$

Case-II : Analysis using π – model of BJT

The AC equivalent circuit of amplifier with BJT replaced by its π – model becomes as shown below,

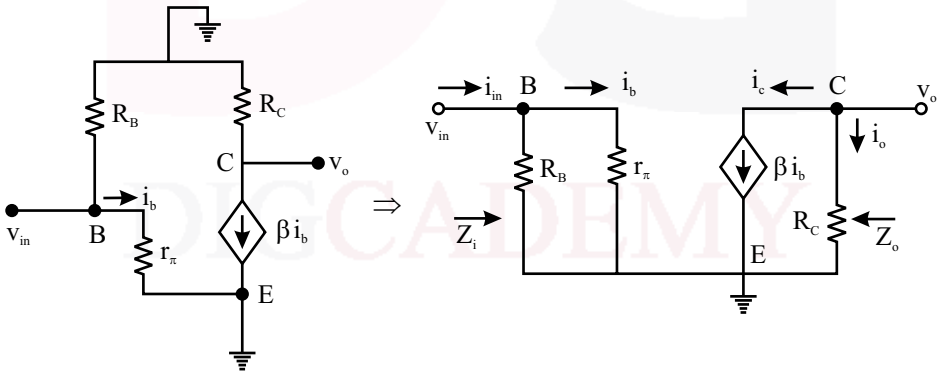


Fig. 38 AC equivalent circuit of base bias CE amplifier with emitter bypass capacitor using π -model

Input Resistance :

From input circuit, $$Z_i = \frac{v_{in}}{i_{in}} = \frac{R_B r_\pi}{R_B + r_\pi} \quad (153)$$

Voltage Gain :

Base current, $i_b = \frac{v_{in}}{r_\pi}$

Output voltage, $v_o = -R_C i_C = -R_C \beta i_b = -R_C \beta \times \frac{v_{in}}{r_\pi}$ (154)

Voltage gain, $\boxed{A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_C}{r_\pi}}$ (155)

Current Gain :

Output current, $i_o = -i_c = -\beta i_b$

From input circuit, $i_b = \frac{R_B}{R_B + r_\pi} \times i_{in}$ (156)

$\Rightarrow$ $i_o = -\frac{\beta R_B}{R_B + r_\pi} \times i_{in}$ (157)

Current gain, $\boxed{A_i = \frac{i_o}{i_{in}} = -\frac{\beta R_B}{R_B + r_\pi}}$ (158)

Output resistance :

Output resistance of amplifier is resistance seen across output terminals with input source set to zero. The equivalent circuit for output resistance becomes as under,

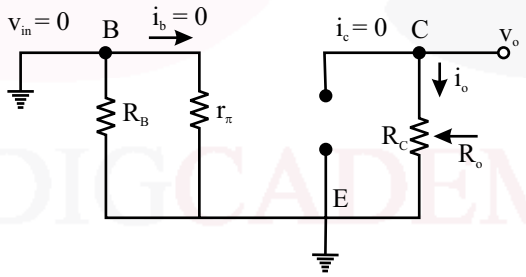


Fig. 39 AC equivalent circuit of base bias CE amplifier with p-model for output resistance

When input v_i is set to zero the base current becomes zero so if the collect current.

$\therefore$ $\boxed{R_o = R_C}$ (159)

Case-III : Analysis using π – model with output resistance r_o

In previous cases we have taken $i_c = \beta i_b$ but in this case we will consider g_m parameter of BJT. The AC equivalent circuit of amplifier with BJT replaced by π - model with output resistance becomes as shown in Fig. 40.

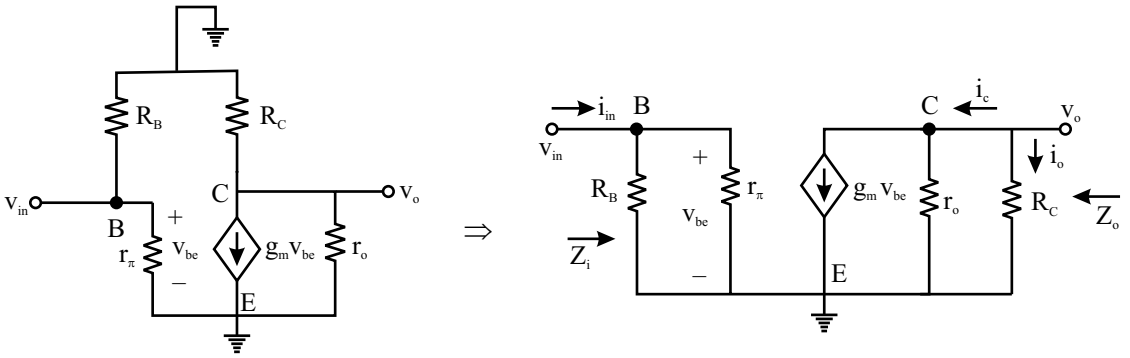


Fig. 40 AC equivalent circuit of base bias CE amplifier with output resistance of BJT & emitter bypass capacitor using p-model

Input Impedance :

Input impedance seen from input circuit,

$$\boxed{Z_{in} = R_B \,||\, r_\pi = \frac{R_B\, r_\pi}{R_B + r_\pi}} \tag{160}$$

Voltage Gain :

Output voltage of the circuit,

$$v_o = -\, g_m v_{be} \times \frac{r_o R_C}{r_o + R_C} \tag{161}$$

From input circuit, $v_{be} = v_{in}$

$$\therefore \quad v_o = -g_m \times \frac{r_o R_C}{r_o + R_C} \times v_{in}$$

Voltage gain,

$$\boxed{A_v = \frac{v_o}{v_{in}} = -\frac{g_m\, r_o R_C}{r_o + R_C}} \tag{162}$$

Current Gain :

Output current, $$i_o = -\frac{r_o}{r_o + R_C} \times g_m\, v_{be} \tag{163}$$

From input circuit, $$v_{be} = \left(r_\pi \,||\, R_B\right) i_{in} = \frac{r_\pi R_B}{r_\pi + R_B} \times i_{in} \tag{164}$$

$$\Rightarrow \quad i_o = -\frac{g_m\, r_o\, r_\pi R_B}{\left(r_\pi + R_B\right)\left(r_o + R_C\right)} \times i_{in} \tag{165}$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = -\frac{g_m r_o r_\pi R_B}{(r_\pi + R_B)(r_o + R_C)} \quad (166)$$

Output resistance :

Output resistance of the circuit is obtained by setting $v_{in} = 0$. When $v_{in} = 0$, the dependent current source $g_m v_{be}$ behaves as open circuit. The resistance seen from output terminals becomes,

$$Z_o = r_o \,||\, R_C = \frac{r_o R_C}{r_o + R_C} \quad (167)$$

4.10 Small Signal Analysis of Collector Feedback CE Amplifier

The collector feedback common emitter amplifier consists of a resistance connected between collector and base terminals. This amplifier provides a feedback from collector voltage to base current. The collector feedback amplifiers can be analyzed by considering emitter resistance and source resistance taken into account separately. The small signal analysis of collector feedback amplifier can be performed by using either of small signal model of BJT. Input and output signals are connected to BJT amplifier though input and output coupling capacitors as shown in Fig.41.

4.10.1 Small Signal Analysis of Collector Feedback CE Amplifier With Emitter Resistance

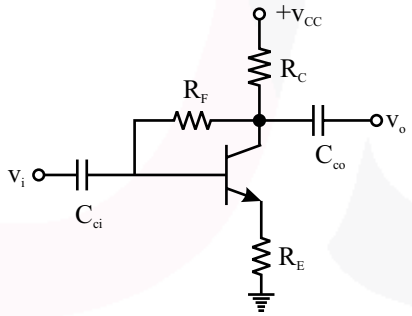


Fig. 41 Collector feedback self biased amplifier with emitter resistance

The AC equivalent circuit of the amplifier, by replacing coupling capacitors by short circuit, biasing source by ground and BJT by its approximate h-parameter model, becomes as shown in Fig. 42.

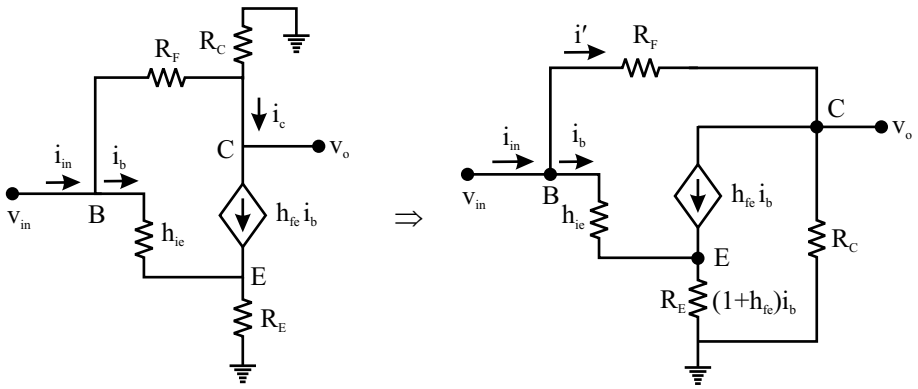


Fig. 42 AC equivalent circuit of collector feedback using approximate h-parameters

Applying KCL at node 'B', we have,

$$-i_{in} + i_b + \frac{v_{in} - v_o}{R_F} = 0 \quad (168)$$

$$-i_{in} R_F + i_b R_F + v_{in} - v_o = 0 \quad (169)$$

Applying KCL node 'C', we have,

$$\frac{v_o - v_{in}}{R_F} + \frac{v_o}{R_C} + h_{fe} i_b = 0 \quad (170)$$

From input circuit, $v_{in} = h_{ie} i_b + (1 + h_{fe}) R_E i_b$

$$\Rightarrow \quad i_b = \frac{v_{in}}{h_{ie} + (1 + h_{fe}) R_E} \quad (171)$$

Putting expression of i_b from above equation in equation (170), we have,

$$\frac{v_o - v_{in}}{R_F} + \frac{v_o}{R_C} + h_{fe} \times \frac{v_{in}}{h_{ie} + (1 + h_{fe}) R_E} = 0 \quad (172)$$

$$\Rightarrow \quad \left(\frac{1}{R_F} + \frac{1}{R_C}\right) v_o = \left[\frac{1}{R_F} - \frac{h_{fe}}{h_{ie} + (1 + h_{fe}) R_E}\right] v_{in}$$

$$\Rightarrow \quad v_o = \frac{R_C}{R_F + R_C}\left[\frac{h_{ie} + (1 + h_{fe}) R_E - h_{fe} R_F}{h_{ie} + (1 + h_{fe}) R_E}\right] v_{in}$$

Voltage gain, $A_v = \frac{v_o}{v_{in}} = \frac{R_C}{R_F + R_C}\left[\frac{h_{ie}(1 + h_{fe}) R_E - h_{fe} R_F}{h_{ie} + (1 + h_{fe}) R_E}\right] \quad (173)$

Let, $R_F >> R_E$, $R_F >> R_C$ and $(1 + h_{fe}) R_E >> h_{ie}$

Then, $R_C + R_F \approx R_F$

$h_{re} + (1 + h_{fe}) R_E \approx h_{fe} R_E$

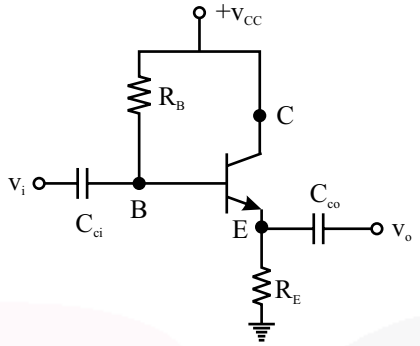
$h_{ie} + (1 + h_{fe}) R_E - h_{fe} R_F \approx -h_{fe} R_F$

$$\therefore \quad A_v = \frac{R_C}{R_F} \times \frac{-h_{fe} R_F}{h_{fe} R_E}$$

$$\Rightarrow \quad A_v = -\frac{R_C}{R_E} \quad (174)$$

4.11 Small Signal Analysis of Emitter Follower Amplifier

The output voltage of emitter follower amplifier is taken from emitter terminal of BJT. This amplifier has voltage gain close to unity and high current gain. The output signal is in phase with the input signal.



Case-I : Analysis using approximate h-parameter model

The AC equivalent circuit of the emitter follower amplifier is drawn by replacing coupling capacitors by short circuit and BJT by its approximate h-parameter model a shown in Fig. 44.

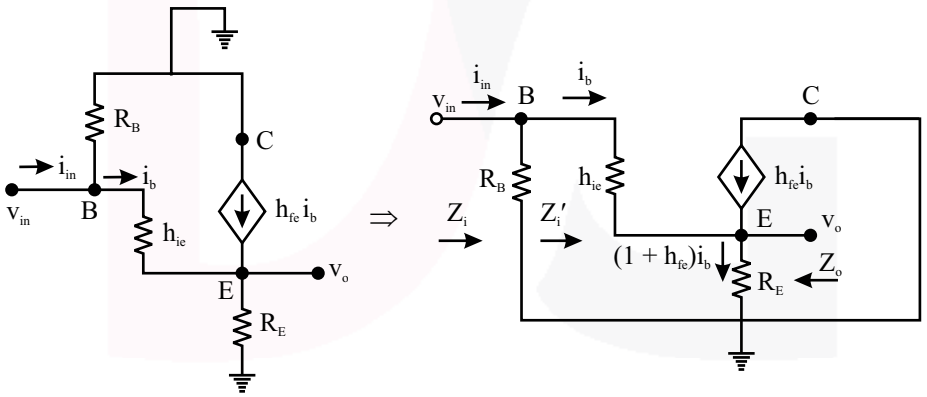


Fig. 44 AC equivalent circuit of emitter follower amplifier using approximate h-parameters

Input Impedance :

From input circuit, $v_{in} = h_{ie}\, i_b + (1 + h_{fe})\, i_b\, R_E$ (175)

$\Rightarrow$ $Z'_i = \dfrac{v_{in}}{i_b} = h_{ie} + \left(1 + h_{fe}\right) R_E$ (176)

Input impedance, $Z_i = R_B \parallel Z'_i = \dfrac{R_B\, Z'_i}{R_B + Z'_i}$ (177)

Voltage Gain :

Output voltage, $v_o = (1 + h_{fe})\, i_b\, R_E$ (178)

Putting expression of base current from equation (175) in above equation, we have,

$$v_o = \frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E} \times v_{in} \quad (179)$$

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = \frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E} \quad (180)$$

If R_E is selected such that $(1+ h_{fe}) R_E >> h_{ie}$

then $(1 + h_{fe}) R_E + h_{ie} \approx (1 + h_{fe}) R_E$

$$\Rightarrow A_v \approx \frac{(1+h_{fe})R_E}{(1+h_{fe})R_E} = 1 \quad (181)$$

Thus an emitter follower amplifier has voltage gain close to unity but less than unity.

Current Gain :

Output current, $$i_o = (1 + h_{fe})\, i_b \quad (182)$$

Base current, $$i_b = \frac{R_B}{R_B + Z_i'} \times i_{in} \quad (183)$$

$$\Rightarrow i_o = (1+h_{fe}) \times \frac{R_B}{R_B + Z_i'} \times i_{in} \quad (184)$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = \frac{(1+h_{fe})R_B}{R_B + Z_i'} \quad (185)$$

Putting expression of Z_i' from (176) in above equation, we have,

$$A_i = \frac{(1+h_{fe})R_E}{R_B + h_{ie} + (1+h_{fe})R_E} \quad (186)$$

Output Impedance :

Output impedance is obtained by setting $v_{in} = 0$ and finding resistance seen across output terminals of the amplifier. The equivalent circuit with input voltage set to zero becomes as shown below,

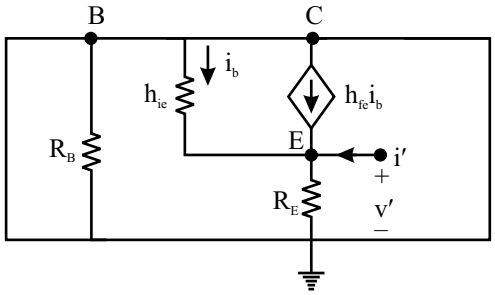


Fig. 45 Equivalent circuit of emitter follower amplifier input source shorted

The resistance R_B is bypassed by short circuit. The circuit can be redrawn as under,

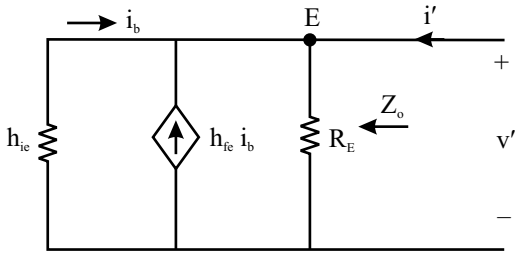


Fig. 46 Equivalent circuit of emitter follower amplifier redrawn for output resistance

From above circuit, $$i_b = -\frac{v'}{h_{ie}} \tag{187}$$

KCL at node 'E' , gives,

$$\frac{v'}{R_E} - h_{fe}\, i_b - i_b - i' = 0 \tag{188}$$

Putting the expression of i_b in above equation from equation (187), we have,

$$\Rightarrow \quad \frac{v'}{R_E} + h_{fe} \cdot \frac{v'}{h_{ie}} + \frac{v'}{h_{ie}} - i' = 0$$

$$\Rightarrow \quad v'\left[\frac{1}{R_E} + \frac{h_{fe}}{h_{ie}} + \frac{1}{h_{ie}}\right] = i'$$

$$\Rightarrow \quad \boxed{R_o = \frac{v'}{i'} = \frac{1}{\frac{1}{R_E} + \frac{h_{fe}}{h_{ie}} + \frac{1}{h_{ie}}}} \tag{189}$$

Case-II : Analysis using π -model

The AC equivalent circuit of the amplifier is drawn by short circuiting the coupling capacitors and by replacing DC biasing source by ground and BJT by π-model as shown in Fig.47.

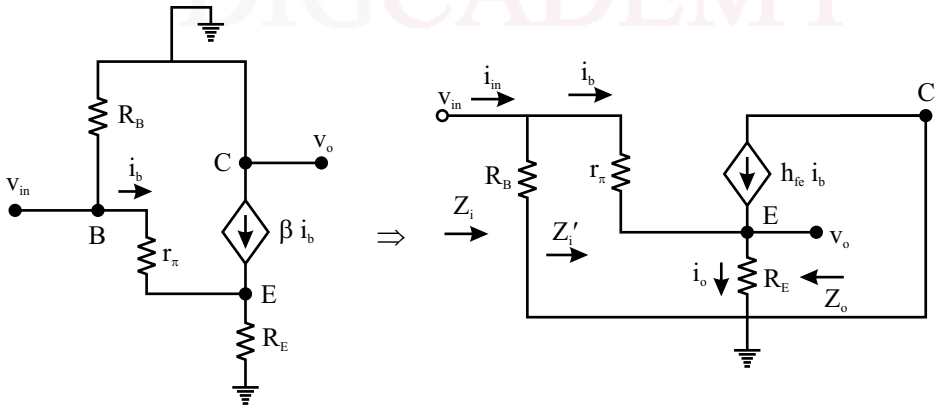


Fig. 47 AC equivalent circuit of emitter follower amplifier using approximate h-parameters

Input Impedance :

From input circuit, $v_{in} = r_\pi i_b + (1+\beta) i_b R_E$ (190)

$$Z'_i = \frac{v_{in}}{i_b} = r_\pi + (1+\beta) R_E \quad (191)$$

Input Impedance, $Z_i = R_B \| Z'_i = \frac{R_B Z'_i}{R_B + Z'_i}$ (192)

Voltage gain :

Output voltage of the circuit,

$$v_o = (1+\beta) i_b R_E \quad (193)$$

Putting expression of base current from equation (190) in above equation, we have,

$$v_o = \frac{(1+\beta) R_E}{r_\pi + (1+\beta) R_E} v_{in} \quad (194)$$

Voltage gain, $A_v = \frac{v_o}{v_{in}} = \frac{(1+\beta) R_E}{r_\pi + (1+\beta) R_E}$ (195)

Current gain :

Output current, $i_o = (1+\beta) i_b$ (196)

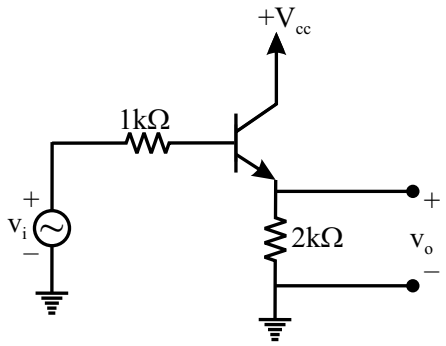
Base current, $i_b = \frac{R_B}{R_B + Z'_i} \times i_{in}$ (197)

$\Rightarrow$ $i_o = (1+\beta) \times \frac{R_B}{R_B + Z'_i} i_{in}$ (198)

Current gain, $A_i = \frac{i_o}{i_{in}} = \frac{(1+\beta) R_B}{R_B + Z'_i}$ (199)

Example 9

An amplifier circuit is shown below. Assume that the transistor works in active region. The low frequency small - signal parameters for the transistor are $g_m = 20$ mS, $\beta_0 = 50$, $r_0 = \infty$, $r_b = 0$. What is the voltage gain, $A_v = (v_o / v_i)$, of the amplifier?

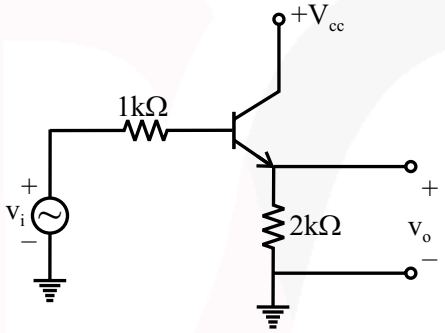


(a) 0.967 (b) 0.967

(c) 0.983 (d) 0.998

GATE(IN/2006/2M)

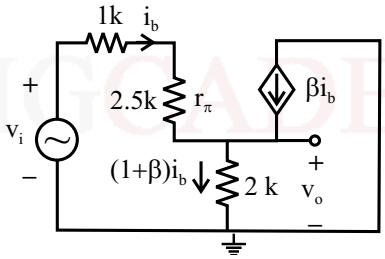
Solution : Ans.(b)



Parameter r_π of BJT,

$$r_\pi = \frac{\beta}{g_m} = \frac{50}{20\times10^{-3}} = 2.5\ \text{k}$$

Replacing BJT by its π-model the ac equivalent of amplifier becomes,



Applying KVL in base circuit,

$$v_i = 3.5\ i_b + (1+\beta)i_b \times 2$$

$$\Rightarrow \quad i_b = \frac{v_i}{3.5+51\times2} = \frac{1}{105.5}v_i$$

From output side, $v_o = (1+\beta)\ i_b \times 2$

$$\Rightarrow \qquad v_o = 51 \times 2 \times \frac{1}{105.5} \times v_i$$

Voltage gain, $$A_v = \frac{102}{105.5} = 0.967$$

4.12 Small Signal Analysis of Common Base Amplifier Using π-Model

Consider a common base amplifier as shown in the Fig. 48. The input and output signals are coupled to the amplifier through input and output coupling capacitors, respectively.

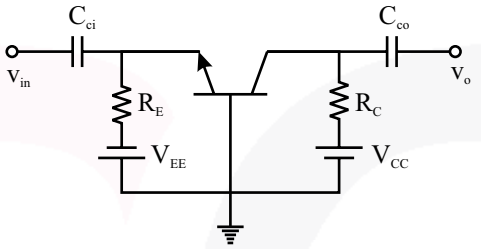


Fig. 48 Common base amplifier

The small signal analysis of the common base amplifier will be carried out with re- model of BJT. For small signal analysis the coupling capacitors are replaced by short circuit, DC biasing voltage sources are replaced by short circuit and BJT is replaced by its r_e-model. The AC equivalent circuit of the amplifier becomes as shown Fig.49.

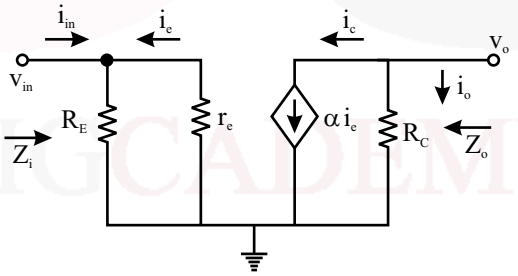


Fig. 49 Small signal equivalent circuit of common base amplifier

I. Input Impedance :

$$Z_i = R_E \| r_e = \frac{R_E r_e}{R_E + r_e} \qquad (200)$$

II. Voltage Gain :

Emitter current, $$i_e = \frac{-v_{in}}{r_e} \qquad (201)$$

Output voltage, $$v_o = \alpha i_e \times R_C = -\alpha R_C \left[-\frac{v_{in}}{r_e}\right] \quad (202)$$

III. Current gain :

Output current, $$i_o = -i_c = -\alpha i_e \quad (203)$$

From input circuit,

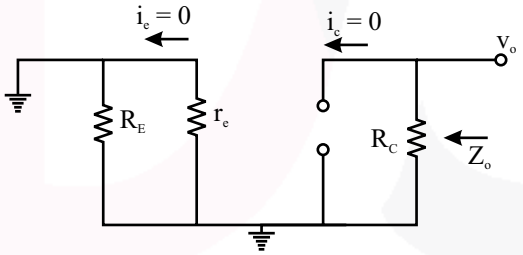
$$i_e = -\frac{R_E}{R_E + r_e} \times i_{in} \quad (204)$$

$$\therefore \quad i_o = \frac{\alpha R_E}{R_E + r_e} \times i_{in} \quad (205)$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = \frac{\alpha R_E}{R_E + r_e} \quad (206)$$

IV. Output Impedance :

Output impedance of the amplifier is obtained by setting $v_{in} = 0$ and finding impedance across output terminals of the amplifier. When input $v_{in} = 0$, the AC equivalent circuit becomes as shown in Fig. 50.



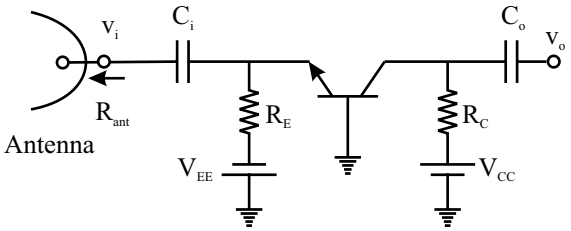
Output impedance, $$Z_o = R_C \quad (207)$$

Example 10

A BJT in a common-base configuration is used to amplify a signal received by a 50 Ω antenna. Assume kT/q = 25 mV. The value of the collector bias current (in mA) required to match to match the input impedance of the amplifier to the impedance of the antenna is_____

GATE(EC-IV/2014/2M)

Solutin : Ans (0.49 to 0.51)



Given, $R_{out} = 50\Omega$, $V_T = \frac{kT}{q} = 25mV$

Output conductance of BJT,

$$g_m = \frac{I_C}{V_T}$$

Output resistance of amplifier,

$$R_o = \frac{1}{g_m} = \frac{V_T}{I_C} = \frac{25\times10^{-3}}{I_C}$$

For impedance matching output resistance of amplifier should be equal to input impedance of antenna.

$$\therefore \quad R_{ant} = R_o$$

$$\Rightarrow \quad 50 = \frac{25\times10^{-3}}{I_C}$$

$$\Rightarrow \quad I_C = \frac{25\times10^{-3}}{50} = 0.5mA$$

4.13 Effect of Source Resistance and Load Resistance

The effect of source and load resistance on performance of an amplifier can be studied on any of the configurations discussed in previous sections. However, CE amplifier with potential divider bias being a most preferred configuration has been used here for discussion.

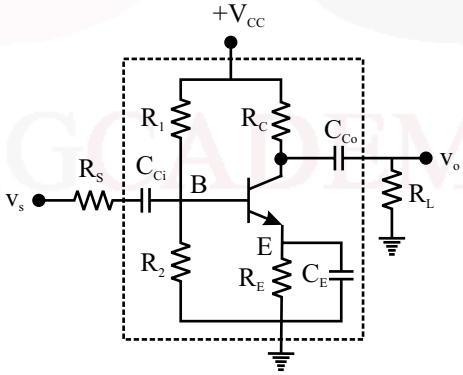


Fig. 51 Potential divider bias CE amplifier with source and load resistances

When load resistance R_L and source resistance, R_s, are also taken into, the small signal AC equivalent circuit can be drawn using any of small signal model of BJT. The AC equivalent model of CE amplifier using hybrid π-model of BJT can be drawn as shown in Fig. 52.

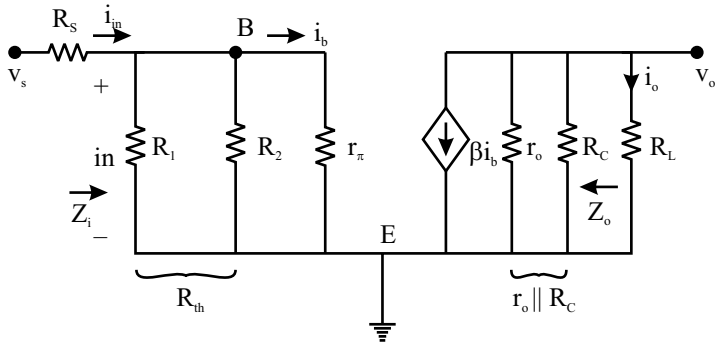


Fig. 52 AC equivalent circuit of potential divider bias CE amplifier with source and load resistances

Input impedance :

The input impedance of the amplifier,

$$Z_i = R_1 \| R_2 \| r_\pi = R_{th} \| r_\pi = \frac{R_{th}\, r_\pi}{R_{th} + r_\pi} \tag{208}$$

Where $$R_{th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{209}$$

Voltage Gain :

Output voltage, $$v_o = R_L\, i_o \tag{210}$$

Applying current divide rule,

$$i_o = -\frac{(r_o \| R_c)}{(r_o \| R_c) + R_L} \times \beta i_b \tag{211}$$

$$\Rightarrow \quad v_o = -\frac{(r_o \| R_c) R_L}{(r_o \| R_c) + R_L} \times \beta i_b \tag{212}$$

From input circuit,

$$i_b = \frac{R_{th}}{R_{th} + r_\pi} \times i_{in} \tag{213}$$

$$\Rightarrow \quad v_o = -\frac{(r_o \| R_c) \times \beta R_L}{(r_o \| R_c) + R_L} \times \frac{R_{th}}{R_{th} + r_\pi} \times i_{in} \tag{214}$$

Input current of BJT, $$r_{in} = \frac{v_s}{R_s + Z_i} \tag{215}$$

$$\therefore \quad v_o = -\frac{(r_o \| R_C) \beta R_L}{(r_o \| R_C) + R_L} \times \frac{R_{th}}{R_{th} + r_\pi} \times \frac{1}{R_s + Z_i} \times v_s \tag{216}$$

Voltage gain, $$A_v = \frac{v_o}{v_s} = -\frac{(r_o \| R_C)\beta R_L}{(r_o \| R_C) + R_L} \times \frac{R_{th}}{R_{th} + r_\pi} \times \frac{1}{R_s + Z_i} \quad (217)$$

Current gain :

From equation (211) & (213), we have,

$$i_o = -\frac{(r_o \| R_C)}{(r_o \| R_C) + R_L} \times \beta \times \frac{R_{th}}{R_{th} + r_\pi} \times i_{in} \quad (218)$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = -\frac{(r_o \| R_C) \times \beta R_{th}}{\left[(r_o \| R_C) + R_L\right](R_{th} + r_\pi)} \quad (219)$$

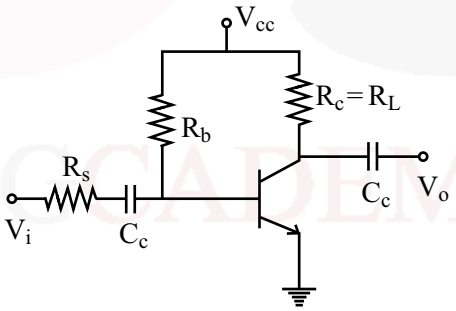
Output Impedance :

Output impedance of the amplifier impedance seen across output terminals is obtained by replacing input voltage source by short circuit and load resistance by open circuit. When $v_s = 0$, then input current i_{in} becomes zero and hence the base current. The dependent current source, βi_b behaves as open circuit. Then resistance seen across the output terminal of the amplifier becomes,

$$Z_o = r_o \| R_C = \frac{r_o R_C}{r_o + R_C} \quad (220)$$

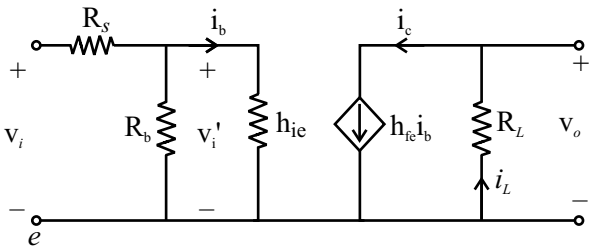
Example 11

Find the voltage gain of common emitter amplifier, shown in the figure below, in terms of h-parameter of BJT.



Solution :

Drawing the ac equivalent circuit of the amplifier with approximate h-parameter we get:



$$v_o = -R_L\, i_c = -R_L\, h_{fe}\, i_b$$

$$i_b = \frac{v_i'}{h_{ie}}$$

$$\Rightarrow \qquad v_o = -\frac{R_L\, h_{fe}}{h_{ie}} . v_i' \qquad \text{...(i)}$$

$$v_i' = \frac{R_b \,||\, h_{ie}}{R_s + R_b \,||\, h_{ie}} . v_i = \frac{R_b\, h_{ie}}{(R_b + h_{ie})R_s + R_b\, h_{ie}} . v_i$$

Putting above expression of v_i' in equation (i), we have,

Voltage gain, $$A_v = \frac{v_o}{v_i} = -\frac{R_L\, h_{fe}}{h_{ie}} \times \frac{R_b\, h_{ie}}{(R_b + h_{ie})R_s + R_b\, h_{ie}}$$

4.14. Phasor Relations of Input and Output Signals of BJT Amplifiers

I. CE configuration

It can be observed that voltage gain and current gain are negative for potential divider bias, base bias and collector feedback bias circuits of common emitter (CE) configuration of BJT amplifier. The negative sign indicates that output signal is 180° out of phase in comparison with input signal. Therefore, CE configuration of BJT acts like an inverter. The waveforms of input and output signals of CE configuration are as shown in Fig. 53.

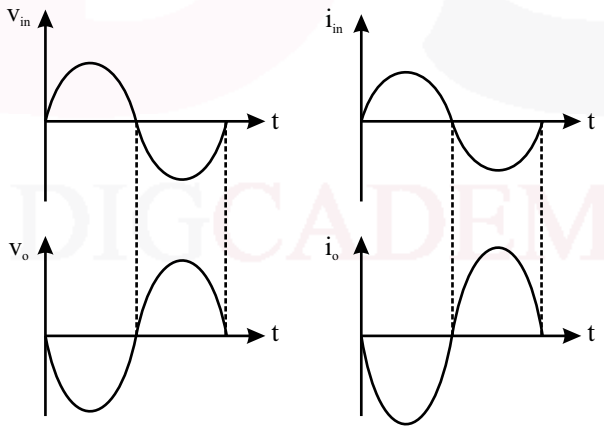


Fig. 53 Input and output signals of CE amplifier

II. Common Collector Configuration

The voltage gain and current gain of common collector or emitter follower configuration of BJT amplifier are positive which means output signals are in phase with input signals. The waveforms of input and output signals of emitter follower can be drawn as shown in Fig.54

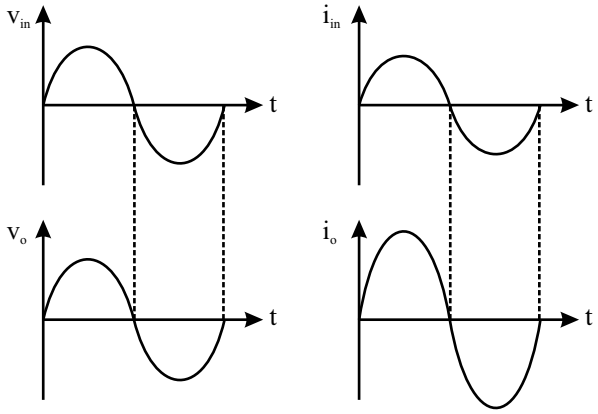


Fig. 54 Input and output signals of emitter follower

III. Common Base Configuration

The voltage gain and current gain of common base configuration of BJT are positive which means input and output signals are in phase with each other. The wave forms of input and output signals of common base amplifier can be drawn as shown in Fig. 55

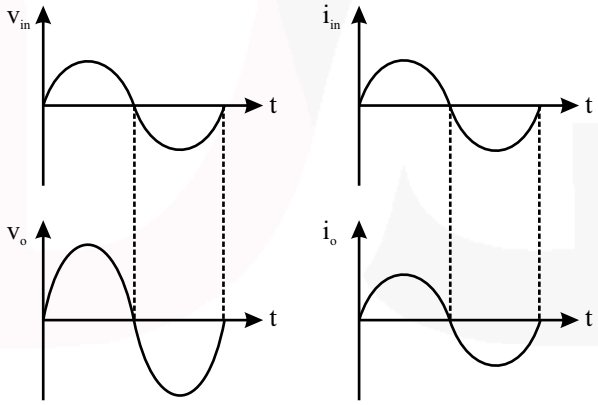


Fig. 54 Input and output signals of common base amplifier

4.15. Effects Emitter Resistance and Emitter By Pass Capacitor

I. Effects of Emitter Resistance (R_{II})

i. Provides negative feedback
ii. Stabilizes the biasing point of BJT and helps in self biasing of BJT
iii. Increases input impedance of amplifier
iv. Reduces voltage and current gain of the amplifier
v. Increases bandwidth of the amplifier
vi. Reduces the non-linear distortion
vii. Reduces the effect of external noise

III. Effects of Emitter By Pass Capacitor

The emitter bypass capacitor behaves as open circuit for DC biasing signals and acts like a short circuit for AC signals. The effects of emitter bypass capacitor are just opposite to the effects of emitter resistance, which are as under,

i. It provides path for AC component of emitter current of amplifier
ii. Reduces the input impedance of amplifier
iii. Increases the voltage and current gain
iv. Reduces the bandwidth of the amplifier
v. Increases lower cutoff frequency of the amplifier

4.16 Comparison of Parameters of CE, CC and CB amplifier

The comparison of voltage gain, current gain input impedance and output impedance of different configuration of BJT amplifier are summarized in Table 2.

Table 2 : Comparison of parameters of CE, CC and CB amplifiers

S.N.	Parameter	CE Amplifier	CC Amplifier	CB Amplifier
1.	Voltage Gain	High	less than 1 but close to unity	High
2.	Current Gain	High	High	less than 1 but close to unity
3.	Input impedance	High	High	Low
4.	Output impedance	High	Low	High

4.17 Power gain, Voltage Gain and Current Gain of the amplifiers in dB

I. Power gain of the amplifier

The power gain of an amplifier is defined as ratio of output power to the input power of the amplifier. However, an amplifier does not generate the power rather it changes the AC input power and DC power from biasing source to the AC power at the output of the amplifier.

The AC input power of an amplifier is given by,

$$P_o = v_o i_o$$

The AC input power of an amplifier is given by,

$$P_{in} = v_{in} i_{in}$$

The power gain of an amplifier is the ratio of output power to the input power of the amplifier.

$$\therefore \quad A_P = \frac{P_o}{P_{in}} = \frac{v_o i_o}{v_{in} i_{in}} = A_v \cdot A_i$$

$$\Rightarrow \quad \boxed{A_P = A_v \,.\, A_i}$$

Due to wide range of frequencies input signals of an amplifier the power gain, voltage gain and current gain of an amplifier are measured in decibel (dB).

The voltage gain in dB is given by,

$$A_{vdB} = 20 \log_{10} \frac{V_o}{V_{in}}$$

The current gain in dB is given by,

$$A_{idB} = 20 \log_{10} \frac{I_o}{I_{in}}$$

Power gain in dB is given by,

$$A_{P\,dB} = 10 \log_{10} \frac{P_o}{P_{in}}$$

Example 12

A common emitter amplifier has a voltage gain of 50 andinput impedance is 1000 Ω find out the power gain of the amplifier if the output impedance is 200 Ω.

Solution :

Given, $A_v = 50$

Voltage gain in terms of current is given by,

$$A_v = \frac{Z_L}{Z_i} \,.\, A_i$$

$$\Rightarrow \quad A_i = \frac{Z_i}{Z_L} A_v = \frac{1000}{200} \times 50 = 250$$

Power gain $A_P = A_v \,.\, A_i = 50 \times 250 = 12500$

In dB, $A_P = 10 \log_{10} 12500 \text{ dB} = 40{\cdot}969 \text{ dB}$

Example 13

An amplifier has an input power of 2 microwatts. The power gain of the amplifier is 60 dB. The output power will be

(a) 6 microwatts (b) 120 microwatts

(c) 2 milliwatts (d) 2 watts

IES(E&T,91)

Solution : Ans.(d)

Power gain (in dB) of amplifier is given by

$$A_p = 10 \log_{10} \frac{P_{out}}{P_{in}}$$

Given, $A_p = 60$ dB,

$P_{in} = 2\ \mu W$

$\Rightarrow \quad 60 = 10\log_{10}\dfrac{P_{out}}{2\times10^{-6}}$

$\Rightarrow \quad P_{out} = 10^6 \times 2 \times 10^{-6}$

$P_{out} = 2W$

❐❐❐

GATE QUESTIONS

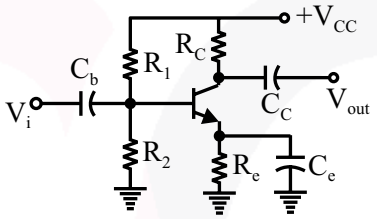
Q.1 The current gain of a BJT is

(a) $g_m r_o$ (b) $\frac{g_m}{r_o}$

(c) $g_m r_\pi$ (d) $\frac{g_m}{r_\pi}$

GATE(EC/2001/1M)

Q.2 In the transistor amplifier shown in figure the ratio of small signal voltage gain, when the emitter resistor R_e is bypassed by the capacitor C_e to when it is not bypassed, (assuming simplified approximate h-parameter model for transistor, is

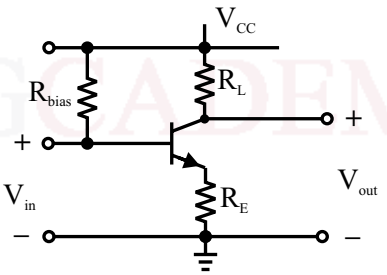


(a) 1 (b) h_{fe}

(c) $\frac{(1+h_{f_e})R_e}{h_{ie}}$ (d) $1+\frac{(1+h_{f_e})R_e}{h_{ie}}$

GATE(EE/1996/1 M)

Q.3 In the BJT amplifier shown in figure, the transistor is biased in the forward active region. Putting a capacitor across R_E will



(a) Decrease the voltage gain and decrease the input impedance

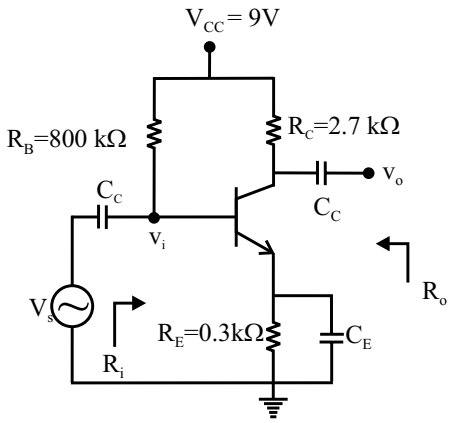
(b) Increase the voltage gain and decrease the input impedance

(c) Decrease the voltage gain and increase the input impedance

(d) Increase the voltage gain and increase the input impedance

GATE(EC/1997/2M)

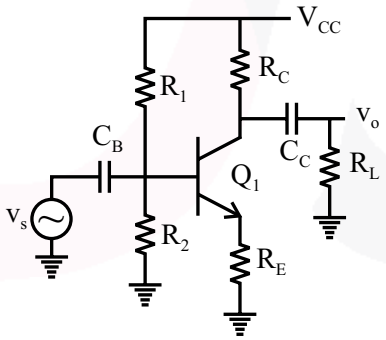
Q.4 The amplifier circuit shown below uses a silicon transistor. The capacitors C_C and C_E can be assumed to be short at signal frequency and the effect of output resistance r_o can be ignored. If C_E is disconnected from the circuit, which one of the following statements is TRUE?



(a) The input resistance R_i increases and the magnitude of voltage gain A_V decreases
(b) The input resistance R_i decreases and the magnitude of voltage gain A_V increases
(c) Both input resistance R_i and the magnitude of voltage gain A_V decrease
(d) Both input resistance R_i and the magnitude of voltage gain A_V increase

GATE(EC/2010/2M)

Q.5 The amplifier shown below has a voltage gain of –2.5, and input resistance of 10 kΩ and a lower 3-dB cut-off frequency of 20Hz. Which one of the following statements is **TRUE** when the emitter resistance R_E is doubled?



(a) Magnitude of voltage gain will decrease
(b) Input resistance will decrease
(c) Collector bias current will increase
(d) Lower 3-dB cut-off frequency will increase

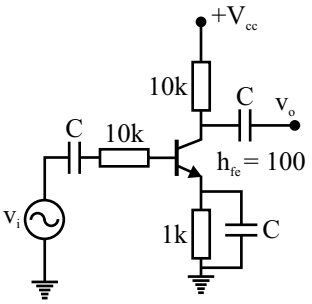
GATE(IN/2011/1M)

Q.6 If the emitter resistance in a common-emitter voltage amplifier is not by passed, it will

(a) reduce both the voltage gain and the input impedance
(b) reduce the voltage gain and increase the input impedance
(c) increase the voltage gain and reduce the input impedance
(d) increase both the voltage gain and the input impedance

GATE(EC-IV/2014/1M)

Q.7 The magnitude of the mid-band voltage gain of the circuit shown in figure is (assuming h_{fe} of the transistor to be 100)

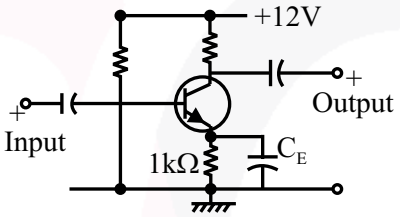


(a) 1 (b) 10

(c) 20 (d) 100

GATE(EE-I/2014/1M)

Q.8 In the single-state transistor amplifier circuit shown in figure the capacitor C_E is removed. Then, the ac small-signal midband voltage gain of the amplifier



(a) Increases (b) Decreases

(c) Is unaffected (d) Drops to zero

GATE(EE/2001/1 M)

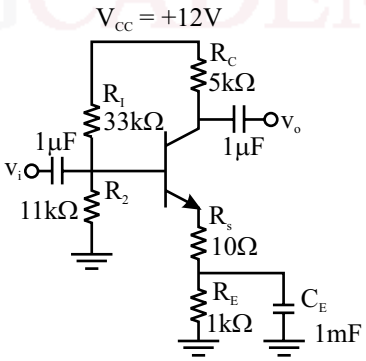
Q.9 A common emitter transistor amplifier, using a collector load of 1 k ohm and operating at room temperature, with a collector current of 1 mA, gives a voltage gain nearly equal to

(a) 25 (b) 40

(c) 250 (d) 1000

GATE(IN/1997/1M)

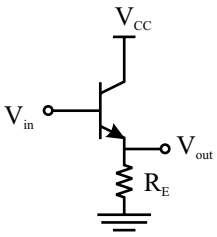
Q.10 For the amplifier shown in the figure, the BJT parameters are V_{BE} = 0.7 V, β = 200, and thermal voltage V_r = 25 mV. The voltage gain (v_o/v_i) of the amplifier is_____.



GATE(EC-I/2014/2M)

Q.11 Consider the common-collector amplifier in the figure (bais circuitry ensures that the transistor operates in forward active region, but has been omitted for simplicity). Let I_C be the collector current,

V_{BE} be the base-emitter voltage and V_T be the thermal voltage. Also, g_m and r_o are the small-signal transconductance and output resistance of the transistor, respectively. Which one of the following conditions ensures a nearly constant small signal voltage gain for a wide range of values of R_E ?

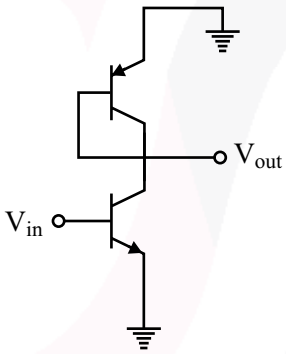


(a) $g_m R_E << 1$ (b) $I_C R_E >> V_T$

(c) $g_m r_o >> 1$ (d) $V_{BE} >> V_T$

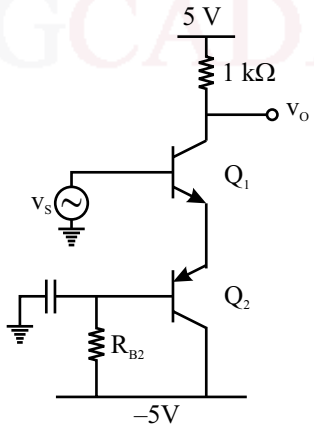
GATE(EC-IV/2014/2M)

Q.12 In the ac equivalent circuit shown, the two BJTs are biased in active region and have identical parameters with $\beta >> 1$. The open circuit small signal voltage gain is approximately .....



GATE(EC-II/2015/2M)

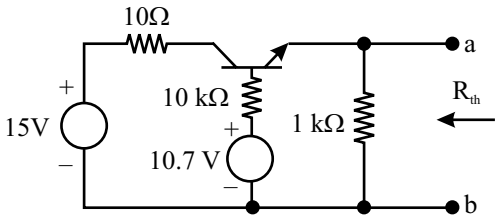
Q.13 In the circuit shown, transistors Q_1 and Q_2 are biased at a collector current of 2.6mA. Assuming that transistor current gains are sufficiently large to assume collector current equal to emitter current and thermal voltage of 26 mV, the magnitude of voltage gain V_0/V_s in the mid-band frequency range is _____ (up to second decimal place).



GATE(EC-II/2017/2M)

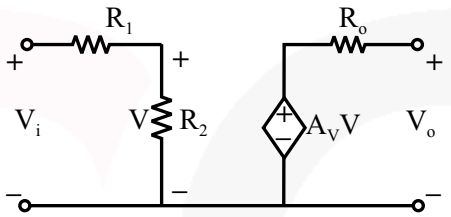
Q.14 In the circuit shown in the figure, the bipolar junction transistor (BJT) has a current gain

$\beta = 100$. The base-emitter voltage drop is a constant, $V_{BE} = 0.7V$. The value of the Thevenin equivalent resistance R_{th} (in Ω) as shown in the figure is _____ (up to 2 decimal places).



GATE(EE/2018/2M)

Q.15 The DC voltage gain $\frac{V_0}{V_i}$ in the following circuit is given by



(a) $A_v \frac{R_2}{R_1+R_2}$

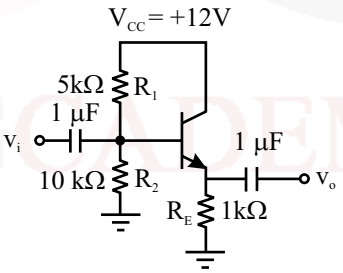
(b) $A_v \frac{R_1}{R_1+R_2}$

(c) $A_v \frac{R_2}{R_1+R_2} + R_0$

(d) V_v

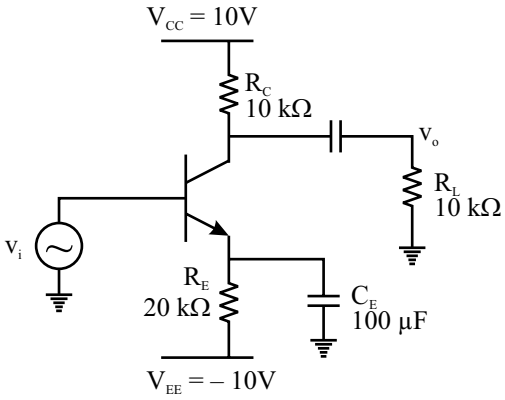
GATE(IN/2007/1M)

Q.16 For the common collector amplifier shown in the figure, the figure, the BJT has high β, negligible $V_{CE(sat)}$, and $V_{BE} = 0.7$ V. The maximum undistorted peak-to peak output voltage v_o (in Volts) is_____



GATE(EC-IV/2014/2M)

Q.17 For the BJT in the amplifier shown below. V_{BE} = 0.7 V, kT/q = 26 mV. Assume the BJT output resistance (r_o) is very high and the base current is negligible. The capacitors are also assumed to be short circuited at signal frequencies. The input v_i is direct coupled. The low frequency gain v_o / v_i of the amplifier is



(a) –89.42
(b) –128.21
(c) –178.85
(d) –256.42

GATE(EC/2020/2M)

❐❐❐

ANSWERS & EXPLANATIONS

Q.1 ***Ans.(c)***

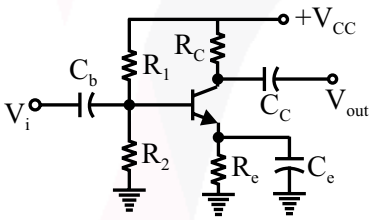
Base resistance r_π of BJT is given by

$$r_\pi = \frac{h_{fe}}{g_m} = \frac{\beta}{g_m}$$

where, $g_m \rightarrow$ transconductance and β is current gain

So, current gain, $\beta = g_m r_\pi$

Q.2 ***Ans.(d)***



Gain of above amplifier with C_e in circuit,

$$A_{v_1} = -\frac{h_{fe} R_L}{h_{ie}}$$

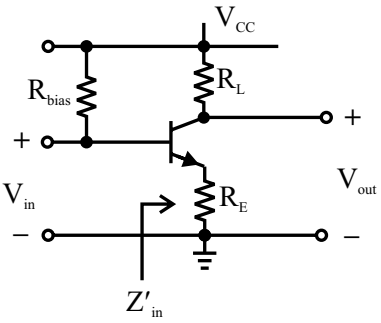
Gain of amplifier when C_e is removed,

$$A_{v_2} = -\frac{h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_e}$$

Ratio of gains, $$\frac{A_{v_1}}{A_{v_2}} = \frac{h_{ie} + (1 + h_{fe}) R_e}{h_{ie}}$$

$\Rightarrow$ $$\frac{A_{v_1}}{A_{v_2}} = 1 + \frac{1 + h_{fe}}{h_{ie}} \cdot R_e$$

Q.3 ***Ans.(b)***



The voltage gain of amplifier shown with R_E is given by,

$$A_V = -\frac{h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_e}$$

The input impedance with negative feed back is given by,

$$Z'_{in} = h_{ie} + (1+h_{fe})R_e$$

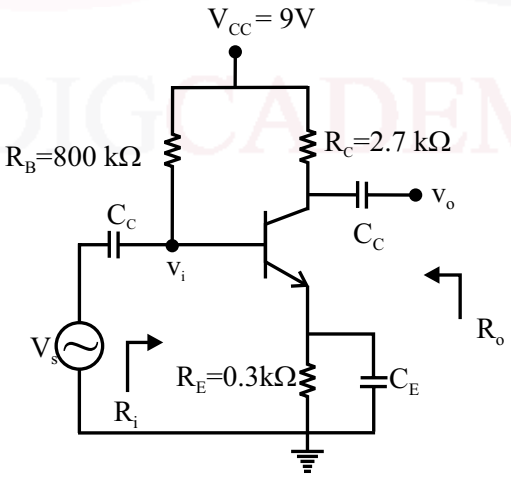
So, if R_E is bypassed by putting a capacitor across it the voltage gain will increase and input impedance will decrease.

Note :-

Effects of emitter resistance, R_E ,

i. Provides negative feedback in base circuit.
ii. Improves bias stability
iii. The voltage gain of amplifier reduces.
iv. The input impedance of amplifier increases.

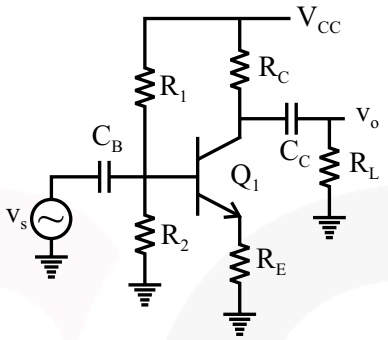
Q.4 Ans.(a)



Capacitor C_E in above circuit behaves like a short circuit for ac signals. When C_E is removed emitter resistance R_E provides current series negative feedback in the input loop. Various effects of negative feedback provided by R_E are listed below,

i. Voltage gain of amplifier is reduced
ii. Input impedance is increased.
iii. Bandwidth of amplifier is increased. So, lower cutoff frequency is reduced and upper cutoff frequency is increased.
iv. Effect of noise is reduced.

Q.5 Ans.(a)



In the above circuit resistance R_E provides current series negative feedback in the input loop. Various effects of negative feedback provided by R_E are listed below,

i. Voltage gain of amplifier is reduced
ii. Input impedance is increased.
iii. Bandwidth of amplifier is increased. So, lower cutoff frequency is reduced and upper cutoff frequency is increased.
iv. Effect of noise is reduced.
v. Non-linear distortion is reduced.

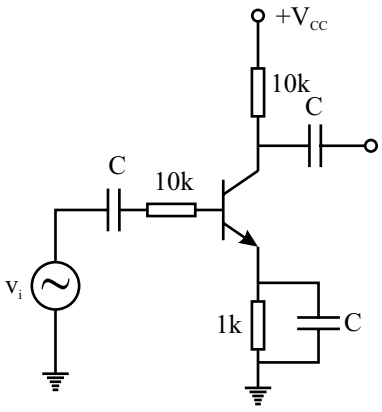
When R_E is doubled feedback voltage is increased and voltage gain is reduced, input resistance is increased, lower cutoff frequency is reduced and collector bias current is reduced.

Q.6 Ans (b)

Various effects of negative feedback provided by R_E are listed below,

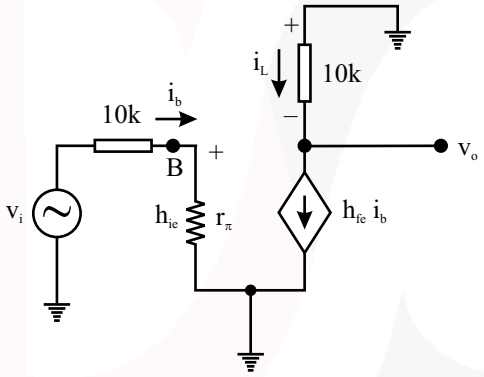
i. Voltage gain of amplifier is reduced
ii. Input impedance is increased.
iii. Bandwidth of amplifier is increased. So, lower cutoff frequency is reduced and upper cutoff frequency is increased.
iv. Effect of noise is reduced.
v. Non-linear distortion is reduced.

Q.7 Ans. (d)



Given $h_{fe} = 100$

Replacing BJT by approximate h-parameter model, coupling and bypass capacitors by short circuit and biasing voltage by groud, the AC equivalent circuit of the amplifier becomes as under,



Output voltage, $v_o = -10k \times h_{fe}\, i_b$

Base current, $i_b = \dfrac{v_i}{10k + h_{ie}}$

$\Rightarrow$ $v_o = -\dfrac{10k \times h_{fe}}{10k + h_{ie}} \cdot v_i$

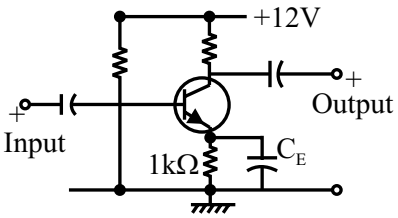
Mid band voltage gain,

$\Rightarrow$ $|A_v| = \left|\dfrac{v_o}{v_i}\right| = \dfrac{10k \times h_{fe}}{10k + h_{ie}}$

Let , $h_{ie} << 10k$

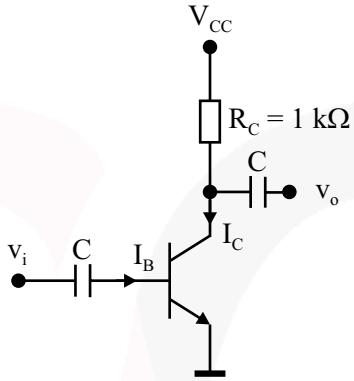
$\Rightarrow$ $|A_v| \approx \dfrac{10k}{10k} \cdot h_{fe} \approx h_{fe} = 100$

Q.8 Ans.(b)



When C_E is removed the emitter resistance produces negative feedback and results in reduction in gain of amplifier.

Q.9 Ans.(c)



Given, $I_C = 1$ mA, $R_C = 1$ kΩ

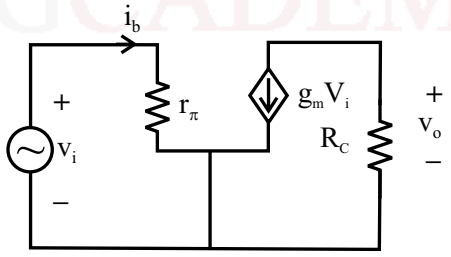
The transconductance of BJT,

$$g_m = \frac{I_C}{V_T} \text{ ; where } V_T \text{ is thermal voltage.}$$

At room temperature, $V_T = 25$ mV

$$\Rightarrow \quad g_m = \frac{1}{25}$$

The ac equivalent of common emiter BJT amplifier can be drawn as under,



Output voltage of amplifier,

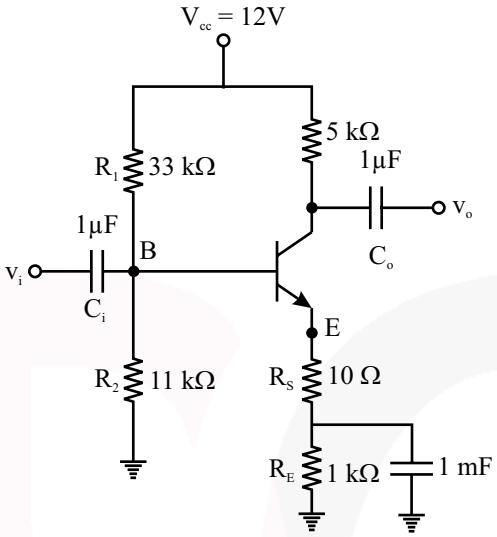
$$V_o = -g_m R_C V_i$$

Voltage gain of the amplifier,

$$\Rightarrow \quad \frac{V_o}{V_i} = -g_m R_C = -\frac{1}{25} \times 1000 = -250$$

$$\Rightarrow \quad \left|\frac{V_o}{V_i}\right| = 250$$

Q.10 Ans.:–240 to –230

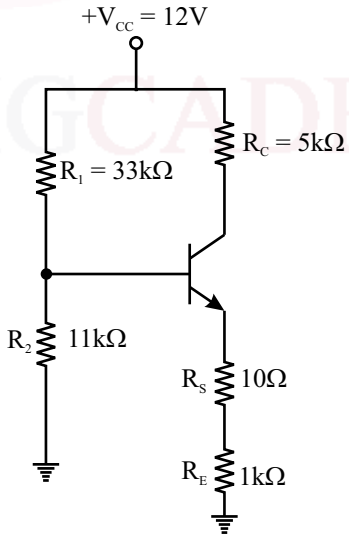


Given, $V_{BE} = 0.7V$ $\beta = 200$ and $V_T = 25$ mV

Here, the parameters for small signal parameters used for finding the gain of amplifier are not given. These parameters are determined by using the DC analysis and gain is obtained by using the AC analysis as follows,

Case-I : DC analysis

The emitter bypass capacitor and coupling capacitors are replaced by open circuit for DC analysis of an amplifier. Then the biasing circuit of the amplifier can be drawn as under,



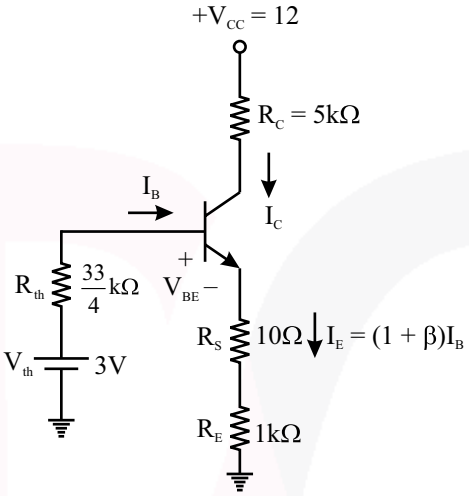
Replacing polential divider circuit by its Thevenin's equivalent circuit, we have,

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{cc} = \frac{11}{33+11} \times 12$$

$$\Rightarrow \quad V_{th} = 3V$$

and $$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{33 \times 11}{33+11} = \frac{33}{4} k\Omega$$

The biasing circuit can be redrawn as under



Applying KVL in base circuit, we have,

$V_{th} - I_B R_{th} - V_{BE} - (1 + \beta) I_B (R_C + R_E) = 0$

$$\Rightarrow \quad I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1+\beta)(R_E + R_S)}$$

$$\Rightarrow \quad I_B = \frac{3 - 0.7}{\frac{33 \times 10^3}{4} + (1+200)\left(10 + 1 \times 10^3\right)}$$

$$\Rightarrow \quad I_B = 10.88\ \mu A = 10.88 \times 10^{-6}\ A$$

Collector current, $I_C = \beta I_B = 200 \times 10.88 \times 10^{-6} A = 2.18\ mA$

Transconductance of BJT, $g_m = \frac{I_C}{V_T} = \frac{2.18 \times 10^{-3}}{25 \times 10^{-3}} = 0.087$

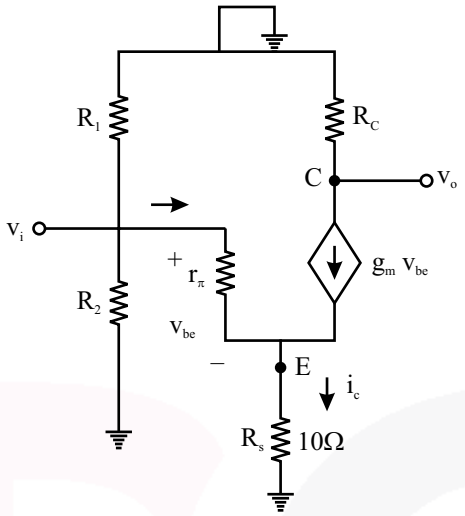
Input or Base resistance of BJT,

$$r_\pi = \frac{V_T}{I_B} = \frac{25 \times 10^{-3}}{10.88 \times 10^{-6}} = 2.314\ k\Omega$$

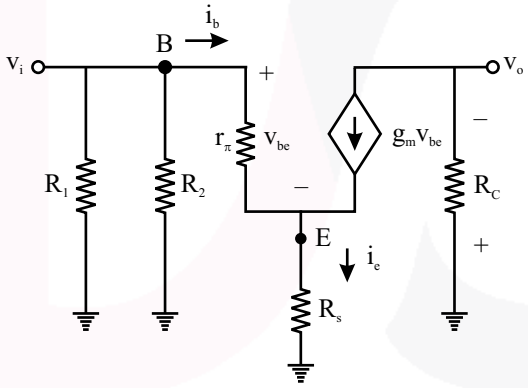
Case-II : AC Analysis

For AC analysis coupling capacitors and emitter bypass capacitor are replaced by short circuit , BJT

is replaced by its small signal model and biasing voltages are replaced by ground or short circuit as under



Above circuit can be redrawn as under,



Output voltage of amplifier,

$$v_o = -(g_m v_{be})\, R_L$$

$$\Rightarrow \quad v_o = -g_m R_C\, v_{be} \qquad \text{.....(i)}$$

From input circuit, $v_i = v_{be} + g_m\, v_{be} R_S$

$$\Rightarrow \quad v_{be} = \frac{v_i}{1 + g_m R_S} \qquad \text{.....(ii)}$$

From (i) and (ii), we have,

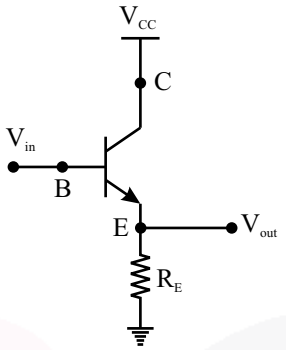
$$v_o = -\frac{g_m R_C}{1 + g_m R_S}$$

Voltage gain of the amplifier,

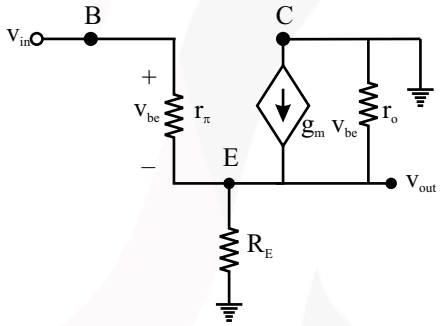
$$A_v = \frac{v_o}{v_i} = -\frac{g_m R_C}{1 + g_m R_S}$$

$$\Rightarrow \quad A_v = \frac{0.087 \times 5 \times 10^3}{1 + 0.087 \times 10} = -232.62$$

Q.11 Ans (b)



Replacing BJT by its small signal model and biasing voltage by ground, the AC equivalent circuit of the amplifier becomes as under,



Applying KCL at node 'E', we have,

$$\frac{V_{out} - V_{in}}{r_\pi} + \frac{V_{out}}{R_E} + \frac{V_{out}}{r_o} - g_m v_{be} = 0$$

voltage, $v_{be} = V_{in} - V_{out}$

$$\Rightarrow \quad \frac{V_{out} - V_{in}}{r_\pi} + \frac{V_{out}}{R_E} + \frac{V_{out}}{r_o} - g_m (v_{be} - V_o) = 0$$

$$\Rightarrow \quad V_{out}\left(\frac{1}{r_\pi} + g_m + \frac{1}{R_E} + \frac{1}{r_o}\right) = \left(\frac{1}{r_\pi} + g_m\right) V_{in}$$

Voltage gain of amplifier,

$$\Rightarrow \quad \frac{V_{out}}{V_{in}} = \frac{\frac{1}{r_\pi} + g_m}{\frac{1}{r_\pi} + g_m + \frac{1}{R_E} + \frac{1}{r_o}}$$

Normally, r_π & r_o are very large for BJT amplifier.

$$\therefore \quad \frac{V_{out}}{V_{in}} \approx \frac{g_m}{g_m + \frac{1}{R_E}}$$

If $g_m >> \frac{1}{R_E}$ then $\frac{V_{out}}{V_{in}} = 1$

It is observed here that the voltage gain becomes almost constant if

$$g_m >> \frac{1}{R_E}$$

$$\Rightarrow \quad g_m R_E >> 1$$

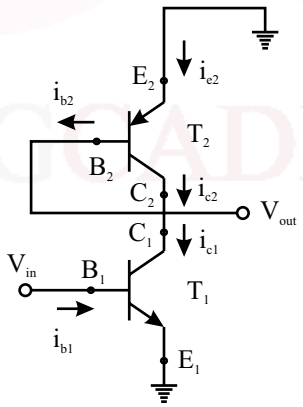
Transconductance of BJT, $g_m = \frac{I_C}{V_T}$

$$\Rightarrow \quad \frac{I_C}{V_T} R_E >> 1$$

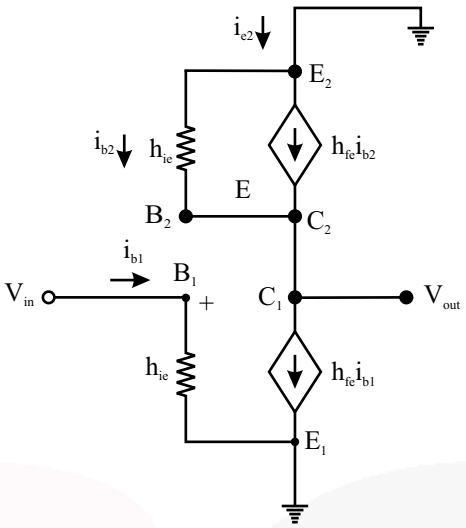
$$\Rightarrow \quad I_C R_E >> V_T$$

Thus the voltage gain becomes almost constant if $I_C R_E >> V_T$

Q.12 Ans: – 1.1 to – 0.9



Replacing both BJTs by their approximate h-parameter models, the ac equivalent circuit becomes as under,



Base current of T_1, $$i_{b1} = \frac{V_{in}}{h_{ie}} \quad \text{.....(i)}$$

Base current of T_2, $$i_{b2} = -\frac{V_{out}}{h_{ie}} \quad \text{.....(ii)}$$

Applying KCL at node 'C_2', we have,

$$\frac{V_{out}}{h_{ie}} + h_{fe}i_{b1} - h_{fe}i_{b2} = 0$$

Putting expression of i_{b1} and i_{b2} from (i) & (ii) in above equation, we have,

$$\frac{V_{out}}{h_{ie}} + h_{fe}\cdot\frac{V_{in}}{h_{ie}} + h_{fe}\cdot\frac{V_{out}}{h_{ie}} = 0$$

$$\Rightarrow \quad V_{out}\left[\frac{1}{h_{ie}} + \frac{h_{fe}}{h_{ie}}\right] = -\frac{h_{fe}}{h_{ie}}\cdot V_{in}$$

Voltage gain, $$A_v = \frac{V_{out}}{V_{in}} = -\frac{h_{fe}}{1+h_{fe}}$$

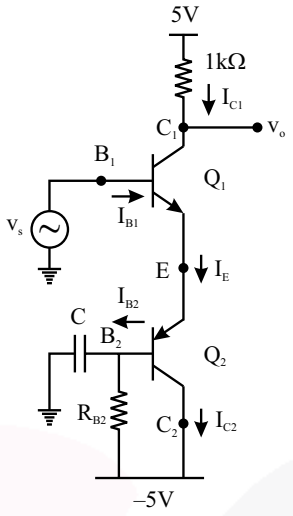
For a BJT, $h_{fe} = \beta$,

$$\Rightarrow \quad A_v = -\frac{\beta}{1+\beta}$$

If $\beta >> 1$ then $1+\beta \approx \beta$

$$\Rightarrow \quad A_v = -\frac{\beta}{\beta} = -1$$

Q.13 Ans. : 49.0 to 51.0



Given, β is large, $I_{C1} = I_{C2} = 2.6\ \text{mA} = I_C$

Emitter current, $I_E = I_C = 2.6\ \text{mA}$

Thermal voltage,

$$V_T = 26\ \text{mV}$$

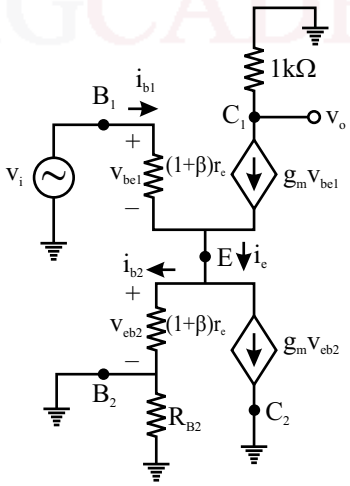
Transconductance of BJTs,

$$g_{m1} = g_{m2} = \frac{I_C}{V_T} = \frac{2.6}{26} = 0.1\,\text{A/V}$$

Emitter resistance,

$$r_e = \frac{V_T}{I_E} = \frac{26}{2.6} = 10\Omega$$

Replacing biasing voltages by groud, coupling capacitors by short circuit and BJTs by its small signal model, the AC equivalent circuit becomes as shown below



From above circuit

$$v_o = -g_m v_{be1} \times 1k \quad \text{.....(i)}$$

From base circuit of both BJTs,

$$v_s = v_{be1} + v_{be2} \quad \text{.....(ii)}$$

If β of transistors is large and emitter current is same as collector current, then,

$$i_{c1} = i_{c2}$$

$$\Rightarrow \quad g_m v_{be1} = g_m v_{eb2}$$

$$\therefore \quad v_{be2} = v_{be1} \quad \text{.....(iii)}$$

From (ii) and (iii), we have,

$$\Rightarrow \quad v_s = 2v_{be1}$$

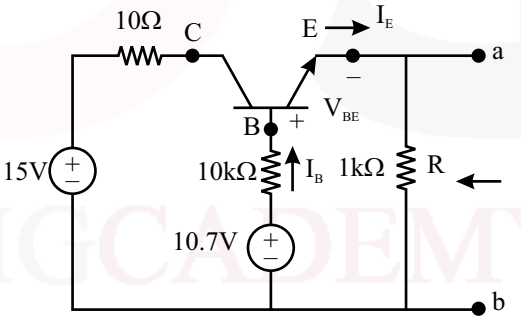
$$\Rightarrow \quad v_{be1} = \frac{v_s}{2} \quad \text{.....(iv)}$$

From (i) and (iv), we have,

$$v_o = -0.1 \times \frac{v_s}{2} \times 1 \times 10^3 = -50 v_S$$

Voltage gain, $\left|\frac{v_o}{v_s}\right| = 50$

Q.14 Ans.(*)



Given, $\beta = 100$, $V_{BE} = 0.7V$

Applying KVL in base-emitter circuit,

$$10.7 - 10k\, I_B - V_{BE} - 1k\, I_E = 0$$

Emitter current,

$$I_E = (1 + \beta) I_B = (1 + 100) I_B$$

$$\Rightarrow \quad 10.7 - 10k\, I_B - 0.7 - 1k\,(1 + 100) I_B = 0$$

$$\Rightarrow \quad I_B = \frac{10.7 - 0.7}{10k + 10k} = \frac{10}{111} mA$$

Emitter current,

$$I_E = 101 \times \frac{10}{111} \text{mA}(1+\beta)I_B$$

Emitter resistance,

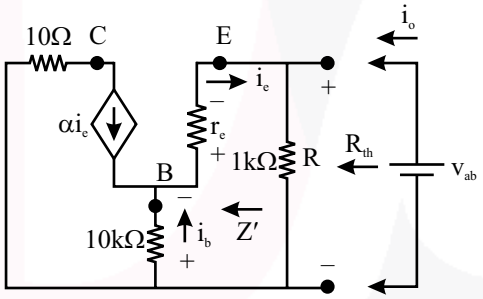
$$r_e = \frac{V_T}{I_E}$$

where $V_T = 26$ mV, thermal voltage

$$\therefore \quad r_e = \frac{26}{1010} \times 111\Omega$$

Current gain, $$\alpha = \frac{\beta}{1+\beta} = \frac{100}{101}$$

Replacing BJT by its small signal T-model, and biasing voltage by short circuit the AC equivalent circuit of the amplifier becomes as shown below,



The thevenin's equivalent resistance seen across ab can be obtained by ..... a voltage source v_o across terminals as shown above.

Applying KCL at node 'B', we have

$$i_e = i_b + \alpha i_e$$

$$\Rightarrow \quad i_b = (1-\alpha) i_e$$

Applying KVL, we have,

$$-v_{ba} + i_e r_e + 10\, i_b = 0$$

$$v_{ba} = 10\text{k}\, i_b + i_e r_e$$

$$= 10\text{k}(1-\alpha)\, i_e + i_e r_e$$

Impedance, $$Z' = \frac{v_{ba}}{i_e}$$

$$\Rightarrow \quad Z' = 10\text{k}(1-\alpha) + r_e = 10 \times 10^3 \left[1 - \frac{100}{101}\right] + \frac{26}{1010} \times 111 = 101.86\ \Omega$$

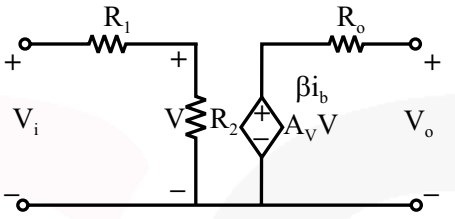
Thevenin's equivalent resistance seen across ab

$$R_{ab} = Z' \parallel R$$

$$\Rightarrow \quad R_{ab} = -\frac{101.86\times1\times10^3}{101.86+1\times10^3} = 92.45\ \Omega$$

Note : As per GATE answer key answer is 9.5 to 10.5

Q.15 Ans.(a)



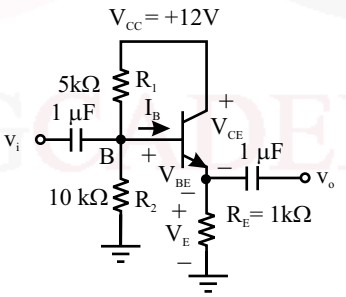
From input side, $V = \frac{R_2}{R_1+R_2}\cdot V_i$

From output side, $V_o = A_v V$

$$\Rightarrow \quad V_o = A_v \cdot \frac{R_2}{R_1+R_2}\cdot V_i$$

$$\Rightarrow \quad \frac{V_o}{V_i} = A_v \cdot \frac{R_2}{R_1+R_2}$$

Q.16 Ans : 9.39 to 9.41



When β is large. The base current is negligible. In that case voltage at base,

$$V_B = \frac{R_2}{R_1+R_2}\times V_{cc} = \frac{10}{10+5}\times12 = 8V$$

Then the voltage at emitter terminal,

$$V_E = V_B - V_{BE} = 8 - 0.7 = 7.3\ V$$

Voltage V_{CE} at Q-point,

$$V_{CEQ} = V_{CC} - V_E = 12 - 7.3 = 4.7\ V$$

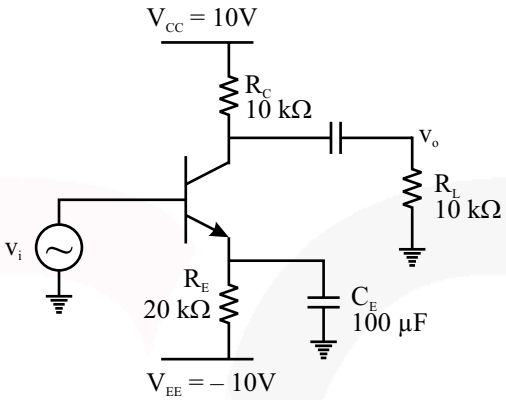
Maximum peak to peak swing of output voltage without distortion is given by,

$$V_{o(p\text{-}p)} = 2(V_{CEQ} - V_{CE(sat)})$$

If $V_{CE(sat)}$ is negligible then ,

$$V_{o(p\text{-}p)} = 2V_{CEQ} = 2 \times 4.7 = 9.4\ V$$

Q.17 Ans(a)



Low frequency voltage gain of the circuit shown above can be given by,

$$A_v = \frac{v_o}{v_i} = -g_m\left(R_C \parallel R_L\right)$$

Where, $g_m = \frac{I_C}{V_T}$; I_C is DC bias collector current.

From base circuit, the KVL for DC bias signals gives,

$$0 - V_{BE} - I_E R_E - V_{EE} = 0$$

$$\Rightarrow \quad I_E = \frac{-0.7 - (-10)}{20}\text{mA}$$

$$\Rightarrow \quad I_E = \frac{9.3}{20}\text{mA}$$

Collector current, $I_C = I_E - I_B$

As base current of given circuit is negligible so,

$$I_C = I_E = \frac{9.3}{20}\text{mA}$$

Transconductance of BJT,

$$g_m = \frac{I_C}{V_T} = \frac{9.3}{20 \times 26}$$

Voltage gain of amplifier,

$$A_v = -g_m(R_C \| R_L)$$

$$= -\frac{9.3}{20\times 26}\times\frac{10\times 10}{10+10}\times 10^3$$

$$\Rightarrow \quad A_v = -89.42$$

❐❐❐

Ch 5 Small Signal Analysis of FETs

5.1 Introduction

A Field Effect Transistor (JFET & MOSFET) based amplifier provides excellent voltage gain and offers very high input impedance. The voltage gain of FET amplifiers is normally less than BJT amplifier but it offers much higher input impedance. However, output impedances are comparable for both types of amplifiers. The FETs are voltage controlled devices and their small signal models are simpler than BJT amplifiers . Analysis of BJT amplifier is performed using current gain β and analysis of FETs based amplifiers is performed using transconductance gain g_m. The small signals are the AC signals with small amplitude and low frequency. The amplitude of AC signals is kept smaller as compared to DC biasing signals for operation of the circuit in linear region of operation as an amplifier. Consider a MOSFET amplifier circuit as shown in Fig 1.

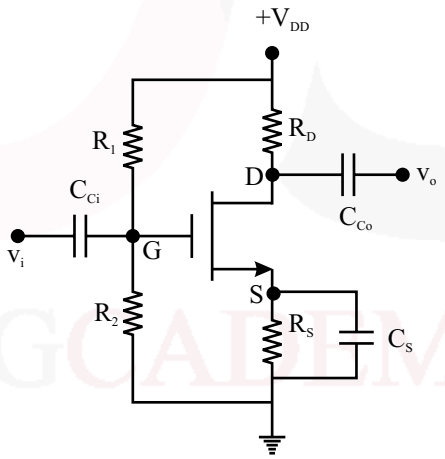


Fig.1 MOSFET amplifier with coupling and bypass capacitors

The amplifier circuit is subjected to both small AC signals and DC biasing signals. The DC biasing signals are responsible for fixing the operating point of FET in saturation region for amplifier operation. Small AC signals at input gate terminal is signal to be amplified. The input and output terminals are connected to the amplifier circuit through coupling capacitors C_{Ci} and C_{Co}, respectively. The coupling capacitors are used to block DC biasing signals from input and output terminals of the amplifier. The source bypass capacitor C_S is used to bypass source resistance in case of AC signals. It helps in increasing the gain of amplifier. A MOSFET amplifier require both AC as well as DC

analysis for small signal analysis of the amplifier. DC analysis is used to find operating point of the amplifier and AC analysis of amplifier gives input impedance, output impedance and voltage gain of the amplifier. The MOSFET amplifier circuit can be analyzed by decoupling the DC analysis and AC analysis by adopting the following techniques

I. DC analysis : Replace coupling and source bypass capacitors by open circuit for DC analysis of the amplifier.

II. AC analysis : The AC analysis is performed by replacing DC biasing voltage signals by ground or short circuit and current source by open circuit, coupling capacitors and bypass capacitor by open circuit and MOSFET by its small signal model.

In this text the biasing signals are normally represented by capital letters with capital subscript i.e. V_{GS}, V_{DS}, V_{DD}, I_D etc. The AC signals are represented by small letters with subscript of small letters only e.s. v_{gs}, v_{ds}, i_d etc. The composite signals as sum of DC and AC signals are represented by the symbols with small letters with subscript of capital letter i.e., v_{GS}, v_{DS}, i_D etc.

Mathematically, the composite signals are algebraic sum of AC and DC signals as under,

$$v_{GS} = V_{GS} + v_{gs}$$

$$i_D = I_D + i_d$$

and

$$v_{DS} = V_{DS} + v_{ds}$$

Where, v_{gs}, i_d and v_{ds} are AC signals and V_{GS}, I_D and V_{DS} are DC biasing signals.

The transfer characteristic exhibiting small signal operation of FET as linear amplifier is shown in Fig.2.

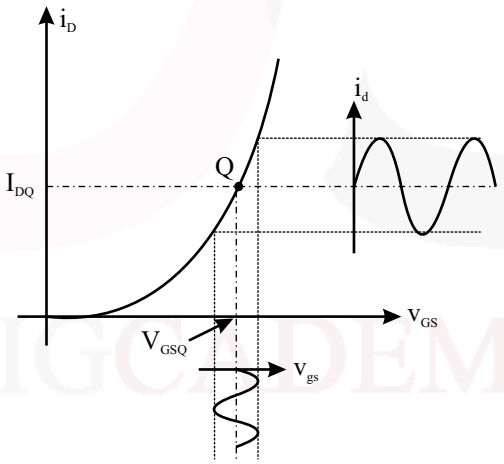


Fig.2 Transfer characteristics and small signal operation of FET amplifier.

When FET is biased at point Q, the small variations of signals about Q is linear.

5.2 Small Signal Model of FETs

The small signal model which performing the AC analysis of the amplifiers. The small signal model of FETs is represented in manner similar to that of a BJT. The small signal model of FETs can be derived by using the relation between drain current, drain to source voltage and gate to source voltage for signals. The drain current for small signal is formally represent as function of drain to source voltage and gate to source voltage as under,

$$i_D = f(v_{GS}, v_{DS}) \quad (1)$$

If both gate and drain voltages are variable then the drain current can be obtained by considering only first two terms of Taylor's series expansion, the drain current of FET can be given by,

$$\Delta i_D = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}} \cdot \Delta v_{GS} + \left.\frac{\partial i_d}{\partial v_{DS}}\right|_{V_{GS}} \cdot \Delta v_{DS} \quad (2)$$

For small signals, $\Delta i_D = i_d$, $\Delta v_{DS} = v_{ds}$, $\Delta v_{GS} = v_{gs}$

$$\Rightarrow \quad \boxed{i_d = g_m v_{gs} + \frac{1}{r_o} . v_{ds}} \quad (3)$$

where, $$g_m = \left.\frac{\delta i_d}{\delta v_{GS}}\right|_{V_{DS} = \text{constant}} \quad (4)$$

and $$r_o = \left.\frac{\delta v_{DS}}{\delta i_D}\right|_{V_{GS} = \text{constant}} \quad (5)$$

The parameter g_m is called mutual conductance or transconductance of FET. It is also designated as common source forwarded transconductance. The second parameter r_o is drain resistance of the FET for saturation region of operation.

i. For enhancement type n-channel MOSFET:

$$g_m = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_T) \quad (6)$$

and $$r_o = \frac{1}{g_o} = \frac{1}{I_D' \lambda} = \frac{V_A}{I_D'} \quad (7)$$

Where, $$I_D' = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2 \quad (8)$$

The current I_D' is drain current without channel length modulation effect taken into account and V_A is early voltage of FET.

ii. For enhancement type p-channel MOSFET:

$$g_m = \frac{\mu_p C_{ox} W}{L}(V_{SG} - |V_T|) \quad (9)$$

and $$r_o = \frac{1}{g_o} = \frac{1}{I_D' \lambda} = \frac{V_A}{I_D'} \quad (10)$$

Where, $$I_D' = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{SG} - |V_T|)^2 \quad (11)$$

iii. For depletion type n-channel MOSFET:

$$g_m = \frac{2I_{DSS}}{|V_T|}\left(1-\frac{V_{GS}}{V_T}\right) \quad (12)$$

where, $$I_{DSS} = \frac{\mu_n C_{ox} W}{2L} V_T^{\,2} \quad (13)$$

iv. For n-channel JFET :

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1-\frac{V_{GS}}{V_P}\right) \quad (14)$$

Where, V_T is threshold voltage of MOSFET, $C_{ox}W/L$ is called transconductance parameter of MOSFET and V_P is called pinch-off voltage of JFET and I_{DSS} is JFET drain current when gate is shorted with source terminal.

Small Signal Voltage Gain or Amplification Factor of FET :

The small signal voltage gain of JFET and MOSFET is defined by,

$$\mu = \frac{\partial v_{DS}}{\partial v_{GS}} \quad (15)$$

$$\Rightarrow \quad \mu = \frac{\partial v_{DS}}{\partial i_D} \times \frac{\partial i_D}{\partial v_{GS}} = r_o g_m \quad (16)$$

The small signal model of FETs can be drawn by using equation (3). The input impedance of FETs is very high so the gate terminal is left open circuited in small signal model. The drain to source circuit is obtained using equation (3). The drawn current of FET is sum of two terms which means the drain current is split in two parallel branches in its small signal model. The term v_{ds}/r_o of equation (3) represents drain or output resistance connected between drain and source and the term $g_m v_{gs}$ represents a voltage dependent current source connected between drain and source terminals in shunt with resistance as shown in Fig. 3 and Fig. 4.

Small Signal Model of JFET :

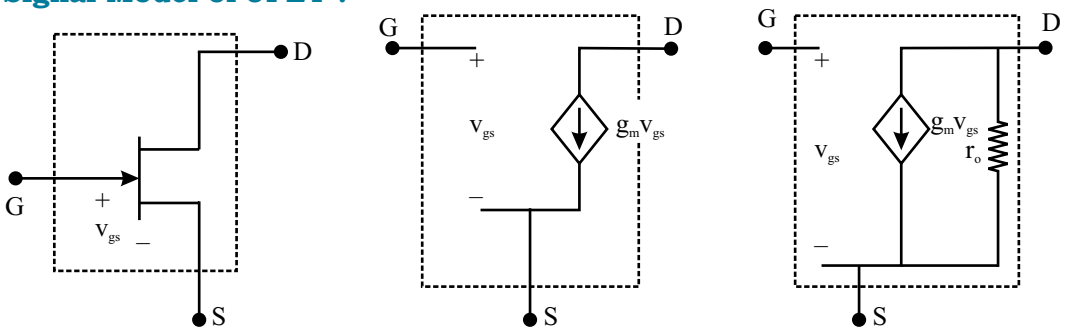


Fig. 3 (a) JFET (b) small signal model of JFET without channel modulation effect (c) small

signal model of JFET with channel modulation effect.

Small signal model of MOSFET :

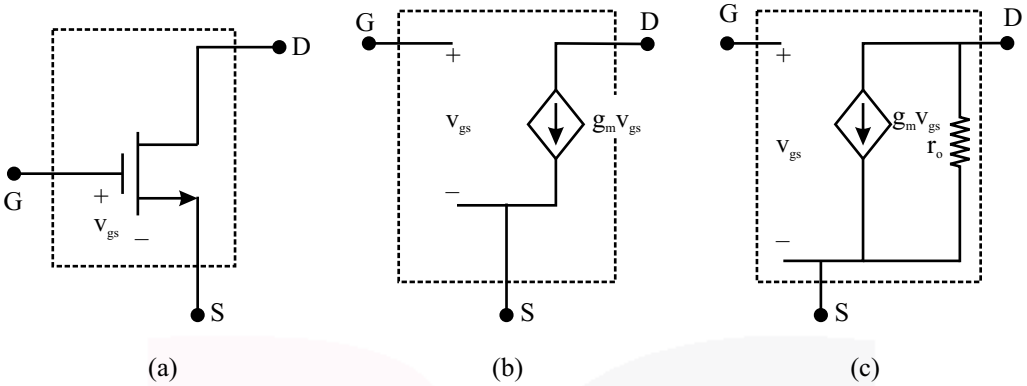


Fig. 4 (a) MOSFET (b) small signal model of MOSFET without channel modulation effect (c) small signal model of MOSFET with channel modulation effect.

The drain or output resistance r_o is infinite when channel modulation effect is not taken into account and it is not included in small signal model. However, when channel modulation effect is also taken into account the drain resistance is given by.

$$r_o = \frac{|V_A|}{I_D} = \frac{1}{\lambda I_D} \tag{17}$$

Where λ is called channel length modulation parameter and $|V_A| = \frac{1}{\lambda}$ is also known as process-technology parameter. The drain resistance is also known as output resistance of MOSFET also denoted by r_d.

5.3 Graphical Method of Determination of Transconductance (g_m) and Drain Resistance (r_o)

Case-I : Determination of g_m

Transconductance of MOSFET is defined as

$$g_m = \frac{\partial i_d}{\partial v_{gs}} \simeq \frac{\Delta i_d}{\Delta v_{gs}}\bigg|_{v_{ds}=\text{fixed}} \tag{18}$$

The transconductance of FET is related to drain current (i_D) and gate-to-source voltage (v_{GS}). The transfer characteristics of MOSFET shown in Fig.5 also gives the relation between drain current and gate to source voltage. Therefore, the transfer characteristics of MOSFET can be used to determine the transconductance of the MOSFET.

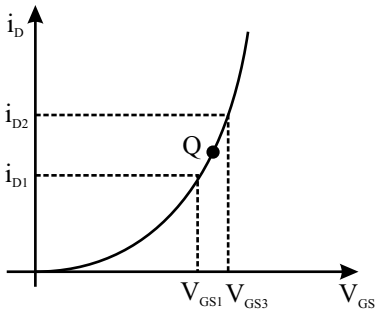


Fig. 5 Transfer characteristics of MOSFET

For small signal variations

$$\Delta v_{GS} = V_{GS2} - V_{GS1} \quad (19)$$

$$\Delta i_D = I_{D2} - I_{D1} \quad (20)$$

$$\therefore \quad g_m = \frac{I_{D2} - I_{D1}}{V_{GS2} - V_{GS1}} \quad (21)$$

Case-II : Determination of r_o

The output resistance of MOSFET is defined by,

$$r_o = \frac{\partial v_{ds}}{\partial i_d} \approx \frac{\Delta v_{DS}}{\Delta i_D}\bigg|_{V_{DS}=\text{fixed}} \quad (22)$$

As r_o is related to drain-to-source voltage,v_{ds}, and drain current,i_d, which determine the output characteristics of MOSFET, therefore, output characteristics shown in Fig. 6 can be used to determined the value of drain resistance of MOSFET.

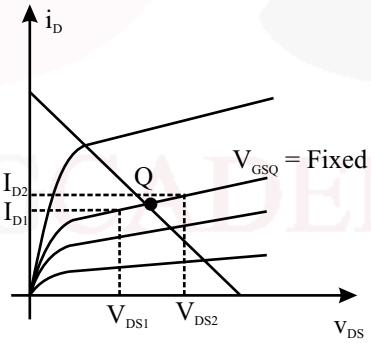


Fig. 6 Output characteristics of n-MOSFET and small signal variations

For small signal variations about the Q-point,

$$\Delta v_{DS} = V_{DS2} - V_{DS1}$$

$$\Delta i_D = I_{D2} - I_{D1}$$

Putting above relations in equation (22), we have,

$$r_o = \frac{V_{DS2} - V_{DS1}}{I_{D2} - I_{D1}} \quad (23)$$

5.4 Small Signal Analysis of MOSFET Amplifiers

5.4.1 Analysis of Potential Divider Bias Common Source n-MOSFET Amplifier

A common-source n-MOSFET amplifier with potential divider bias with AC signals connected through coupling capacitors is shown in Fig. 7.

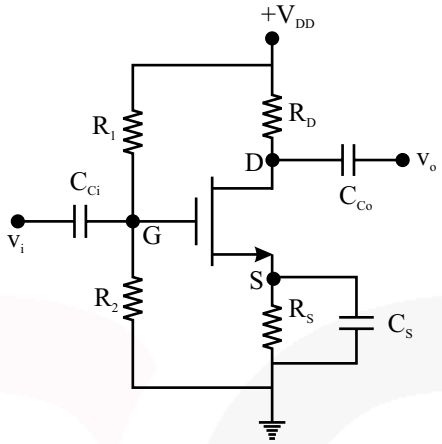


Fig. 7 Common source n-MOSFET amplifier with potential divider bias

The AC equivalent of the amplifier is can be drawn by replacing biasing voltage by ground, coupling and bypass capacitors by short circuit and MOSFET by its small signal equivalent as shown in Fig.8.

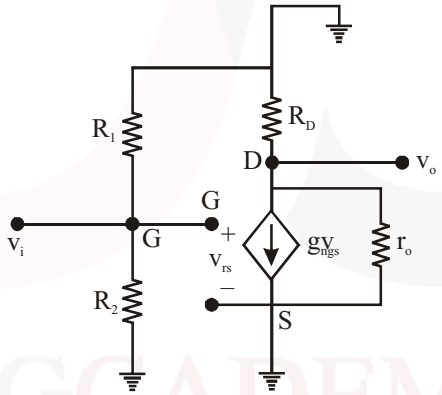


Fig. 8 AC equivalent circuit of common source n-MOSFET amplifier with potential divider bias

Above circuit can be redrawn as shown below in Fig.9

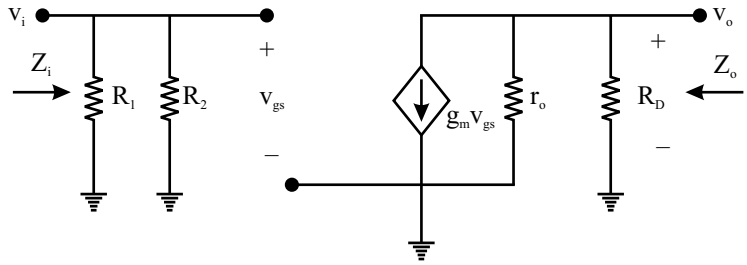


Fig. 9 Simplified AC equivalent circuit of common source n-MOSFET amplifier with potential divider bias

i. Input impedance

The impedance seen from input terminals of the amplifier,

$$\boxed{Z_i = R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2}} \tag{24}$$

ii. Output Impedance

The output impedance of the amplifier is impedance seen across output terminals of the amplifier with input of the amplifier set to zero. If input voltage of the amplifier is set to zero, $v_i = v_{gs} = 0$, then the voltage dependent current source, $g_m v_{gs}$, becomes zero and behaves like open circuit. Then the output impedance seen across output terminals becomes as under,

$$\boxed{Z_o = r_o \,||\, R_D = \frac{r_o R_D}{r_o + R_D}} \tag{25}$$

iii. Voltage Gain

From input side, $v_{gs} = v_i$

Output voltage, $v_o = -g_m v_{gs} \times (r_o \,||\, R_D) = g_m v_i (r_o \,||\, R_D)$ (26)

$\therefore$ Voltage gain of amplifier,

$$A_v = \frac{v_o}{v_i} = -g_m (r_o \,||\, R_D) \tag{27}$$

$\Rightarrow$

$$\boxed{A_v = -g_m \times \frac{r_o R_D}{r_o + R_D}} \tag{28}$$

If channel modulation effect is neglected then $r_o = \infty$

Then $Z_o = R_D$ (29)

and $A_v = g_m R_D$ (30)

5.4.2 Analysis of Common Source Drain Feedback n-MOSFET Amplifier

A common source drain feedback amplifier consists of resistance connected between drain and gate terminals of the MOSFET as shown in Fig. 10. The input and output terminals are connected through coupling capacitors.

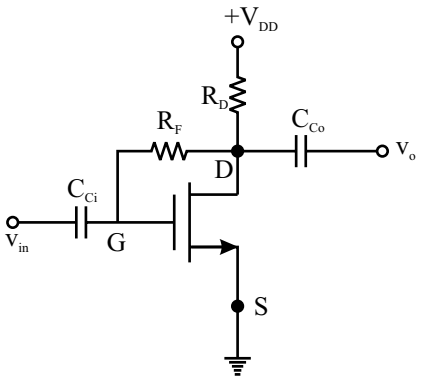


Fig. 10 Common source drain feedback n-MOSFET amplifier

The AC equivalent circuit of the amplifier can be drawn by replacing biasing voltage source V_{DD} by ground, coupling capacitors by short circuit and MOSFET by its small signal model as shown in Fig. 11.

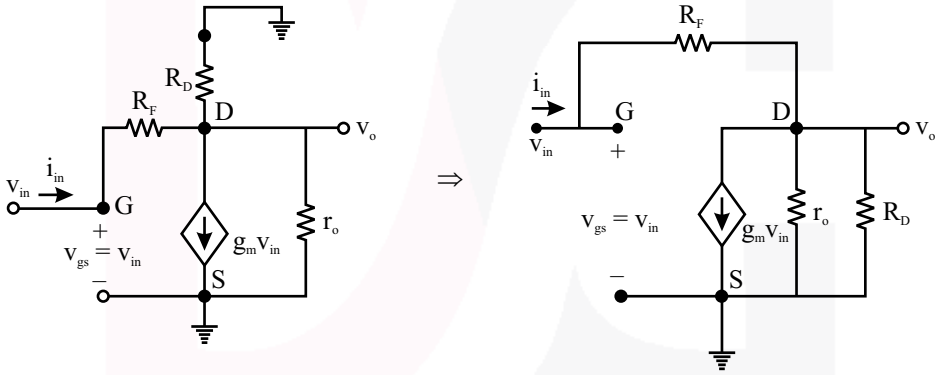


Fig. 11 AC equivalent circuit of common source drain feedback n-MOSFET amplifier

i. Input Impedance (Z_i)

Applying of KCL at node 'G', we have,

$$-i_{in} + \frac{v_{in} - v_o}{R_F} = 0$$

$$-i_{in} R_F + v_{in} - v_o = 0 \qquad (31)$$

Applying KCL at node 'D', we have,

$$\frac{v_o}{r_o} + \frac{v_o}{R_D} + \frac{v_o - v_{in}}{R_F} + g_m v_{gs} = 0$$

From input circuit, $v_{gs} = v_{in}$

$$\therefore \quad v_o \left[\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}\right] + \left[g_m - \frac{1}{R_F}\right] v_{in} = 0$$

$$\Rightarrow \quad v_o = \frac{\frac{1}{R_F} - g_m}{\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}} \times v_{in} \tag{32}$$

From (31) and (32), we have,

$$-i_{in} R_F + v_{in} - \frac{\frac{1}{R_F} - g_m}{\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}} v_{in} = 0$$

Input Impedance, $$Z_i = \frac{v_{in}}{i_{in}} = \frac{R_F\left[\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}\right]}{\frac{1}{r_o} + \frac{1}{R_D} + g_m} \tag{33}$$

ii. Voltage gain (A_v)

From equation (32), we have,

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = \frac{\frac{1}{R_F} - g_m}{\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_F}} \tag{34}$$

iii. Output Impedance (Z_o)

Output impedance is impedance seen across output terminals of amplifier by replacing input voltage source by short circuit or ground. Then, the equivalent circuit for output impedance becomes as shown in Fig. 12.

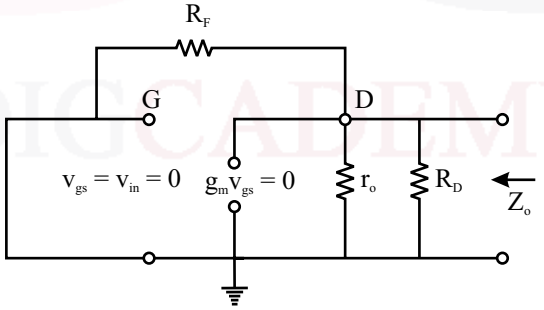


Fig. 12 Equivalent circuit of common source drain feedback n-MOSFET amplifier for ouput impedance

Output impedance, $$Z_o = r_o \parallel R_D \parallel R_F \tag{35}$$

Normally $R_F >> r_o \parallel R_D$

$$\therefore \quad Z_o \approx r_o \parallel R_D \tag{36}$$

5.4.3 Analysis of Common Source Fixed Bias n-MOSFET Amplifier

The CS n-MOSFET amplifier with fixed bias arrangement with voltage and current sources is shown in Fig.13.

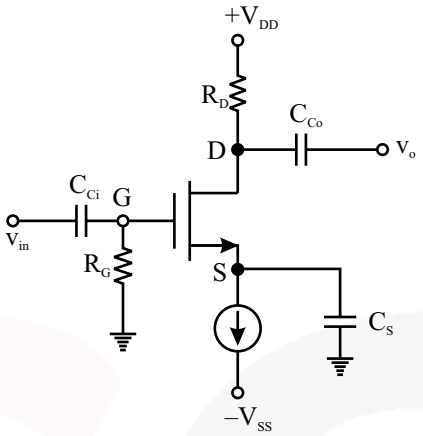


Fig. 13 Common source fixed bias n-MOSFET amplifier

The AC equivalent circuit of the amplifier can be drawn by replacing coupling capacitors (C_{Ci}, C_{Co}) and bypass capacitor (C_S) by short circuit, biasing voltage sources by ground, biasing current source by open circuit and MOSFET by its small signal model as shown below,

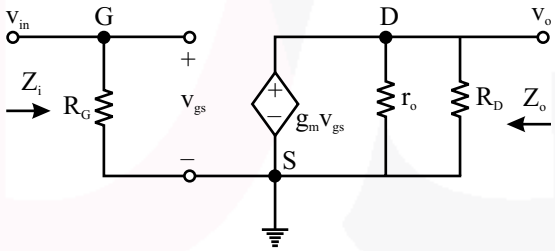


Fig. 14 AC equivalent circuit of common source fixed bias n-MOSFET amplifier

i. Input Impedance

$$Z_i = R_G \tag{37}$$

ii. Voltage Gain

From gate circuit, $v_{gs} = v_{in}$

Output voltage, $$v_o = -g_m v_{gs} (r_o \| R_D) = -\frac{g_m r_o R_D}{r_o + R_D} \times v_{in} \tag{38}$$

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = -\frac{g_m r_o R_D}{r_o + R_D} \tag{39}$$

iii. Output Impedance

Output impedance is impedance seen from output terminals with input source replaced by ground or short circuit. When source is replace by ground or short circuit, $v_{gs} = v_{in} = 0$. The dependent current source, g_m

$v_{gs} = 0$ and behaves like open circuit. Then equivalent circuit of amplifier becomes as shown in Fig. 15.

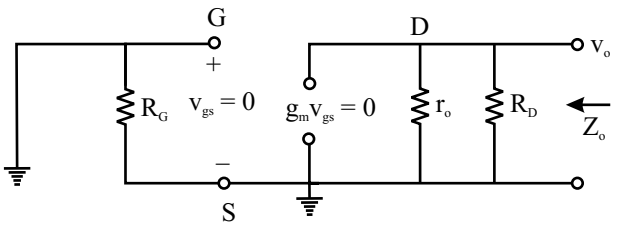


Fig. 15 Equivalent circuit common source fixed bias n-MOSFET amplifier for output impedance

The output impedance, $$Z_o = r_o \| R_D = \frac{r_o R_D}{r_o + R_D} \quad (40)$$

If $r_o >> R_D$ then , $$Z_o \approx R_D \quad (41)$$

5.4.4 Effect of Source and Load Resistances on Parameters of MOSFET Amplifiers

When source and load resistances are also taken into account, the circuit a potential divider based common source NMOS amplifier can be drawn as under,

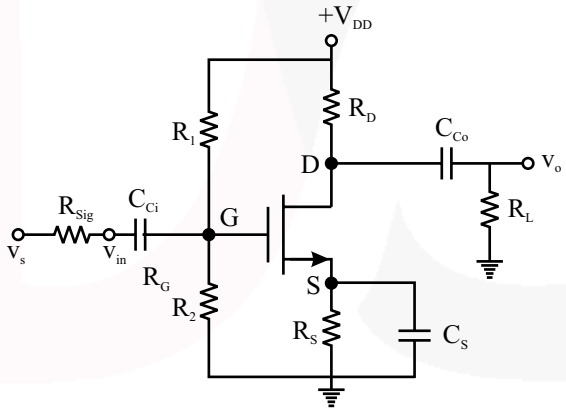


Fig. 16 Common source n-MOSFET amplifier with source and load resistances

The AC equivalent of this amplifier can be drawn by replacing coupling and bypass capacitors by short circuit, biasing voltage source by ground and n-MOSFET by its small signal model as shown below.

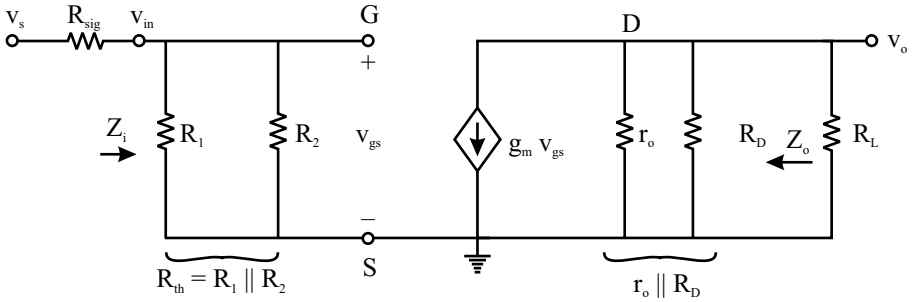


Fig. 17 AC equivalent circuit of common source n-MOSFET amplifier with source and load resistances

i. Input Impedance

The input impedance of the amplifier can be given by,

$$Z_i = R_1 \| R_2 = R_{th} = \frac{R_1 R_2}{R_1 + R_2} \tag{42}$$

ii. Voltage Gain

Output voltage of amplifier,

$$v_o = -g_m v_{gs} \times (r_o \| R_D \| R_L)$$

From input circuit, $v_{gs} = v_{in}$

$$\Rightarrow \quad v_o = -g_m v_{in} (r_o \| R_D \| R_L) \tag{43}$$

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = -g_m (r_o \| R_D \| R_L) \tag{44}$$

If effect of source impedance, R_S is also taken into account then,

$$v_{in} = \frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}} \times v_s \tag{45}$$

Putting above relation in equation (43), we have,

$$\Rightarrow \quad v_o = -g_m \times (r_o \| R_D \| R_L) \times \frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}} \times v_s \tag{46}$$

Voltage gain with respect to source voltage,

$$A_{vs} = \frac{v_o}{v_s} = -g_m (r_o \| R_D \| R_L) \times \frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}} \tag{47}$$

Note : *Negative sign indicates that common source (CS) amplifier acts like an inverter amplifier which shifts phase by 180°.*

iii. Output Impedance :

The output impedance is obtained by setting $v_s = 0$. When $v_s = 0$ the voltage v_{gs} is also zero and hence dependent current source $g_m v_{gs}$ is zero, which means dependent source is open circuited. Then equivalent resistance seen across the output terminals can be obtained from equivalent circuit shown below,

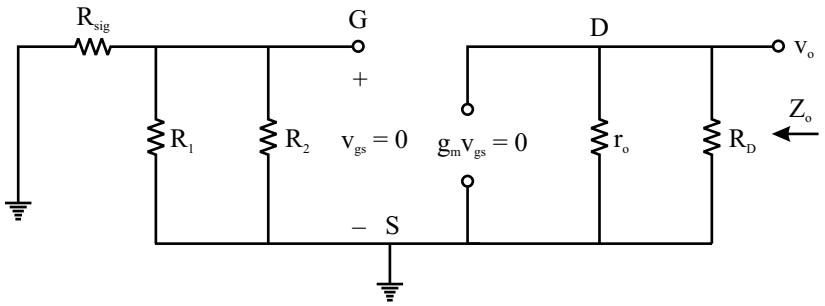


Fig. 18 Equivalent circuit of n-MOSFET amplifier with source and load resistances for output impedance

Output Impedance, $Z_o = r_o \| R_D = \dfrac{r_o R_D}{r_p + R_D}$ (48)

If $r_o >> R_D$ then , $Z_o \approx R_D$ (49)

5.4.5 Common Gate n-MOSFET Amplifier

The circuit of common gate amplifier source terminal as input and drain terminal of n-MOSFET as output is shown in Fig. 19.

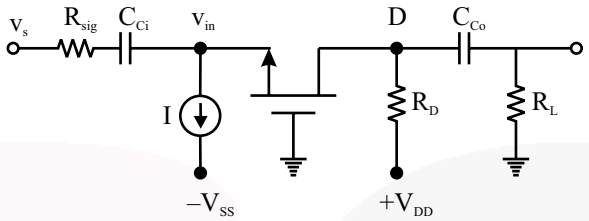


Fig. 19 Common gate n-MOSFET amplifier

The AC equivalent of the amplifier neglecting r_o, can be drawn as shown in Fig. 20.

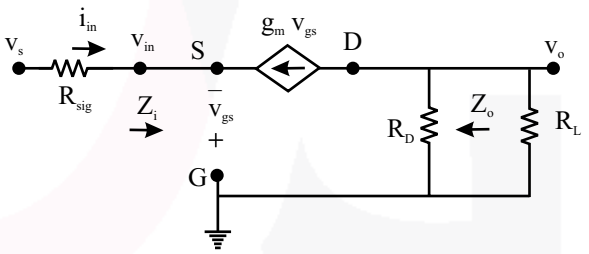


Fig. 20 AC equivalent of common gate n-MOSFET amplifier

i. Inputs Impedance

From inputs circuit, $i_{in} = -g_m v_{gs}$ (50)

and $v_{gs} = -v_{in}$

$\Rightarrow$ $i_{in} = g_m v_{in}$ (51)

Inputs impedance, $Z_i = \dfrac{v_{in}}{i_{in}} = \dfrac{1}{g_m}$ (52)

ii. Voltage Gain

Output voltage, $v_o = -g_m v_{gs} (R_D \| R_L) = -g_m (-v_{in}) \times (R_D \| R_L)$ (53)

$\Rightarrow$ $v_o = g_m (R_D \| R_L) v_{in}$ (54)

Voltage gain, $A_v = \dfrac{v_o}{v_{in}} = g_m (R_D \| R_L)$ (55)

If effect of source resistance is also taken into account then input voltage of amplifier becomes,

$$v_{in} = \frac{Z_i}{Z_i + R_{sig}} \times v_s = \frac{1/g_m}{1/g_m + R_{sig}} \times v_s = \frac{1}{1 + g_m R_{sig}} \times v_s \quad (56)$$

$$\Rightarrow \quad v_o = g_m (R_D \| R_L) \times \frac{1}{1 + g_m R_{sig}} \times v_s \quad (57)$$

Voltage gain with respect to source voltage,

$$\Rightarrow \quad A_{vs} = \frac{v_o}{v_s} = \frac{g_m (R_D \| R_L)}{1 + g_m R_{sig}} \quad (58)$$

iii. Output Impedance

The output impedance is obtained by setting $v_s = 0$. When $v_s = 0$ the voltage v_{gs} is also zero and hence dependent current source $g_m v_{gs}$ becomes zero, which means dependent source is open circuited. Then equivalent resistance seen across the output terminals becomes,

$$Z_o \approx R_D \quad (59)$$

Note : *(i) It seen voltage gain of common gate (CG) amplifier is positive so CG amplifier is non-inverting.*
(ii) Input resistance of CG amplifier is low (i.e. $1/g_m$) where as input impedance of CS amplifier is high.
(iii) Voltage gain of both CS & CG amplifier is nearly identical.
(iv) CG amplifier has superior high frequency response than a CS amplifier.

5.4.6 Common-Drain or Source-Follower Amplifier

The output of common drain amplifier is taken from source terminal and input is given at gate terminal as shown in Fig. 21. The voltage gain of a common drain amplifier is almost unity, so, the source voltage follows the gate voltage due to which this amplifier is also known as source follower amplifier.

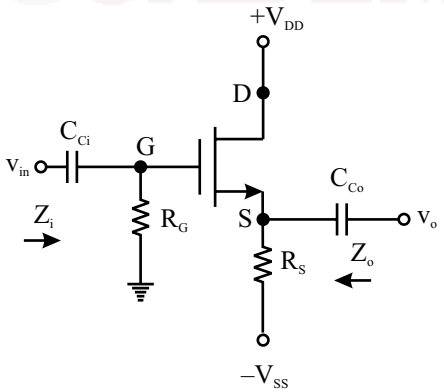


Fig. 21 Common source or source follower n-MOSFET amplifier

The AC equivalent circuit of source follower is drawn by replacing coupling and bypass capacitors by short circuit, biasing voltage sources by ground and n-MOSFET by its small signal model as shown in Fig. 22.

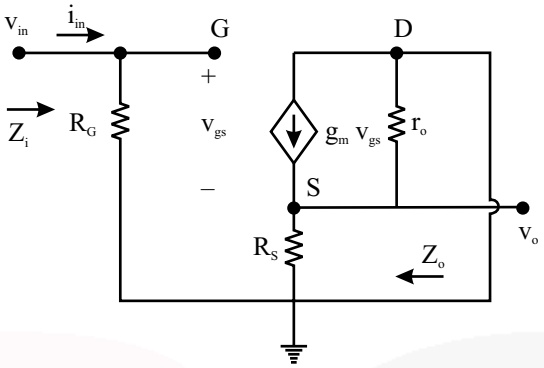


Fig. 22 AC equivalent circuit of source follower n-MOSFET amplifier

i. Input Impedance

The impedance seen from input terminals of the amplifier,

$$Z_i = R_G \tag{60}$$

ii. Voltage Gain

Input voltage, $$v_{in} = v_{gs} + g_m v_{gs} \times (R_S \| r_o) = \left[\left(1 + g_m (R_S \| r_o)\right)\right] v_{gs} \tag{61}$$

Output voltage, $$v_o = (r_o \| R_S)\, g_m\, v_{gs} \tag{62}$$

Voltage gain can be obtained using (61) & (62) as under,

$$A_v = \frac{v_o}{v_{in}} = \frac{(r_o \| R_S) g_m}{1 + g_m (R_S \| r_o)} \tag{63}$$

iii. Output Impedance

The output impedance is obtained by setting $v_{in} = 0$ and connecting an independent voltage v_o across the output terminals. Let i_o is current supplied by the source v_o. Then equivalent circuit of source follower becomes as shown in Fig. 23.

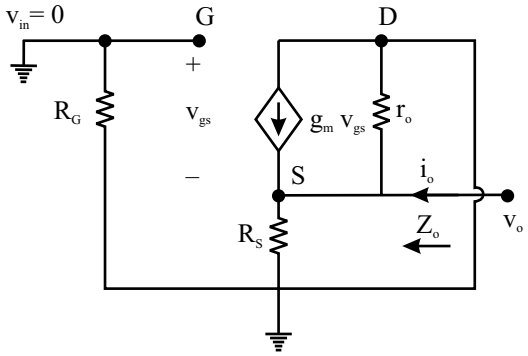


Fig. 23 Equivalent circuit of source follower n-MOSFET amplifier for output resistance

Voltage at node 'S', $v_o = -v_{gs}$ (64)

Applying KCL at node 'S', we have,

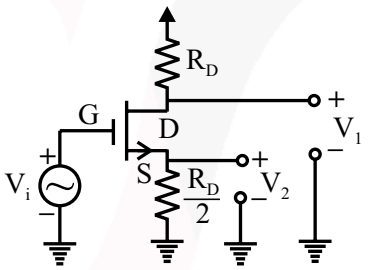
$$-g_m v_{gs} + \frac{v_o}{r_o} + \frac{v_o}{R_S} - i_o = 0 \quad (65)$$

$$\Rightarrow \quad g_m v_o + \frac{v_o}{r_o} + \frac{v_o}{R_S} - i_o = 0 \quad (66)$$

$$\Rightarrow \quad Z_o = \frac{v_o}{i_o} = \frac{1}{g_m + \frac{1}{r_o} + \frac{1}{R_S}} = \frac{1}{g_m} \| r_o \| R_S \quad (67)$$

Example 1

In the MOSFET amplifier of Figure, the signal output V_1 and V_2 obey the relationship

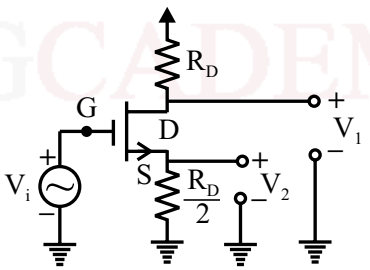


(a) $V_1 = \frac{V_2}{2}$ (b) $V_1 = -\frac{V_2}{2}$

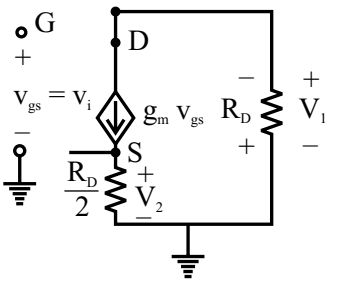
(c) $V_1 = 2V_2$ (d) $V_1 = -2V_2$

GATE(EE/1998/1 M)

Solution : Ans.(d)



Replacing MOSFET by its small signal model(neglecting r_d) the ac equivalent of amplifier can be drawn as under,



From equivalent circuit,

$$V_2 = g_m v_{gs} \times \frac{R_D}{2}$$

$$\Rightarrow \quad V_2 = g_m \times \frac{R_D}{2} v_i \quad [\because v_i = v_{gs}]$$

and

$$V_1 = -g_m v_{gs} R_D = -g_m R_D \cdot v_i$$

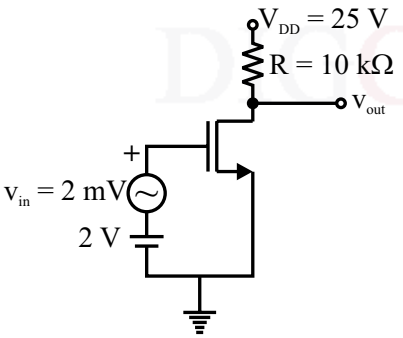
$$\Rightarrow \quad \frac{V_1}{V_2} = \frac{-g_m R_D v_i}{g_m \frac{R_D}{2} \cdot v_i}$$

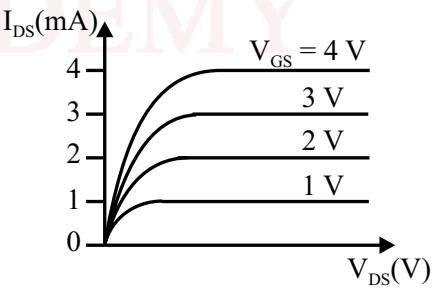
$$\Rightarrow \quad \boxed{V_1 = -2V_2}$$

Example 2

Statement for Linked Answer Questions (i) & (ii) :

Assume that the threshold voltage of the N-channel MOSFET shown in Figure is +0.75 V. The output characteristics of the MOSFET are also shown





(i) The trans-conductance of the MOSFET is

(a) 0.75 mS (b) 1 mS

(c) 2 mS (d) 10 mS

GATE(EE/2005/2 M)

(ii) The voltage gain of the amplifier is

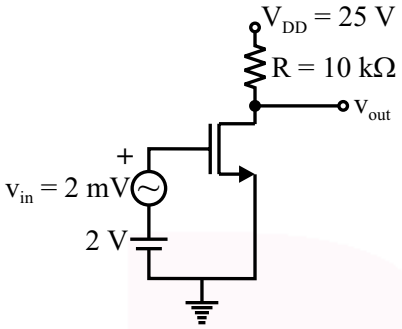
(a) +5 (b) –7.5

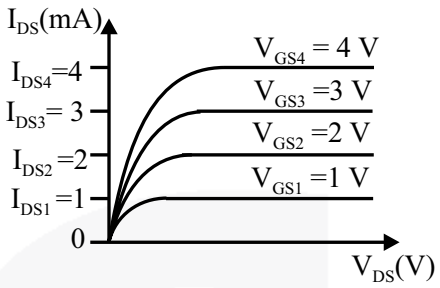
(c) +10 (d) –10

GATE(EE/2005/2 M)

Solution :

(i). Ans.(b)





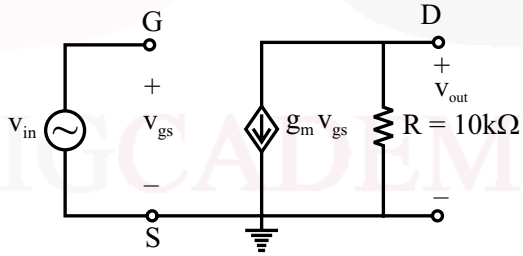
The drain characteristics of the MOSFET are linear. The transconductance of the MOSFET can be obtained from drain characteristics as under,

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} = \frac{I_{DS2} - I_{DS1}}{V_{GS2} - V_{GS1}}$$

$$\Rightarrow \quad g_m = \frac{2-1}{2-1} = 1 \text{ mS}$$

(ii) Ans.(d)

Replacing MOSFET by its small signal model (neglecting r_d) the ac equivalent of amplifier can be drawn as under,



From equivalent circuit,

$$v_{out} = -g_m v_{gs} \cdot R$$

but, $v_{gs} = v_{in}$

$$\Rightarrow \quad v_{out} = -g_m v_{in} R$$

Voltage gain, $$A_v = \frac{v_{out}}{v_{in}} = -g_m R = -1 \times 10 = -10$$

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GATE QUESTIONS

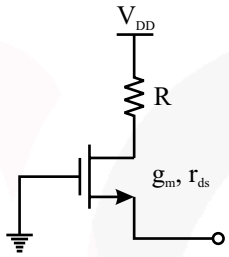
Q.1 A common-source amplifier with a drain resistance, R_D = 4.7 kΩ, is powered using a 10 V power supply. Assuming that the transconductance, g_m, is 520 μA/V, the voltage gain of the amplifier is closest to:

(a) –2.44 (b) –1.22

(c) 1.22 (d) 2.44

GATE(EE/2020/1M)

Q.2 Using the incremental low frequency small-signal model of the MOS device, the Norton equivalent resistance of the following circuit is

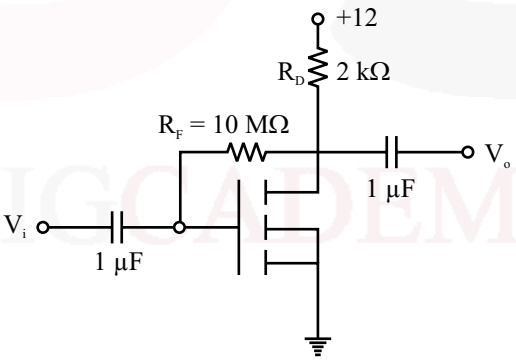


(a) $r_{ds} + R + g_m r_{ds} R$ (b) $\frac{r_{ds} + R}{1 + g_m r_{ds}}$

(d) $r_{ds} + \frac{1}{g_m} + R$ (d) $r_{ds} + R$

GATE(EC/2020/2M)

Q.3 The MOSFET in the amplifier unit shown below has V_{GSQ} = 8V, I_{DSQ} = 6 mA and $V_{GS(Th)}$ = 3V.

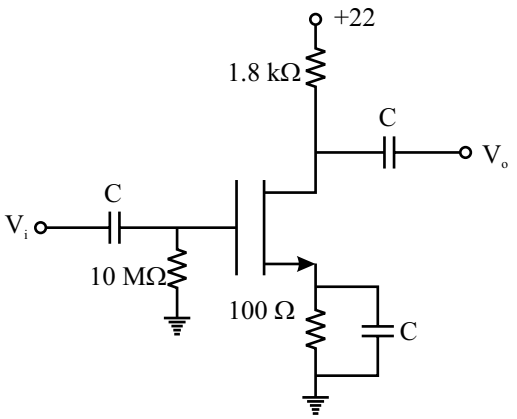


The voltage gain of the amplfier is ....

(a) –1.4 (b) –3.26

(c) –4.8 (d) –5.27

Q.4 The output impedance of amplifier shown in the figure is

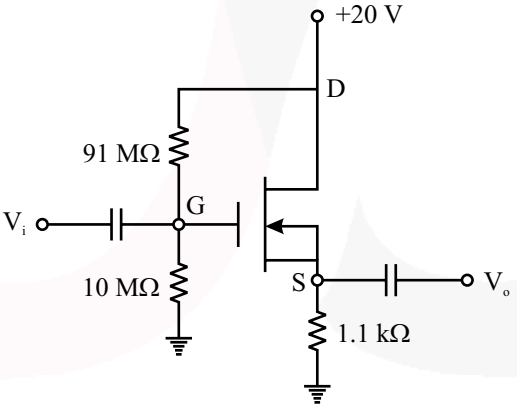


The MOSFET has drain resistance of $r_d = 60\ k\Omega$.

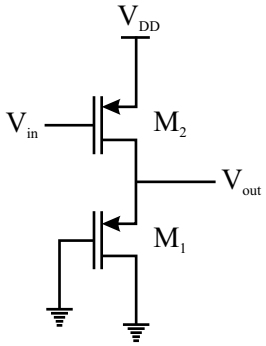
(a) 1.75 kΩ (b) 2.25 kΩ

(c) 0.8 kΩ (d) 3.1 kΩ

Q.5 The depletion MOSFET of amplifier circuit shown below has $I_{DSS} = 12$ mA, $V_{Th} = -3V$ and $r_d = 45$ kΩ. The voltage gain of the amplifier is .....



Q.6 In the circuit shown in the figure, the transistors M_1 and M_2 are operating in saturation. The channel length modulation coefficients of both the transistors are non-zero. The transconductance of the MOSFETs M_1 and M_2 are g_{ml} and g_{m2}, respectively, and the internal resistance of the MOSFETs M_1 and M_2 are r_{01} and r_{02}, respectively.



Ignoring the body effect, the ac small signal voltage gain $\left(\partial V_{out} / \partial V_{in}\right)$ of the circuit is

(a) $-g_{m2}\ (r_{01} \| r_{02})$

(b) $-g_{m2}\left(\frac{1}{g_{m1}} \| r_{02}\right)$

(c) $-g_{m1}\left(\frac{1}{g_{m2}} \| r_{01} \| r_{02}\right)$

(d) $-g_{m2}\left(\frac{1}{g_{m1}} \| r_{01} \| r_{02}\right)$

GATE(EC/2021/1M)

❐❐❐

ANSWERS & EXPLANATIONS

Q.1 ***Ans(a)***

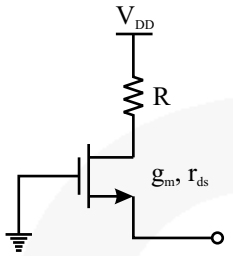
The voltage gain of common source FET amplifier is given by,

$$A_v = -g_m R_D$$

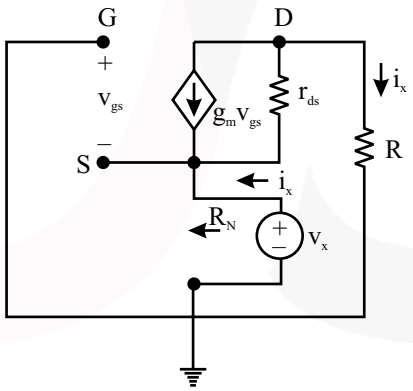
$$\Rightarrow \quad A_v = -520 \times 0^{-6} \times 4.7 \times 10^3$$

$$\Rightarrow \quad A_v = -2.444$$

Q.2 ***Ans(b)***



The small signal equivalent of given circuit, for finding Norton's equivalent resistance, can be drawn as under



The Norton's equivalent resistance of the circuit with dependent sources can be obtained by connecting an independent source across output terminals & replacing all other independent voltage source by short circuit & independent current sources by open circuit as shown above.

Current through R = i_x

Voltage at node 'D' , $v_o = Ri_x$

Voltage at node 'S' = v_x

Gate to source voltage, $v_{gs} = -v_x$

Applying KCL as node 'S', we have,

$$-i_x + \frac{v_x - v_o}{r_{ds}} - g_m v_{gs} = 0$$

$$\Rightarrow \quad -i_x + \frac{v_x - i_x R}{r_{ds}} - g_m(-v_x) = 0$$

$$\Rightarrow \quad -i_x r_{ds} + v_x + g_m r_{ds} v_x - i_x R = 0$$

$$\Rightarrow \quad v_x (1 + g_m r_{ds}) = (r_{ds} + R)\, i_x$$

$$\Rightarrow \quad \frac{v_x}{i_x} = \frac{r_{ds} + R}{1 + g_m r_{ds}}$$

$\therefore$ Norton's equivalent resistance

$$R_N = \frac{v_x}{i_x} = \frac{r_{ds} + R}{1 + g_m r_{ds}}$$

Q.3 ***Ans.(c)***

The drain current of MOSFET is given by,

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \left(V_{GSQ} - V_{GS(Th)} \right)^2$$

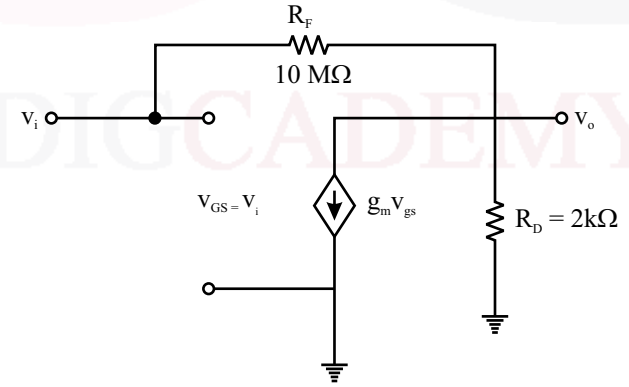
$$\Rightarrow \quad \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} = \frac{6}{(8-3)^2} = \frac{6}{25} \text{mA/V}^2$$

The transconductance of MOSFET,

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L} \left(V_{GSa} - V_{GS(Gh)} \right)$$

$$\Rightarrow \quad g_m = 2 \times \frac{6}{25} \times 10^{-3} (8-3) = \frac{12}{5} \text{mS}$$

The small signal equivalent circuit of amplifier can be drawn as under,



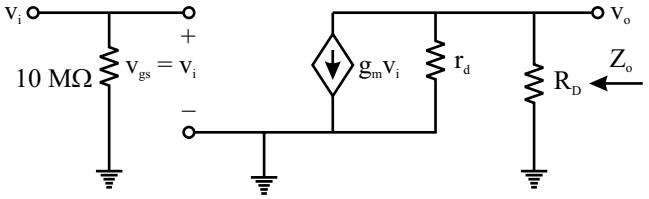
Output voltage, $v_o = -g_m v_{gs} R_D = -g_m R_D v_i$

Voltage gain, $A_v = \frac{v_o}{v_i} = -g_m R_D = -\frac{12}{5} \times 10^{-3} \times 2 \times 10^3$

$$\Rightarrow \quad A_v = -\frac{24}{5} = -4.8$$

Q.4 ***Ans.(a)***

The small signal equivalent Q, circuit of amplifier,



Input is set to zero for finding the output impedance.

$$\therefore \quad Z_o = r_d \,||\, R_D = \frac{1.8 \times 60}{60 + 1.8} = 1.75\,\text{k}\Omega$$

Q.5 ***Ans.: 0.80 to 0.84***

DC voltage at gate terminal,

$$V_G = \frac{10}{10+91} \times 20 = \frac{10}{101} \times 20 = 1.98\,\text{V}$$

Voltage at source terminal, $V_S = I_D R_S$

$$\Rightarrow \quad V_S = 1.1\, I_D$$

Gate to source voltage, $V_{GS} = V_G - V_S = 1.98 - 1.1\, I_D$ V

The drain current of depletion MOSFET is given by,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{Th}}\right]^2$$

$$\Rightarrow \quad I_D = 12\left[1 - \frac{1.98 - 1.1 I_D}{(-3)}\right]^2$$

$$\Rightarrow \quad I_D = \frac{12}{9}\left[3 + 1.98 - 1.1 I_D\right]^2$$

$$\Rightarrow \quad 9\, I_D = 12\,[4.98 - 1.1\, I_D]^2$$

$$\Rightarrow \quad 9\, I_D = 12\,[24.8 + 1.21\, I_D^3 - 10.95\, I_D]$$

$$\Rightarrow \quad 14.52\, I_D^2 - 140.4\, I_D + 297.6 = 0$$

$$I_D = 6.53,\ 3.13\ \text{mA}$$

At $I_D = 3.13$ mA, $V_{GS} = 1.98 - 1.1 \times 3.13 = -1.463$ V

At $I_D = 6.53$ mA, $V_{GS} = 1.98 - 1.1 \times 6.53 = -5.203$ V

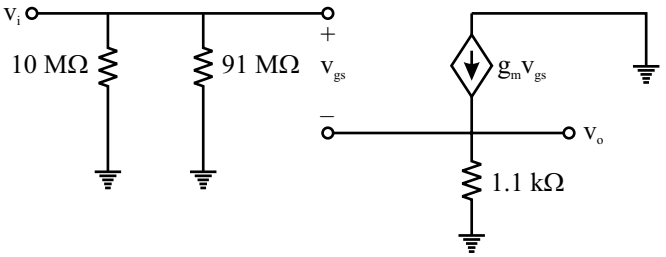
For active region $V_{GS} > V_{Th}$ so $I_D = 3.13$ mA

Trans conductance of MOSFET,

$$g_m = \frac{2 I_{DSS}}{|V_{TH}|}\left[1 - \frac{V_{GS}}{V_{TH}}\right]$$

$$g_m = \frac{2 \times 12}{3}\left[1 - \frac{(-1.463)}{(-3)}\right] \text{mA/V} = 4.10\,\text{mA/V}$$

Small signal equivalent circuit of amplifier,



Output voltage, $v_o = g_m v_{gs} \times 1.1 \times 10^3$

$\Rightarrow$ $v_o = g_m v_{gs} \times 1.1 \times 10^3$

$v_o = (4.10 \times 10^{-3} \times 1.1 \times 10^3)\, v_{gs}$

$v_o = 4.51\, v_{gs}$

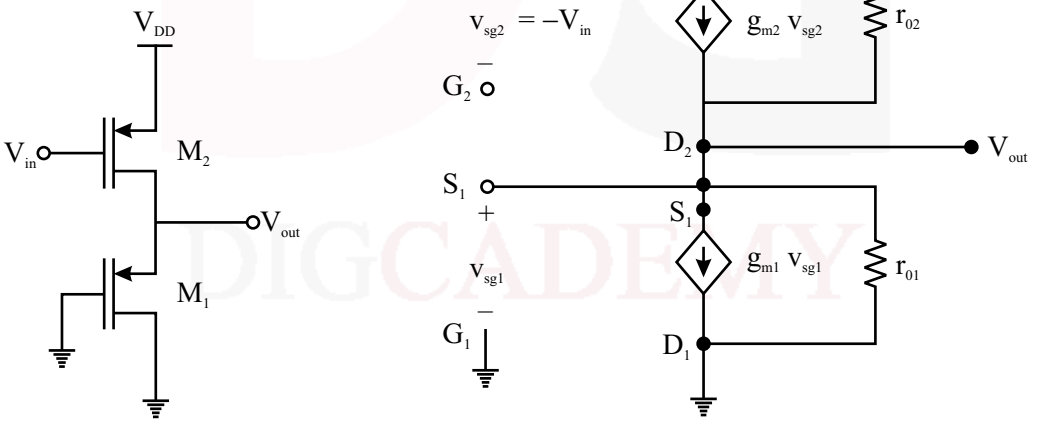
Voltage $v_{gs} = v_i - v_o$

$\Rightarrow$ $v_o = 4.51\,(v_i - v_o)$

$\Rightarrow$ $(1 + 4.51)\, v_o = 4.51\, v_i$

Voltage gain, $A_v = \dfrac{v_o}{v_i} = \dfrac{4.51}{1+4.51} = 0.82$

Q.6 ***Ans.(d)***



(a) Given circuit (b) Small signal equivalent

Replacing DC biasing source by ground and MOSFETs by their small signal model, the ac equivalent circuit becomes as shown above.

Applying KCL at output node, we have,

$$\frac{V_{out}}{r_{01}} + \frac{V_{out}}{r_{02}} - g_{m2}\, v_{sg2} + g_{m1}\, v_{sg1} = 0$$

From above circuit, $v_{sg1} = V_{out}$

and $v_{sg2} = -V_{in}$

$$\Rightarrow \frac{V_{out}}{r_{01}} + \frac{V_{out}}{r_{02}} + g_{m2} V_{in} + g_{m1} V_{out} = 0$$

$$\Rightarrow V_{out}\left[\frac{1}{r_{01}} + \frac{1}{r_{02}} + g_{m1}\right] = -g_{m2} V_{in}$$

$\therefore$ Voltage gain, $$A_v = \frac{V_{out}}{V_{in}} = -\frac{g_{m2}}{\frac{1}{r_{01}} + \frac{1}{r_{02}} + g_{m1}}$$

Above expression can also be written as,

$$A_v = -g_{m2}\left(r_{01} \| r_{02} \| \frac{1}{g_{m1}}\right)$$

❐❐❐

Ch 6 Frequency Response of BJT And MOFET

6.1 Introduction

Response of an amplifier to different frequency components of input signal is called frequency response of the amplifier. If input of an amplifier is sinusoidal signal, $v_{in} = V_m \sin(\omega t + \phi)$ and gain of amplifier is $A_v = A\angle\theta$ then output signal amplifier becomes,

$$v_o = AV_m \sin(\omega t + \phi + \theta)$$

The amplitude of output of amplifier depends as gain of amplifier & amplitude of input signal and phase angle of output depends on phase of input and phase angle of gain of amplifier. The frequency characteristics of an amplifier can be split in three regions called mid band, low frequency and high frequency. The mid band frequency region is frequency range of input signal for which gain of amplifier fairly remains constant. In low frequency region below mid band region, the gain of amplifier may decrease with decrease in frequency and amplifier may act as high pass circuit. In this region gain decreases with decrease in frequency and reaches zero at f = 0. At low frequency, the gain of amplifier is limited by coupling and bypass capacitances of the amplifier. The third region is high frequency region above the mid band region where gain reduces with increase in frequency. In sigh frequency region, an amplifier acts like a low pass filter. The gain of amplifier in high frequency region is limited by parasitic or junction capacitance of the device i.e. BJT or MOSFET. The amplifier response discussed so far is essentially small signal low frequency response where amplitude of input signal is very low in comparison of biasing signals of the amplifier. The analysis mainly focused on mid-band frequencies. The frequency range of an amplifier used to amplify a video signal is totally different from frequency range of amplifier used for amplification of audio signals. Similarly, if an amplifier is used to amplify a signal at power frequency (i.e. 50 Hz) then its response is different from an amplifier used to amplify a radio frequency signal. The amplification of a signal by an amplifier depends on many factors like amplitude of signal, frequency range of input signal, the characteristic of active device (r.e. BJT or FET) and external circuit components including biasing signals. Analysis of amplifier discussed so for ignored the effect of different capacitances of BJT and parameters of amplifier circuits. This chapter presents the effect of internal capacitances as well as circuit capacitances on response of the FET and BJT amplifiers. The voltage gain, current gain and power gain will be considered in decibel in order to caver wide range of frequencies and large variations.

(i) Voltage gain in dB, $A_{v,dB} = 20\log_{10} A_v = 20\log_{10}\frac{V_o}{V_{in}}$ (1)

(ii) Current gain in dB, $A_{i,dB} = 20\log_{10} A_i = 20\log_{10} \frac{I_o}{I_{in}}$ (2)

(iii) Power gain in dB

Power gain of amplifier,

$$A_p = \frac{P_o}{P_{in}} = \frac{V_o I_o}{V_{in} I_{in}} = A_v A_i \quad (3)$$

Power gain in dB, $A_{p,dB} = 10\log_{10} A_p = 20\log_{10} \frac{P_o}{P_{in}}$ (4)

$$\Rightarrow \quad A_{P,dB} = 20\log_{10} \frac{V_o I_o}{V_{in} I_{in}} = 20\log_{10} \frac{V_o}{V_{in}} + 20\log_{10} \frac{I_o}{I_{in}} \quad (5)$$

$$\Rightarrow \quad A_{P,dB} = A_{v,dB} + A_{i,dB} \quad (6)$$

Note : *i. Power gain is product of voltage gain and current gain but on dB scale power gain is sum of voltage gain in dB and current gain in dB.*

ii. In case of a RC coupled amplifier gain at low frequencies is decreased due to coupling and bypass capacitors and at high frequencies it is decreased due to internal parasitic capacitances and frequency dependence of gain. The frequency response of RC coupled amplifier is shown in Fig. 1.

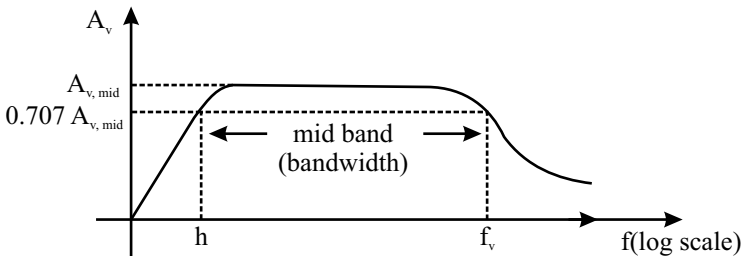


Fig. 1 Frequency response of RC coupling amplifier

iii. In case of a transformer coupled amplifiers, the gain a low frequencies is decreased because the coupling transformer at low reactance ($X_L = 2\pi fL$) at low frequencies and gain at high frequencies decreases due to increase in inter-tern capacitance of winding of transformer at high frequencies. The frequency response of transformer coupled amplifier is shown in Fig. 2.

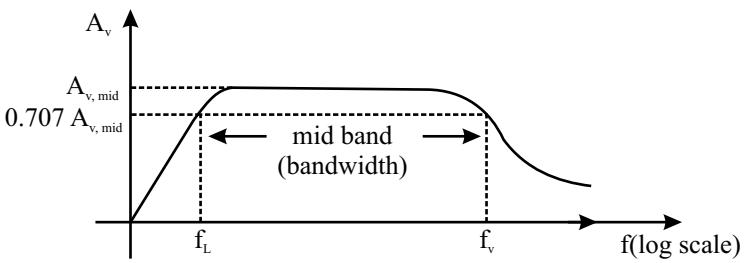


Fig. 2 Frequency response of transforms coupling amplifier

iv. In of case of a direct coupled amplifier with no coupling and bypass capacitors the low frequency response is almost flat and same as midband but gain at high frequencies decreases due to parasited internal capacitance of the device. The frequency response of direct coupled amplifier is shown in Fig. 3.

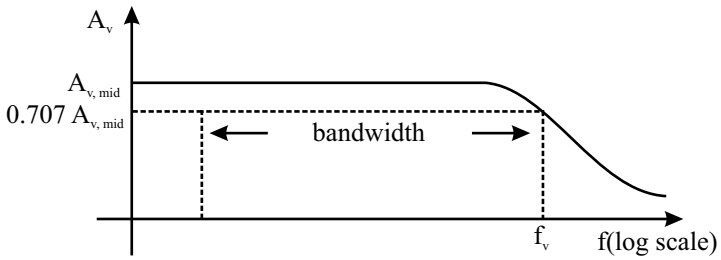


Fig.3 Frequency response of direct coupling amplifier

Therefore, the effect of coupling and bypass capacitors cannot be ignored at low frequencies . Similarly the response of the amplifier is limited by internal parasitic capacitances and frequency dependence of gain of BJT and FET.

Cut-Off Frequency :

The frequencies at which the gain of amplifier falls to $\frac{1}{\sqrt{2}}$ or 0.707 times of the mid band gain are called cut-off frequencies of the amplifier. The output power at cut off frequencies become half of output power at midband, so, cutoff frequencies are also called half power frequencies. At cut off frequency gain of amplifiers falls by $3\text{dB}\left(=20\log\frac{1}{\sqrt{2}}\right)$.

Band width (BW) :

The difference between upper and lower cut off frequencies of the amplifier is called band width of the amplifier.

$$BW = f_H - f_L \tag{7}$$

Where f_H is upper cutoff frequency and f_L is lower cutoff frequency of the amplifiers.

Note : *The frequency in frequency response of amplifiers is normally taken in log scale to cover wide range of frequencies.*

Note : *In common Emitter BJT amplifier and common source FET amplifier,*

(i) The output leads input by 180° at mid band frequencies i.e. between lower and upper cutoff frequencies.

(ii) The output leads input by angle more than 180° below lower cutoff frequencies.

(iii) The output leads input by angle less than 180° above upper cutoff frequencies.

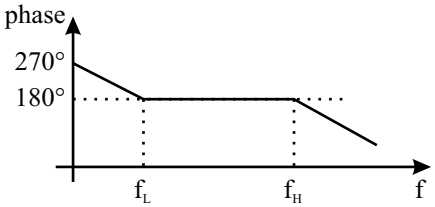


Fig.4 Phase Vs frequency response of common emitter BJT or common source FET amplifier

6.2 Frequency Response of High Pass RC Circuit

BJT and FET amplifiers behave like high pass RC circuit at low frequencies. If gain of active device is ignored then the amplifier can be modeled as high pass RC circuit as shown in Fig. 5.

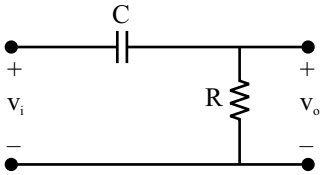


Fig. 5 High RC circuit

The output voltage of the circuit,

$$V_o = \frac{R}{R + \frac{1}{j\omega C}} \cdot V_i \tag{8}$$

Voltage transfer ratio or gain of the circuit,

$$\frac{V_o}{V_i} = \frac{1}{1 + \frac{1}{j\omega RC}} = \frac{1}{1 - j\frac{\omega_L}{\omega}} = \frac{1}{1 - j\frac{2\pi f_L}{2\pi f}} \tag{9}$$

$$\Rightarrow \quad \frac{V_o}{V_i} = \frac{1}{1 - j\frac{f_L}{f}} \tag{10}$$

Where $$f_L = \frac{1}{2\pi RC} \tag{11}$$

Magnitude of transfer function,

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}} \tag{12}$$

Phase angle, $$\angle(V_o / V_i) = \tan \text{—} \tag{13}$$

At $f = f_L$, $\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}}$ and $\angle(V_o / V_i) = 45^o$ (14)

The frequency f_L is called lower cutoff frequency of the circuit.

When frequency is varied from 0 to infinity the gain changes as given in table 1 below,

Table 1 : Gain Vs Frequency

f	A_v	$A_{v,dB} = 20 \log A_v$
0	0	–
f_L	$\frac{1}{\sqrt{2}}$	–3dB
∞	1	0dB

The variation in gain or voltage ratio of high pass RC circuit with frequency of input signal is shown in Fig. 6.

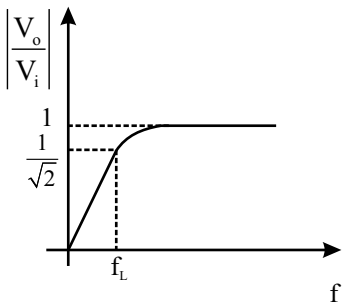


Fig. 6 Frequency response of high RC circuit

6.3 Low Frequency Response of BJT Amplifier

Consider potential divider bias common emitter BJT amplifier shown in Fig. 7.

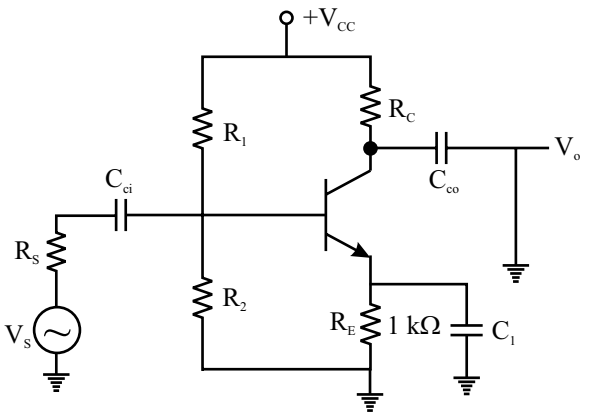


Fig. 7 Frequency response of BJT amplifier

The low frequency response of the amplifier is determined by coupling capacitors C_{ei}, C_{co} and emitter bypass capacitor C_E.

Case-I : Lower cutoff frequency in terms of C_{ci}

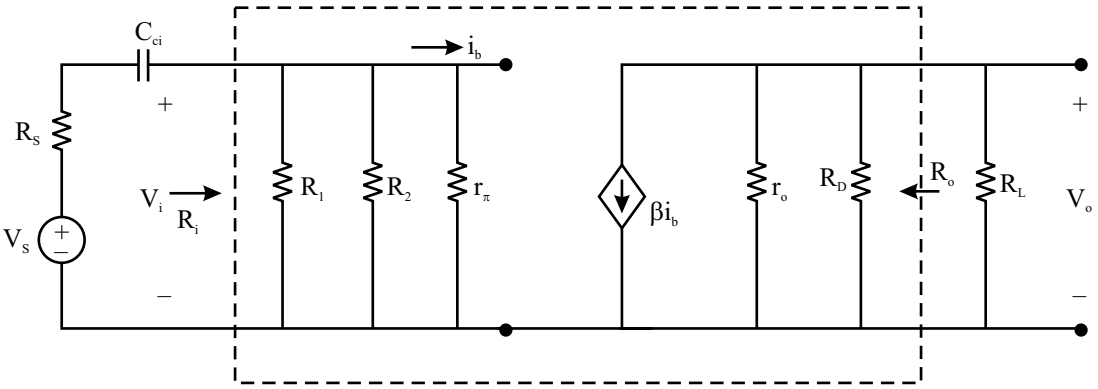
The effects of output coupling capacitor, C_{co} and emitter bypass capacitor, C_E on lower cutoff frequency are neglected for determination of lower cutoff frequency in terms of input coupling capacitor, C_{ci}. Therefore, C_{co} and C_E are replaced by short circuit for determination of effect of C_{ci}. The AC equivalent circuit of the amplifier will be as show in Fig. 8.

Input resistance of amplifier,

$$R_i = R_1 \parallel R_2 \parallel r_\pi \tag{15}$$

Output resistance of amplifier,

$$R_o = r_o \parallel R_D \tag{16}$$



BJT amplifier

Fig. 8 small signal equivalent consider effect of C_{ci}

$$\text{Input voltage of amplifier, } V_i = \frac{R_i}{R_i + R_s - jX_{ci}} \cdot V_s \tag{17}$$

$$\text{Where} \quad X_{ci} = \frac{1}{j\omega C_{ci}} \tag{18}$$

Output voltage of amplifier,

$$V_o = A_{vo} V_i \tag{19}$$

$$\text{Where} \quad A_{vo} = \frac{V_o}{V_i} = \text{Voltage gain neglecting } R_s \text{ \& } C_{ci} \tag{20}$$

$$\text{Here} \quad A_{vo} = \frac{\beta(r_o \parallel R_D)}{r_\pi} \tag{21}$$

$$\Rightarrow \quad V_o = A_{vo} \cdot \frac{R_i}{R_i + R_s - jX_{ci}} \tag{22}$$

$$\Rightarrow \quad A_{vs} = \frac{V_o}{V_s} = \frac{A_{vo} R_i}{R_i + R_s - jX_{ci}} = \frac{A_{vo} R_i}{(R_i + R_s)\left[1 - j\frac{X_{ci}}{R_i + R_s}\right]} \tag{23}$$

The combination of source resistance (R_s) and input resistance (R_i) of amplifier forms a high pass RC circuit as shown in Fig. 9.

Total resistance of RC circuit on input side of amplifier will be,

$$R = R_s + R_i \tag{24}$$

The lower cutoff frequency in terms of C_{ci} can be given by,

$$f_{Li} = \frac{1}{2\pi R C_{ci}} = \frac{1}{2\pi(R_s + R_i)C_{ci}} \tag{25}$$

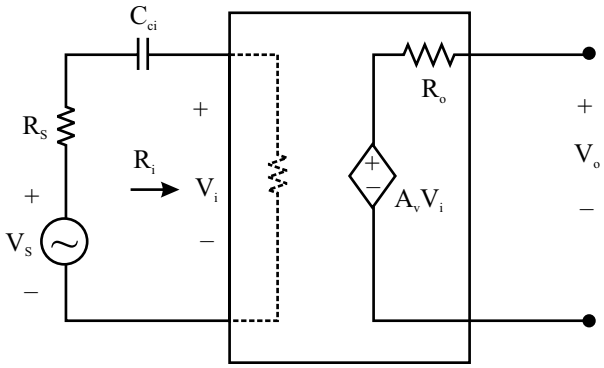


Fig. 9 BJT amplifier with input coupling capacitor behaving as low pass RC circuit on input side

Case-II : Lower cutoff frequency in terms of C_{co}

The effect of C_{co} on lower cutoff frequencies of the amplifier can be determined by neglecting the effects of C_{ci} and C_E. The equivalent circuit seen from output of the amplifier becomes as show in Fig. 10.

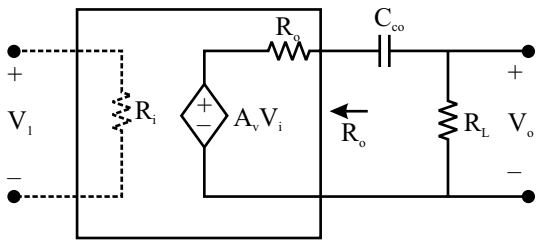


Fig. 10 BJT amplifier with output coupling capacitor behaving as low pass RC circuit on output side

The resistance seen across terminals of capacitor C_{co}, $R = R_o + R_L$ (26)

The lower cutoff frequency of the amplifier in terms of C_{co} becomes

$$f_{Lo} = \frac{1}{R\,C_{co}} = \frac{1}{2\pi(R_o + R_L)C_{co}} \tag{27}$$

Where, $R_o = r_o \parallel R_C$ = output resistance of amplifier. (28)

Case-III : Lower cutoff frequency in terms of C_E

The lower cutoff frequency of amplifier in terms of emitter bypass capacitor can be obtained by neglecting effect of C_{ci} and C_{co}. The amplifier circuit seen from terminals of emitter bypass capacitor becomes as shown in Fig. 11.

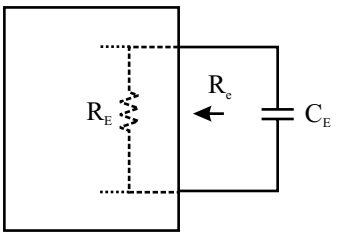


Fig. 11 BJT amplifier with emitter bypass capacitor behaving as low pass RC circuit

The lower cutoff frequency of amplifier in terms of C_E can be given by,

$$f_{LE} = \frac{1}{2\pi R_{eq}\,C_E} \tag{29}$$

Where R_{eq} is total resistance seen across terminals of C_E. Mathematically, R_e is given by

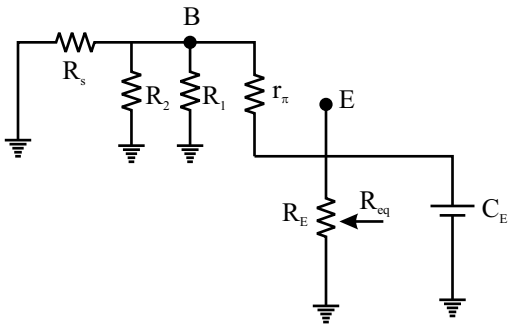


Fig. 12 Total resistance seen across terminals of emitter bypass capacitor

$$\boxed{R_e = R_E \parallel \left(\frac{R_s \parallel R_1 \parallel R_2 + r_\pi}{1+\beta} \right)} \tag{30}$$

Note : Here, the resistance of base circuit when seen from emitter side is reduced by a factor of (1 + β). Similarly, when resistance of emitter circuit is seen from base side, it is increased by a factor of (1 + β) So, resistance R_E appears as resistance (1 + β) R_E on input side of the circuit.

Note : i. C_{ci} C_{co} and C_E have effect on lower cutoff frequency only.

ii. The largest of lower cutoff frequencies, due to C_{ci} and C_{co} and C_E, is called dominant frequency.

iii. The dominant frequency is overall lower cutoff frequency of the amplifier.

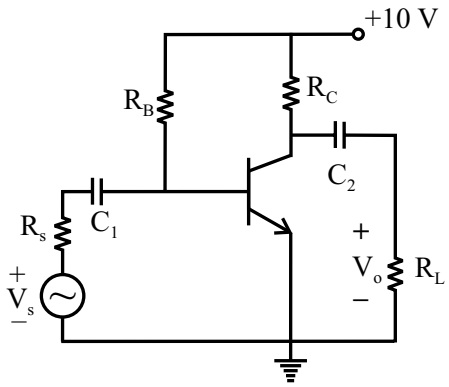
iv. At high frequencies the reactances offered by coupling & bypass capacitance are negligible and these capacitors can be replaced by short circuit.

Example 1

Common Data for Questions (i) and (ii) :

Consider the common emitter amplifier shown below with the following circuit parameters :

β = 100, g_m = 0.3861 A/V, $r_o = \infty$, r_π = 259 Ω, R_s =1 kΩ, R_B = 93 kΩ, R_C = 250 Ω, R_L = 1kΩ, $C_1 = \infty$ and C_2 = 4.7 μF.



(i) The resistance seen by the source V_s is

(a) 258 Ω (b) 1258 Ω

(c) 93 kΩ (d) ∞

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(ii) The lower cut-off frequency due to C_2 is

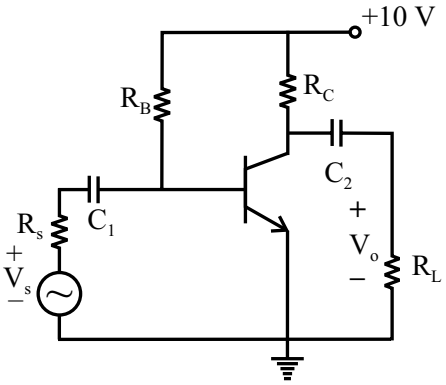
(a) 33.9 Hz (b) 27.1 Hz

(c) 13.6 Hz (d) 16.9 Hz

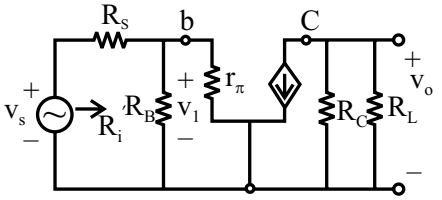
GATE(EC/2010/2M)

Solution :

(i) Ans.(b)



Equivalent circuit using π-model we have,



Given, $\beta = 100\ g_m = 0.3861,\ r_o = \infty$

$r_\pi = 259\Omega,\ R_s = 1\ K\Omega,\ R_B = 93\ K\Omega,$

$R_c = 250\ \Omega,\ R_L = 1\ K\Omega$

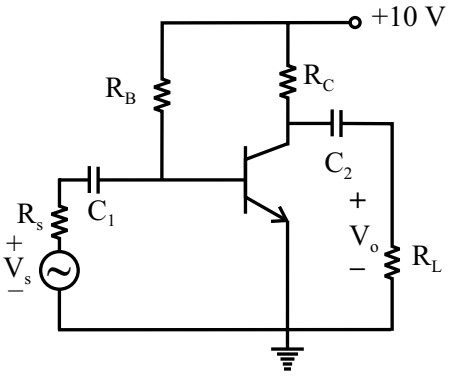
$C_1 = \infty,\ C_2 = 4.7\ \mu F$

Resistance seen by source,

$$R_i = R_s + \frac{R_B r_\pi}{r_\pi + R_B}$$

$$\Rightarrow \quad R_i = 1\times10 + \frac{93\times10 \times 259}{93\times10 + 259} = 1258\ \Omega$$

(ii) Ans.(b)



Lower cutoff frequency of BJT amplifier shown above, is given by,

$$f_L = \frac{1}{2\pi C_C (R_L + R_o)}$$

Where, $R_o = R_c \parallel r_o$

Given, $r_o = \infty$, $C_C = C_2 = 4.7\ \mu F$ and $R_L = 1\ K\Omega$

$\therefore$ $R_o = R_c = 250\ \Omega$

$\Rightarrow$ $$f_L = \frac{1}{2\pi C_2 (R_L + R_C)}$$

$\Rightarrow$ $$f_L = \frac{1}{2\pi \times 4.7 \times 10^{-6} (1000 + 250)}$$

$\Rightarrow$ $f_L = 27.09\ Hz$

6.4 Low Frequency Response of MOSFET Amplifier

The low frequency response of MOSFET is affected by coupling and bypass capacitors, similar to a BJT amplifier. The effects of input and output coupling capacitors and source bypass capacitor can be studied by considering the MOSFET based amplifier with as shown in Fig.13.

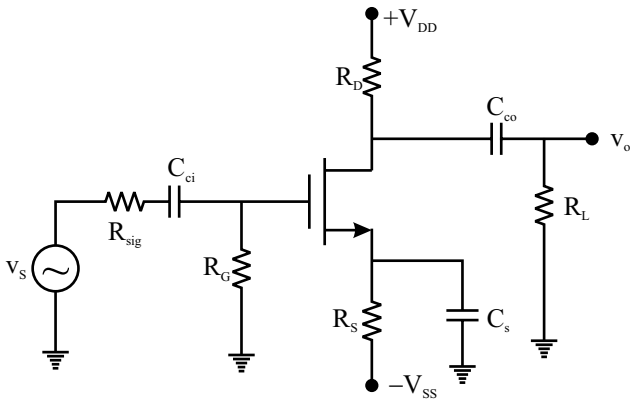


Fig. 13 Frequency response of MOSFET amplifier

Case-I : Effect of C_{ci}

The lower cutoff frequency due to C_{ci} is determined by replacing C_{co} and C_s by short circuit. The AC equivalent circuit with C_{ci} can be drawn as shown in Fig. 14.

The lower cutoff frequency of the amplifier in terms of C_{ci} is given by,

$$f_{Lci} = \frac{1}{2\pi (R_{sig} + R_i) C_{ci}} \quad (31)$$

Where $R_i = R_G$ = input resistance of amplifier. (32)

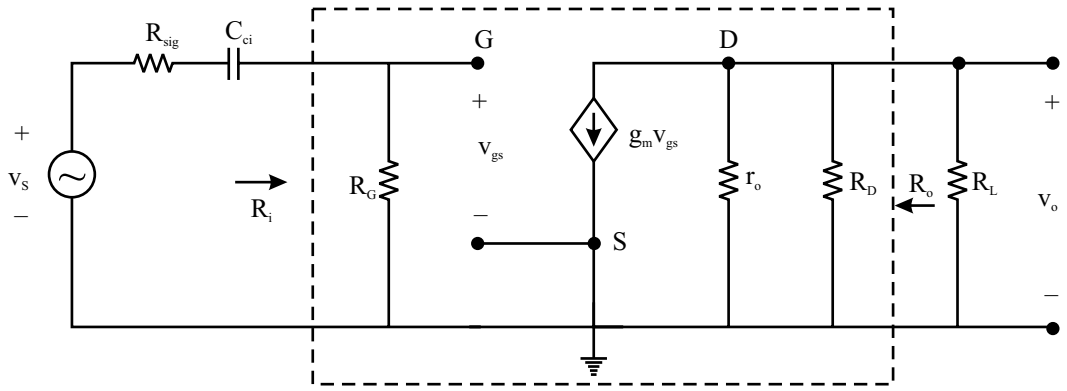


Fig. 14 MOSFET amplifier with input coupling capacitor behaving as low pass RC circuit on input side

Case-II : Lower cutoff frequency in terms of C_{co}

The effect of coupling capacitor C_{co} on low frequency response can be determined by replacing C_{ci} and C_s by short circuit. The equivalent circuit seen across terminals of C_{co} becomes as shown in Fig. 15.

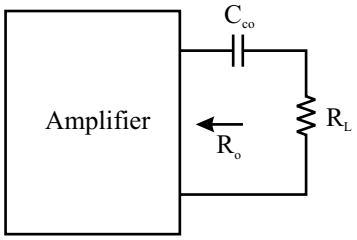


Fig. 15 MOSFET amplifier with output coupling capacitor behaving as low pass RC circuit on output side

Total resistance seen across the capacitor C_{co},

$$R = R_o + R_L \tag{33}$$

The lower cutoff frequency of the amplifier in terms of C_{co} is given by

$$f_{Lco} = \frac{1}{2\pi RC_{co}} = \frac{1}{2\pi(R_o + R_L)C_{co}} \tag{34}$$

Where $R_o = R_D \parallel r_o$ = output resistance of the amplifier (35)

Case-III : Lower cutoff frequency in terms of C_s

The lower cutoff frequency in terms of source bypass capacitor C_s can be determined by replacing C_{ci} and C_{co} by short circuit. Then, the equivalent circuit seen across terminals of C_s becomes as shown in Fig. 16.

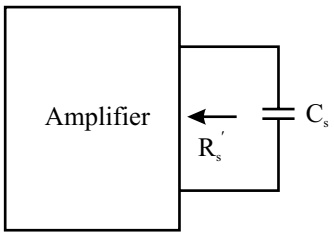


Fig. 16 MOSFET amplifier with source bypass capacitor behaving as low pass RC circuit

The lower cutoff frequency in terms of C_s can be given by

$$f_{Lcs} = \frac{1}{2\pi R_s' C_s} \tag{36}$$

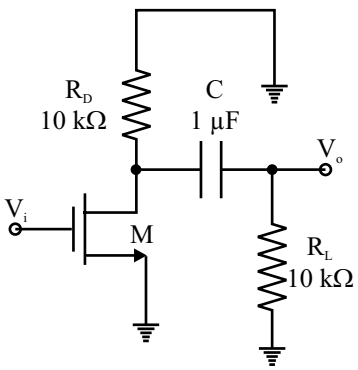
Where R'_s is effective resistance seen across terminals of C_s. The resistance R'_s can be determined from AC equivalent circuit of the amplifier.

Note : i. Highest of lower cutoff frequencies f_{Lci}, f_{Lco} and f_{Lcs}, determines the over all lower cutoff frequency and it is called dominant pole or frequency of the amplifier.

ii. At high frequencies the reactances offered by coupling and bypass capacitors become very small and capacitors behave like short circuit. So, the effect of coupling and bypass capacitors can be neglected at high frequencies.

Example 2

The ac schematic of an NMOS common source stage is shown in the figure below, where part of the biasing circuit has been omitted for simplicity. For the n-channel MOSFET M, the transconductance g_m = 1 mA/V and body effect and channel length modulation effect are to be neglected. The lower cutoff frequency in Hz of the circuit is approximately at



(a) 8 (b) 32

(c) 50 (d) 200

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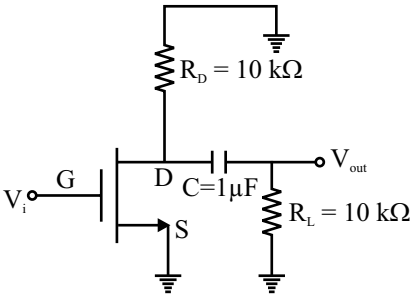
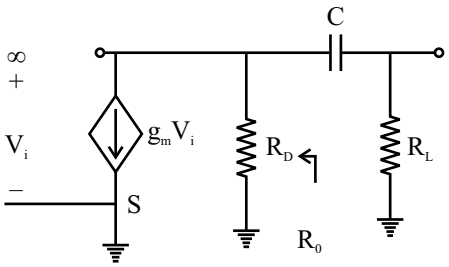
Solution : Ans.(a)



Given, transconductance of MOSFET,

$$g_m = 1 \text{ mA/V}$$

Replacing MOSFET by its small signal model the equivalent circuit of amplifier can be drawn as under,



Output resistance of above circuit is obtained by setting $V_i = 0$,

So output resistance,

$$R_o = R_D$$

Resistance seen across capacitor,

$$R = R_o + R_L = R_D + R_L$$

Lower cut off frequency of amplifier can be given as,

$$f_L = \frac{1}{2\pi C(R_D + R_L)}$$

From given circuit, C = 1 μF, R_D = 10 kΩ,

$$R_L = 10 \text{ kΩ}$$

$$\Rightarrow \quad f_L = \frac{1}{2\pi \times 10^{-6}(10+10)\times 10^3} = 8 \text{ Hz}$$

6.5 Miller Effect

Consider an amplifier with a feed back impedance ,Z_f, is connected between input and output terminals as show in Fig. 17.

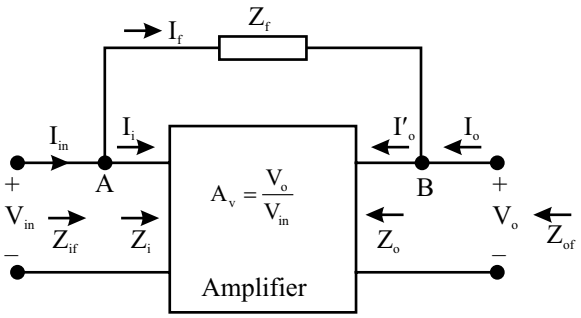


Fig. 17 Amplifier with feedback impedance

Case-I : Effect of Z_f on input impedance of Amplifier

Applying KCL at node 'A', we have,

$$I_{in} = I_f + I_i$$

$$\Rightarrow \quad \frac{V_{in}}{Z_{if}} = \frac{V_{in} - V_o}{Z_f} + \frac{V_{in}}{Z_i} \tag{37}$$

$$\Rightarrow \quad \frac{1}{Z_{if}} = \frac{1 - \frac{V_o}{V_{in}}}{Z_f} + \frac{1}{Z_i} \tag{38}$$

$$\Rightarrow \quad \frac{1}{Z_{if}} = \frac{1 - A_v}{Z_f} + \frac{1}{Z_i} \tag{39}$$

$$\Rightarrow \quad \frac{1}{Z_{if}} = \frac{1}{\frac{Z_f}{1 - A_v}} + \frac{1}{Z_i} \tag{40}$$

$$\Rightarrow \quad Z_{if} = \left(\frac{Z_f}{1 - A_v}\right) \| Z_i \tag{41}$$

Thus, the feedback impedance appears as $\frac{Z_f}{1 - A_v}$ when it is seen from input terminals.

Case-II : Effect of Z_f on output impedance of amplifier

Apply KCL at node 'B' , we have,

$$I_o = I_f + I'_o \tag{42}$$

$$\Rightarrow \quad \frac{V_o}{Z_{of}} = \frac{V_o - V_{in}}{Z_f} + \frac{V_o}{Z_o} \tag{43}$$

$$\Rightarrow \quad \frac{1}{Z_{of}} = \frac{1-\frac{V_{in}}{V_o}}{Z_f} + \frac{1}{Z_o} \tag{44}$$

$$\Rightarrow \quad \frac{1}{Z_{of}} = \frac{1-\frac{1}{A_v}}{Z_f} + \frac{1}{Z_o} \tag{45}$$

$$\Rightarrow \quad \frac{1}{Z_{of}} = \frac{1}{\frac{Z_f}{1-\frac{1}{A_v}}} + \frac{1}{Z_o} \tag{46}$$

$$\Rightarrow \quad \frac{1}{Z_{of}} = Z_o \left\| \left(\frac{Z_f}{1-\frac{1}{A_v}} \right) \right. \tag{47}$$

Thus, the feedback impedance appears as $\frac{Z_f}{1-\frac{1}{A_v}}$ in parallel to output impedance of amplifier when it is seen from the output terminals of the amplifier.

It is observed from above two cases that an impedance Z_f connected in feedback arrangement of amplifier can be transferred an as shunt impedance of value $\frac{Z_f}{1-A_v}$ on input terminals and as a shunt impedance of value $\frac{Z_f}{1-\frac{1}{A_v}}$ on output terminals as shown in Fig.18 Where A_v is voltage gain of amplifier without feedback. This effect is known as Miller's effect.

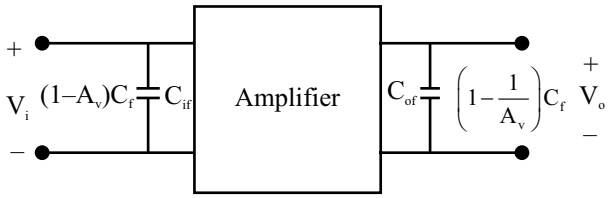


Fig. 18 Feedback impedances transfered to input and output side of amplifier

6.5.1 Miller Effect Capacitances

At high frequencies the effect of coupling and bypass capacitances becomes negligible due to

decreased reactances offered by these capacitors. However, the effect of small parasitic or inter electrode capacitances become predominant. Consider an amplifier in which parasitic capacitances (C_f) appear in feedback path between input and output terminals as shown in Fig.19.

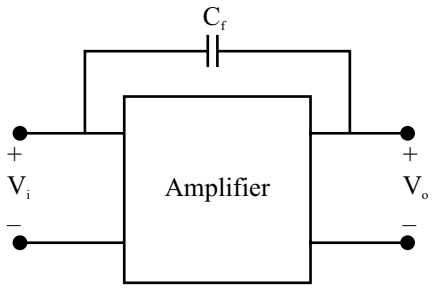


Fig. 19 Miller effect capacitances

The Miller Effect can be used to study effect of the parasite capacitance appearing between input and output terminals. According to millers effect, feedback impedance transfered to input side is given by,

$$Z_{if} = \frac{Z_f}{1 - A_v} \tag{48}$$

For capacitive elements, $Z_f = \frac{1}{j\omega C_f}$ and $Z_{if} = \frac{1}{j\omega C_{if}}$ (49)

$$\therefore \quad \frac{1}{j\omega C_{if}} = \frac{1}{j\omega C_i (1 - A_v)} \tag{50}$$

$$\Rightarrow \quad \boxed{C_{if} = (1 - A_v) C_i} \tag{51}$$

The capacitance C_{IF} is called Millers capacitance and it is also represented by C_M.

Similarly, th feedback impedance transfered to output terminals is given by,

$$Z_{of} = \frac{Z_f}{1 - \frac{1}{A_v}} \tag{52}$$

$$\Rightarrow \quad \frac{1}{j\omega C_{of}} = \frac{1}{j\omega C_f \left(1 - \frac{1}{A_v}\right)} \tag{53}$$

$$\Rightarrow \quad C_{of} = C_f \left(1 - \frac{1}{A_v}\right) \tag{54}$$

6.5.2 Dual of Miller Theorem :

According to dual of miller theorem an impedance, Z_f, connected in shunt branch series feedback arrangement of amplifier can be transferred as series impedance of value $(1 - A_i)Z_f$, on input terminals and as a series impedance of value $\left(1-\frac{1}{A_i}\right)Z_f$ on output terminals as shown in Fig.20. Where A_i represents current gain of the amplifier without feedback.

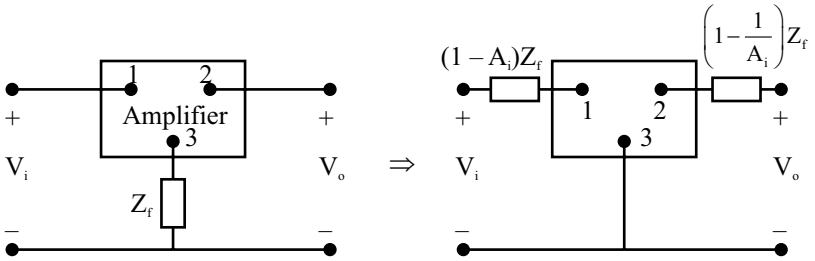


Fig. 20 Dual of Miller's effect

6.6 Frequency Response of Low Pass RC Circuit

At high frequencies, the effect of coupling and bypass capacitors become negligible and effect of parasitic capacitance of BJT and MOSFET become dominant. The BJT and MOSFET amplifiers can be modelled as low pass RC circuit as shown in Fig. 21 at high frequencies.

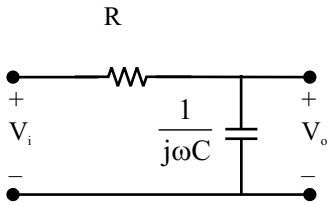


Fig. 21 Low pass RC circuit

Output voltage of the circuit,

$$V_o = \frac{1/j\omega C}{R + \frac{1}{j\omega C}} \times V_i \tag{55}$$

The voltage transfer function of the circuit,

$$\Rightarrow \quad \frac{V_o}{V_i} = \frac{1}{1+\frac{j\omega}{1/RC}} = \frac{1}{1+\frac{j\omega}{\omega_H}} = \frac{1}{1+\frac{j2\pi f}{2\pi f_H}} = \frac{1}{1+j\frac{f}{f_H}} \tag{56}$$

Where, $\omega_H = 2\pi f_H$ (57)

and $f_H = \frac{1}{2\pi RC}$ = higher cutoff frequency of the circuit. (58)

Magnitude, $$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} \quad (59)$$

Phase angle, $$\angle\left(\frac{V_o}{V_i}\right) = -\tan^{-1}\frac{f}{f_H} \quad (60)$$

The magnitude Vs frequency curve or frequency reponse of low pass RC circuit can be drawn as shown in Fig.22.

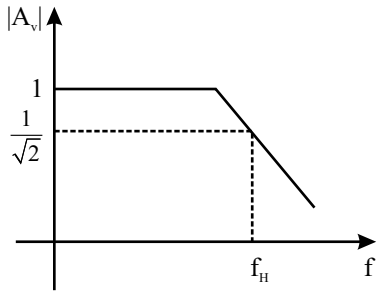


Fig. 22 Frequency response of low pass RC circuit.

At $f = f_H$, $$\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}} \quad (61)$$

The magnitude in dB at $f = f_H$,

$$\left|\frac{V_o}{V_i}\right|_{dB} = 20\log_{10}\left(\frac{1}{\sqrt{2}}\right) = -3 \text{ dB}$$

Note : The magnitude of transfer function of low pass filter becomes –3dB at cutoff frequency due to which cutoff frequency is some times called as 3dB cut off frequency.

6.7 High Frequency Response of BJT Amplifier

6.7.1 Hybrid π-model of BJT

Hybrid π-Model of BJT can be used for high frequency analysis of a BJT amplifier fig. shows the hybrid π-model of CE configuration of BJT. The terminal B′ is not accessible but a fictitious point at base.

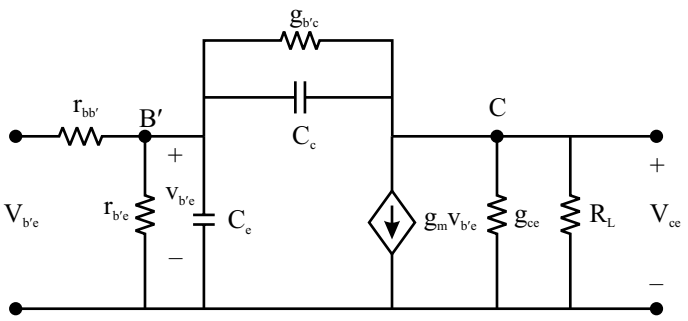


Fig. 23 Hybrid π-model of BJT

- In hybrid π-model of the BJT shown above, the resistance $r_{bb'}$ is called base spreading resistance.
- The resistance $r_{b'e}$ is reponsible for change in base current due to increased recombination rate with change in base-emitter voltage $v_{b'e}$.
- The capacitor $C_{b'e}$ or C_e or C_π represent emitter junction diffusion capacitance.
- The base width modulation effect or early effect is taken into account by connecting a conductance $g_{b'c}$ between base terminal B′ and collector terminal 'C'.
- The conductance g_{ce} represents output conductance of BJT
- The capacitance $C_{b'c}$ or C_c or C_μ represents the capacitance of collector junction.

Note : i. All the parameters of hybrid π-model can be determined using h-parameters of BJT
ii. Hybrid-π model is applicable for frequencies upto proximately $f_T/3$. Where f_T is unity gain frequency.

6.7.2 Conductances and Resistances of Hybrid π-model of BJT

1. Transconductance g_m

The transconductance of BJT is defined by,

$$g_m = \left.\frac{\partial I_c}{\partial V_{b'e}}\right|_{V_{CE}=\text{fixed}} \tag{62}$$

The transconductance in terms of gains of BJT and DC bias collector current is given by,

$$g_m = \frac{\alpha}{r_e} = \frac{\beta}{r_\pi} = \frac{|I_C|}{V_T} \tag{63}$$

Where, V_T is thermal voltage. The thermal voltage at any temperature T (in Kelvin) is given by,

$$V_T = \frac{T}{11600} \tag{64}$$

2. Input conductance, $g_{b'e}$

The collector current of BJT,

$$I_c = g_m V_{b'e} = g_m I_b r_{b'e} \tag{65}$$

$$\Rightarrow \quad g_m r_{b'e} = \frac{I_c}{I_b} = h_{fe} \tag{66}$$

$$\Rightarrow \quad \boxed{h_{fe} = g_m\, r_{b'e}} \tag{67}$$

$$\Rightarrow \quad \boxed{g_{b'e} = \frac{1}{r_{b'e}} = \frac{g_m}{h_{fe}} = \frac{|I_C|}{h_{fe}\, V_T}} \tag{68}$$

Note : The resistance $r_{b'e}$ is directly proportional to temperature and inversely proportional to collector bias current.

3. Feedback conductance, $g_{b'e}$

From hybrid π-model of BJT,

$$h_{re} = \left.\frac{V_{b'e}}{V_{ce}}\right|_{I_b=0} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \tag{69}$$

or $$r_{b'e}(1 - h_{re}) = h_{re} r_{b'c}$$

The reverse voltage gain (h_{re}) for CE configuration of BJT, $h_{re} << 1$

$$\therefore \quad r_{b'e} \approx h_{re}\, r_{b'e} \tag{70}$$

$$\Rightarrow \quad \boxed{g_{b'c} = \frac{h_{re}}{r_{b'e}} = h_{re} \cdot g_{b'e}} \tag{71}$$

4. Base spreading resistance, $r_{b'b}$

Base spreading resistance is a lumped resistance between external base terminal and terminal B′ of hybrid π-model. The input resistance of BJT with output terminal shorted is h_{ie}.

From the hybrid π-model of BJT,

$$h_{ie} = r_{bb'} + r_{b'e} \tag{72}$$

$$\Rightarrow \quad r_{bb'} = h_{ie} - r_{b'e} = h_{ie} - \frac{h_{fe}\, V_T}{|I_C|} \tag{73}$$

5. Output conductance, g_{ce}

Output conductance is given by

$$g_{ce} = h_{oe} - g_m\, h_{re} \tag{74}$$

6.7.3 Capacitances of BJT in Hybrid π-Model

I. Base-Emitter Diffusion Capacitance of BJT

In amplifier applications, the emitter junction of BJT is forward biased and collector junction is reverse biased. The minority carriers (i.e. electrons for npn & hales for pnp) carriers are diffused from emitter region to base region through emitter-base junction. The width of base region of BJT is very small as compared as diffusion length of minority carries in base. So, the concentration of holes in base region of pnp transistor varies almost linearly in the base region as shown in Fig. 24.

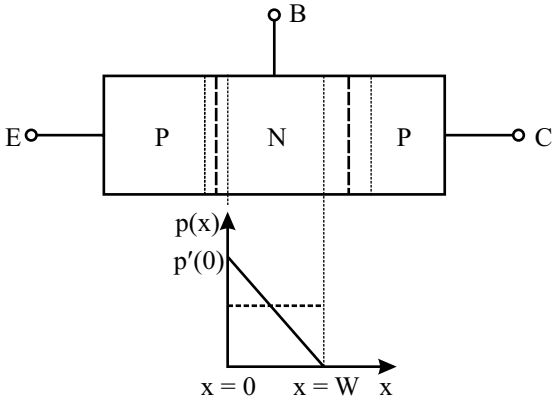


Fig. 24 Variation of holes concentration in base region of pnp transistor

For linear decrease in minority carrier concentration, the average concentration of excess minority carriers stored in base region is p′(0)/2. If A is cross section of emitter function, W is width of base region then charge of excess minority carriers stored in base region can be given by,

$$Q_B = AW \times \frac{p'(0)}{2} \times q \tag{75}$$

The diffusion current in base region due to minority carriers holes in base region of pnp transistor can be given by,

$$I = - AqD_{pB} \cdot \frac{dp}{dx} = -AqD_{pB} \cdot \left(\frac{p'(0) - 0}{0 - W} \right) = AqD_{pB} \cdot \frac{p'(0)}{W} \tag{76}$$

Where D_{pB} is diffusion constant of holes in the base region. The current I is almost equal to emitter current of BJT.

$$\Rightarrow \quad p'(0) = \frac{W I_E}{AqD_{pB}} \tag{77}$$

Putting above expression of p′(0) in equation (75), we have,

$$Q_B = \frac{I_E W^2}{2D_{pB}} \tag{78}$$

The static emitter diffusion capacitance due to rate of change of excess minority carrier in base region can be given by,

$$C_{De} = \frac{dQ_B}{dV_{BE}} = \frac{W^2}{2D_{pB}} \cdot \frac{dI_E}{dV_{BE}} \tag{79}$$

For BJT, $$\frac{dI_E}{dV_{BE}} = \frac{1}{r_e} = \frac{I_E}{V_T} \quad (80)$$

$$\therefore \quad \boxed{C_{De} = \frac{W^2}{2D_{pB}} \cdot \frac{I_E}{V_T} = \frac{W^2}{2D_{pB}} \cdot \frac{1}{r_e}} \quad (81)$$

Emitter current of BJT, $I_E \approx I_C$ (82)

$$\therefore \quad \boxed{C_{De} = g_m \frac{W^2}{2D_{pB}}} \quad (83)$$

Note : i. Diffusion capacitance is proportional emitter current

ii. For BJT, $D_{pB} = \mu V_T$

Here $\mu \propto T^{-m}$

$\therefore$ $D_{pB} \propto T^{-m}$

$\therefore$ $C_{De} \propto T^{+m}$

So C_{De} increases as temperatures increases and the increase in C_{De} is more for Si than Ge

iii. Diffusion capacitance of BJT for sinusoidal signals is 2/3rd of static capacitance

II. Base-Emitter Junction Capacitance of BJT

The base-emitter junction of a BJT amplifier is forward biased so the capacitance of base-emitter junction is similar to capacitance offered by the junction of a forward biased pn junction diode. The junction capacitance of emitter junction can be given by,

$$C_{je} = \frac{\varepsilon A}{W_e} \quad (84)$$

Where W_e is width of emitter junction. The width of forward biased emitter junction can be given by,

$$W_e = \sqrt{\frac{2\varepsilon}{q} \cdot \left[\frac{1}{N_D} + \frac{1}{N_A}\right](V_{oe} - V_{BE})} \quad (85)$$

Where, $V_{BE} \rightarrow$ For emitter junction forward bias voltage.

$V_{oe} \rightarrow$ Built-in potential of emitter junction.

$N_D \rightarrow$ The concentration of donor impurity

$N_A \rightarrow$ Concentration of acceptor impurity

III. Collector-Base Junction Capacitance of BJT (C_c or C_μ)

The collector-base junction of BJT is reverse biased and its capacitance is similarity capacitance offered by a reverse biased p-n junction diode. The collector junction capacitance of BJT can be given by,

$$C_c = \frac{\varepsilon A}{W_c} \tag{86}$$

Where W_c is width of reverse biased collector junction. The width of reverse biased collector junction is given by

$$W_c = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\left(V_{oc}+V_{CB}\right)} \tag{87}$$

Where V_{CB} is reverse biased collector junction voltage and V_{oc} is built in potential of collection junction.

Note : i. Typical value Hybrid parameters and their variations with I_C, V_{CE} and Temperature (T) of

Parameter	Value	Variation with increase in $\lvert I_C \rvert$	Variation with increase in $\lvert V_{CE} \rvert$	Variation with increase in T
g_m	50 m A / V	$g_m \propto \lvert I_C \rvert$	Independent	$g_m \propto 1/T_C$
$r_{bb'}$	100 Ω	decreases	–	increases
r_{ce}	80 K	–	–	–
$r_{b'e}$	1 K	$r_{b'e} \propto 1/\lvert I_C \rvert$	increases	increases
$r_{b'c}$	4 M	–	–	–
r_{ce}	80 K	–	–	–
C_c	3 pF	Independent	decreases	Independent
C_e	100 pF	$C_e \propto \lvert I_C \rvert$	decreases	–

ii. In some literature C_c is denoted by C_μ, C_e is denoted by C_π and $r_{b'e}$ is denoted by r_π.

6.7.4 Short Circuit Current Gain of BJT Amplifier

The equivalent circuit of hybrid-π model under short circuited condition becomes as shown in Fig. 25.

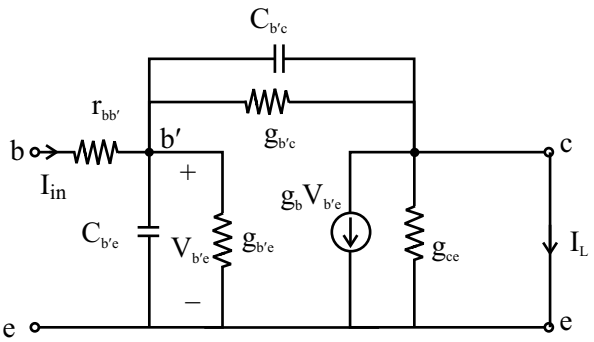


Fig. 25 High frequency equivalent circuit with output short circuited

Above circuit can be redrawn as under,

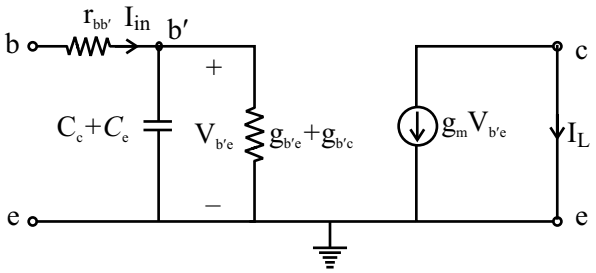


Fig. 26 Simplified high frequency equivalent circuit with output short circuited

Shorted load current, $$I_L = -g_m V_{b'e} \quad (88)$$

From input side of the circuit,

$$V_{b'e} = I_{in} \times \frac{1}{g_{b'e} + g_{b'c} + j\omega(C_c + C_e)} \quad (89)$$

Putting above relation in equation (88), we have,

$$I_L = -g_m \times \frac{1}{g_{b'e} + g_{b'c} + j\omega(C_c + C_e)} . I_{in} \quad (90)$$

Short circuited current gain,

$$A_{Is} = \frac{I_L}{I_{in}} = \frac{-g_m}{g_{b'e} + g_{b'c} + j\omega(C_c + C_e)} \quad (91)$$

Since collector junction is reversed biased, $r_{b'c}$ is large and $g_{b'c}$ is negligible.

$$\therefore \quad g_{b'e} + g_{b'c} \approx g_{b'e} \quad (92)$$

$$\Rightarrow \quad A_{Is} = \frac{-g_m}{g_{b'e} + j\omega(C_c + C_e)} \quad (93)$$

From equation (68), $$g_{b'e} = \frac{g_m}{h_{fe}} \quad (94)$$

$$\Rightarrow \quad A_{Is} = \frac{-h_{fe}}{1 + \frac{j\omega(C_c + C_e)}{g_m} h_{fe}} \quad (95)$$

$$\Rightarrow \quad A_{Is} = \frac{-h_{fe}}{1+\frac{j\omega}{\omega_\beta}} \tag{96}$$

where, $$\omega_\beta = \frac{g_m}{h_{fe}(C_c + C_e)} \tag{97}$$

$$\Rightarrow \quad \boxed{f_\beta = \frac{g_m}{2\pi h_{fe}(C_c + C_e)}} \tag{98}$$

where, f_β is also called β or upper 3dB cut-off frequency of amplifier.

$$\Rightarrow \quad |A_{Is}| = \frac{h_{fe}}{\sqrt{1+\left(\frac{f}{f_\beta}\right)^2}} \tag{99}$$

Note : i. In case of high frequency response of single CE BJT amplifier, at upper cutoff frqueny, $f = f_\beta$, the magnitude of gain becomes 0.707 h_{fe} and phase angle of gain becomes 135°.

ii. In case of low frequency response of single CE BJT amplifier, at lower cutoff frequency, $f = f_L$, the magnitude of gain becomes 0.707 h_{fe} and phase angle of gain becomes 225°.

Short circuit unity current gain cut off frequency (f_T):

At $f = f_T$, $$A_{Is} = 1 \tag{100}$$

$$\Rightarrow \quad 1 = \frac{h_{fe}}{\sqrt{1+\left(\frac{f_T}{f_\beta}\right)^2}} \tag{101}$$

$$\Rightarrow \quad \left(\frac{f_T}{f_\beta}\right)^2 = h_{fe}^2 - 1 \tag{102}$$

$$\Rightarrow \quad f_T = \sqrt{h_{fe}^2 - 1}\, f_\beta \tag{103}$$

Since, h_{fe} is large so $h_{fe}^2 >> 1$

$$\Rightarrow \quad \boxed{f_T = h_{fe}\, f_\beta \approx \beta f_\beta} \tag{104}$$

Here the frequencies up to f_β represent bandwidth of the amplifier and because of above relation f_T is represents the short circuit current gain-bandwidth product of the amplifier.

$$\Rightarrow \quad f_T = h_{fe} \times \frac{g_m}{2\pi h_{fe}(C_c + C_e)} \tag{105}$$

$$\Rightarrow \qquad \boxed{f_T = \frac{g_m}{2\pi(C_c + C_e)}} \tag{106}$$

Since, $C_e >> C_c$, therefore,

$$f_T = \frac{g_m}{2\pi C_e} \tag{107}$$

There is one more cut off frequency defined for an amplifier called α-cutoff frequency. The α-cutoff frequency of an amplifier is given by,

$$\boxed{f_\alpha = (1+\beta) f_\beta} \tag{108}$$

Gain magnitude Plot of Short Circuit Current Gain :

On decibel scale the magnitude of current can be represented by,

$$|A_I|_{dB} = 20 \log |A_I| \tag{109}$$

At low frequencies, $f << f_\beta$, $1 + \left(\frac{f}{f_\beta}\right)^2 \approx 1$, $|A_I| = h_{fe}$ and $|A_I|_{dB} = 20 \log h_{fe}$ (110)

At low frequencies, $f = f_\beta$, $1 + \left(\frac{f}{f_\beta}\right)^2 \approx 2$ $|A_I| = h_{fe}/\sqrt{2}$ and $|A_I|_{dB} = 20 \log h_{fe} - 3dB$ (111)

At very high frequencies, $f >> f_\beta$, $1 + \left(\frac{f}{f_\beta}\right)^2 \approx \left(\frac{f}{f_\beta}\right)^2$ (112)

$$\therefore \qquad |A_{Is}| \approx \frac{h_{fe} f_\beta}{f} \text{ and } |A_I|_{dB} = 20 \log h_{fe} f_\beta - 20 \log f \tag{113}$$

Using above relations, the gain (dB) vs. frequency (log f) can be drawn as shown in Fig.27.

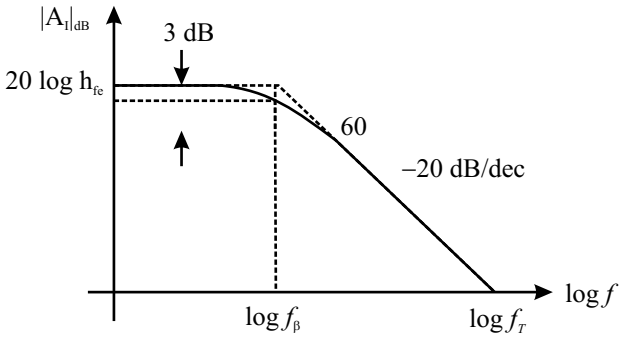


Fig. 27 Current gain Vs frequency plot of short circuit CE amplifier

Experimental Measurement of f_T :

At very high frequencies, $f >> f_\beta$, $1+\left(\frac{f}{f_\beta}\right)^2 \approx \left(\frac{f}{f_\beta}\right)^2$ (114)

$$\therefore \quad |A_{Is}| \approx \frac{h_{fe} f_\beta}{f} \tag{115}$$

$$\Rightarrow \quad |A_{Is}| f \approx h_{fe} f_\beta \approx f_T \tag{116}$$

If at any frequency $f = f_1$ gain is $|A_{Is1}|$ then $f_T = A_{Is1} f_1$ (117)

This measured value of f_T can be and to determine the emitter junction capacitance by using the relation,

$$C_e = \frac{g_m}{2\pi f_T} \tag{118}$$

Variation of f_T with collector current :

The value of parameter fT of BJT depends on operating condition of BJT. The variation of fT with collector current of BJT is shown in Fig. 28.

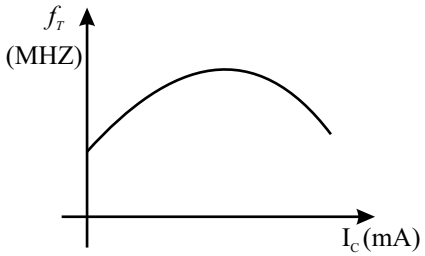


Fig. 28 Variation of parameter f_T with collector current

Note : *i. BJT behaves like low pass filter at high frequencies and high pass filter at low frequencies.*

ii. In RC coupled amplifier the Low frequency response of BJT is limited by coupling capacitors and bypass capacitors, in transformer coupled amplifiers it is limited by transformer turn to turn capacitance.

iii. Direct coupled amplifier has good low frequency response than RC coupled and transformer coupled amplifiers. It can amplify very low frequency signals.

iv. High frequency response of BJT amplifiers is limited by junction and parasitic capacitances.

v. For low frequency or small signal analysis, the coupling and bypass capacitors are included in the circuit and junction and parasitic capacitances are open circuited.

vi. For high frequency analysis, the coupling and bypass capacitors are replaced by short circuit and junction and parasitic capacitances are included into circuit.

vii. At mid band frequencies the coupling and bypass capacitors are replaced by short circuit and junction and parasitic capacitances are replaced by open circuit.

Note : High frequency response of BJT can be impoved by adopting non-uniform doping or graded doping profile in base of BJT in stead of uniform doping. The transistor with uniform base doping is called diffusion transistor and transistor with graded or non-uniform base doping is called graded

transistor. The graded base BJTs exhibit better high frequency response characteristic as compared to their uniform base counterparts because there exists a built-in electric field in the base region of the graded base BJT gives additional drift velocity to minority carries in base reason resulting reduction of switching time and hence giving better high frequency response.

Example 3

An npn transistor has a beta cutoff frequency f_β of 1 MHz, and common emitter short circuit low-frequency current gain β_0 of 200. It unity gain frequency f_T and the alpha cutoff frequency f_α respectively are

(a) 200 MHz, 201 MHz (b) 200 MHz, 199MHz

(c) 199 MHz, 200 MHz (d) 201 MHz, 200 MHz

GATE(EC/1996/2M)

Solution : Ans.(a)

The unity gain frequency in terms of β-cutoff frequency is given by

$$f_T = h_{fe} f_\beta = \beta f_\beta$$

f_β = β-cutoff frequency of amplifier.

Given, $\beta = 200, f_\beta = 1MH$

$\Rightarrow$ $f_T = 200 \times 1 = 200$ MHz

The alpha cutoff frequency of BJT is given by,

$$f_\beta = (1-\alpha) f_\alpha$$

$$f_\alpha = \frac{f_\beta}{1-\alpha}$$

where, $\alpha = \dfrac{\beta}{1+\beta}$

$\Rightarrow$ $f_\alpha = (1+\beta) f_\beta$

$\Rightarrow$ $f_\alpha = (1 + 200) \times 1$ MHz

$\Rightarrow$ $f_\alpha = 201$ MHz

Example 4

An npn transistor (with $C_\pi = 0.3$ pF) has a unity - gain cutoff frequency f_T of 400 MHz at a dc bias current $I_c = 1$mA. The value of its C_μ (in pF) is approximately ($V_T = 26$ mV)

(a) 15 (b) 30

(c) 50 (d) 96

GATE(EC/1999/2M)

Solution : Ans.(a)

The unity gain frequency of CE mode BJT amplifier is given by,

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

where, $g_m = \dfrac{I_c}{|V_T|}$ & $|V_T|$ is thermal voltage

Given, $f_T = 400$ MHz,

$C_\pi = 0.3$pF,

$I_c = 1$ mA

and $V_T = 26$ mV

$$\Rightarrow \quad f_T = \frac{I_c}{2\pi V_T (C_\pi + C_\mu)}$$

$$\Rightarrow \quad f_T = \frac{1}{2\pi V_T (0.3\times 10^{-12} + C_\mu)}$$

$$\Rightarrow \quad 400\times 10^6 = \frac{1}{2\pi \times 26 (0.3\times 10^{-12} + C_\mu)}$$

$$\Rightarrow \quad C_\mu = \frac{1}{2\pi \times 26 \times 400 \times 10^6} - 0.3\times 10^{-12} = 15 \text{ pF}$$

6.7.5 Frequency Response of BJT Amplifier with Resistive Load

Consider hybrid-π equivalents circuit of BJT with load resistance as shown in Fig. 29.

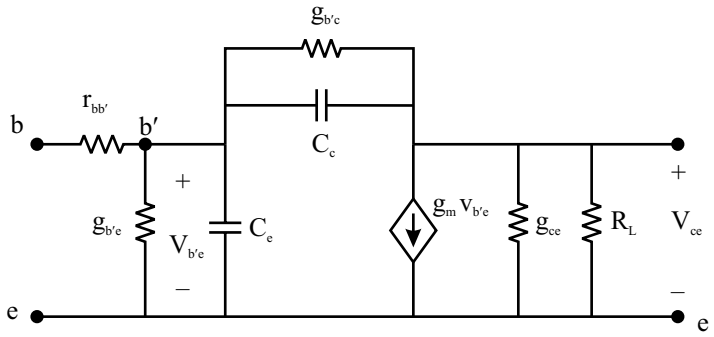


Fig. 29 High frequency model of CE BJT amplifier with resistive load

The conductance $g_{b'c}$ and capacitance C_c from feedback path can be transferred to input and output terminals by using Mitter's Theorem as under,

$$g_{b'ci} = (1 - A_v) g_{b'c} \quad \text{and} \quad g_{b'co} = \left(1 - \frac{1}{A_v}\right) g_{b'c} \tag{119}$$

$$C_{ci} = (1 - A_v) C_c \quad \text{and} \quad C_{co} = \left(1 - \frac{1}{A_v}\right) C_c \tag{120}$$

Where $$A_v = \frac{V_{ce}}{V_{b'e}} \quad (121)$$

The alternate circuit of the amplifier with conductances and capacitances transferred to input and output terminals of the amplifier can be drawn as shown in Fig. 30.

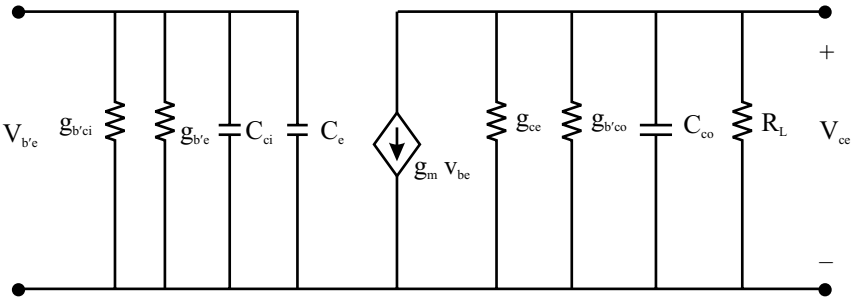


Fig. 30 Simplified high frequency model of CE BJT amplifier with resistive load

Above circuit has two high pass RC circuits. The overall transfer function of the amplifier has two poles. One belong to on input circuit and another for output circuit. So, the circuit of amplifier has two times constants corresponding to input and output circuits of the amplifier.

The time constant of RC circuit on input side can be given by,

$$\tau_i = R_{eq} C_{eq} \quad (122)$$

Where $$R_{eq} = \frac{1}{g_{b'e}} \Bigg\| \frac{1}{(1 - A_v) g_{b'c}} \quad (123)$$

and $$C_{eq} = C_e + (1 - A_v) C_c \quad (124)$$

As $g_{b'c} << g_{b'e}$ so $g_{b'c}$ can be neglected.

$$\therefore \quad R_{eq} = \frac{1}{g_{b'e}} \quad (125)$$

The cutoff frequency of RC high pass circuit on input side,

$$f_H = \frac{1}{2\pi R_{eq} C_{eq}} = \frac{g_{b'e}}{2\pi C_{eq}} \quad (126)$$

Where, $$C_{eq} = C_e + (1 - A_v) C_b \quad (127)$$

The resistance r_{ce} and $r_{b'c}$ are high so g_{ce} & $g_{b'c}$ can neglected from circuit on output side.

then, $$A_v = \frac{V_{ce}}{V_{b'e}} = -g_m R_L \quad (128)$$

$$\Rightarrow \quad C_{eq} = C_e + (1 + g_m R_L) C_c \quad (129)$$

The time constant of RC circuit on output side,

$$\tau_o = R_{eq}C_{co} = R_{eq}\left(1-\frac{1}{A_v}\right)C_c \qquad (130)$$

Where,
$$R_{eq} = \frac{1}{g_{ce}} \left\| \frac{1}{\left(1-\frac{1}{A_v}\right)g_{b'c}} \right\| R_L \qquad (131)$$

As collector junction is reverse biased and emitter junction is forward biased so $r_{b'c} >> r_{b'e}$

$\therefore \quad g_{b'c} << g_{b'e}$

As $g_{b'c}$ is very small so R_{eq} is small and τ_o is negligible.

The larger time constant of the circuit plays the dominant role as the time constant of input circuit is larger so it gives overall time constant of the amplifier. So, the overall cutoff frequency of the amplifier is determined by the input circuit.

Note :

i. When transfer function of a high frequency equivalent of an amplifier has multiple poles then pole with lowest cutoff frequency is dominant pole and gives overall cutoff frequency and time constant of the amplifier. Time constant is inverse of cutoff frequency so lowest cutoff frequency gives largest time constant of the amplifier.

ii. When high frequency voltage transfer ratio of amplifier has multiple time constants then larger time constant determine. Thus the pole corresponding to largest constant in high frequency resonance is dominant pole.

iii. The upper cutoff frequency is given by

$$f_H = \frac{1}{2\pi\tau}$$

where $\tau = R_{eq}C_{eq}$ = largest time constant

iii. Bandwidth of a two pole amplifier is smaller than bandwidth of a single pole amplifier.

iv. The transfer function of single stage CE transistor at high frequencies has one zero and two poles.

v. When transfer function of low frequency equivalent circuit of an amplifier has multiple poles then pole with highest cutoff frequency is dominant pole and gives oveall cutoff frequency and overall time constant of the amplifier. The highest cutoff frequency gives lowest overall time constant of the circuit.

vi. Gain-bandwidth product of an amplifier increases with increase in R_L and decreases with increase in R_s.

vii. Frequency response of amplifier can be determined by using four parameter h_{fe}, f_T, h_{ie}, and C_c.

Dominant Pole :

Case-I : Dominant Pole for high frequency response

If a transfer function, determining high frequency response, has several poles and if smallest of these is at f_{p1} and of each of other pole is at least two octaves higher or 4 f_{p1}, then the amplifier behaves like a single pole or single time constant amplifier where 3-dB cutoff frequency is f_{p1}. The frequency f_{p1} is called dominant pole of the amplifier.

Case-II : Dominant Pole for low frequency response

On other hand if a transfer function, determining low frequency response, has several poles and if smallest of these is at f_{p1} and of each of other pole is at least two octaves smaller or $f_{p1}/4$ then the amplifier behaves like a single pole or single time constant amplifier where 3-dB cutoff frequency is f_{p1}. The frequency f_{p1} is called dominant pole of the amplifier.

6.8 High Frequency Response of MOSFET Amplifiers

6.8.1 MOSFET Internal Capacitances

There are two types of internal capacitance of MOSFET which are discussed in the following sections,

I. The gate capacitive Effect

The gate electrode forms parallel plate capacitor with the channel with oxide layer in-between serving as dielectric. The gate oxide layer capacitance per unit area is given by,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (132)$$

Where ε_{ox} is dielectric constant of oxide and t_{ox} is thickness of oxide layer.

The gate capacitive offed can be modeled by three capacitances called gate-to-source (C_{gs}), gate-to-drain (C_{gd}) and gate to body (C_{gb}). These capacitances can be deterined as under,

i. Triode or Ohmic region

The channel has uniform depth across length of the channel when MOSFET operates triode region with small v_{DS} . If W is width of channel and L is length of channel then gate-channel capacitance is WLC_{ox}. This capacitance can be modeled by dividing equality between drain and source.

$$\therefore \quad C_{gs} = C_{gd} = \frac{1}{2} WL C_{ox} \qquad (133)$$

ii. Saturation Region

The channel has tapered shape when MOSFET operates in saturation region and it is pinched off at or near drain end. Under this condition gate-channel capacitance is approximately $\frac{2}{3}$ WL C_{ox}.

$$\therefore \quad C_{gs} = \frac{2}{3} WL C_{ox} \qquad (134)$$

In this case C_{gd} is assumed to be zero.

iii. Cut-off Region

The channel disappears when MOSFET operates in cutoff region. Under this condition gate capacitive effect is modeled as,

$$C_{gs} = C_{gd} = 0 \tag{135}$$

and

$$C_{gb} = WL\,C_{ox} \tag{136}$$

iv. Overlap Capacitance (C_{ov})

There is an additional capacitance which adds up to C_{gs} and C_{gd} due slight extension of source and drain regions below gate electrode/oxide due to diffusion. If length of over tap is L_{ov} then overlap capacitance is given by,

$$C_{ov} = WL_{ov}C_{ox} \tag{137}$$

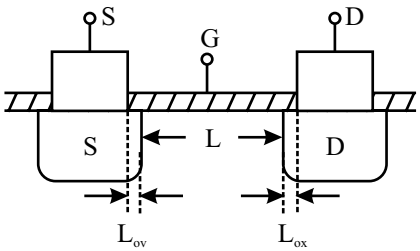


Fig. 31 Gate electrode overlap with drain and source

II. Junction Capacitances

There are two junctions in a MOSFETs between source & substrate/body as well as drain & substrate/body. These junctions offer capacitances similar to the depletion layer capacitance of a p-n junction.

i. Source-Body Capacitance, C_{sb}

The source-body capacitance of MOSFET can be given by

$$C_{sb} = \frac{\varepsilon A_{sb}}{W_{sb}} \tag{138}$$

Where ε is dielectric constant of semiconductor, A_{sb} is area of contact between source & body (substrate) and W_{sb} width of depletion layer between source and substrate.

The width of depletion layer between source & body/substrate can be given by,

$$W_{sb} = \sqrt{\frac{2\varepsilon}{q}\left[\frac{1}{N_A}+\frac{1}{N_D}\right](V_o + V_{SB})} \tag{139}$$

Where V_{SB} is reverse biasing voltage between source & substrate and V_o ss built-in potential of source-substrate junction, N_A is acceptor concentration and N_D is donor concentration.

ii. Drain-body capacitance (C_{db})

The drain-body capacitance of MOSFET is similar to source-body capacitance which can be given by,

$$C_{db} = \frac{\varepsilon A_{db}}{W_{db}}$$

Where A_{db} is area of contact between drain and substrate/body and W_{db} is width of depletion layer between drain and substrate. W_{db} can be given as,

$$W_{db} = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\left(V_o + V_{DB}\right)} \qquad (140)$$

Where V_{DB} is reverse bias voltage between drain & body or substrate.

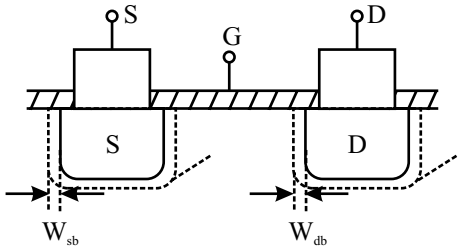
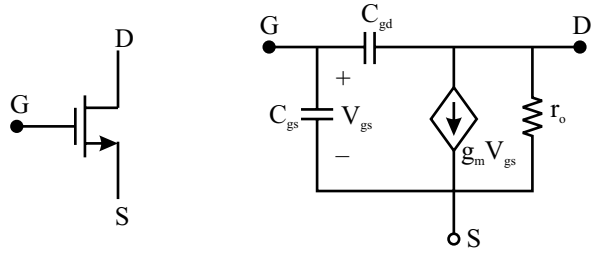


Fig. 32 Source-body and drain-body junctions of MOSFET

6.8.2 High Frequency Model of MOSFET

The high frequency equivalent or model of MOSFET can be drawn by including gate-to-source and gate-to-drain capacitances of MOSFET in its small signal model as shown in Fig.33.



(a) MOSFET (b) High frequency model of MOSFET

Fig. 33 NMOSFET and its high frequency model

Note : Above equivalent circuit has been drawn with source connected to body and by neglecting capacitance C_{db}.

6.8.3 Short circuit current gain of MOSFET

Consider a common source circuit of MOSFET in s-domain represented by hybrid-π model as shown below,

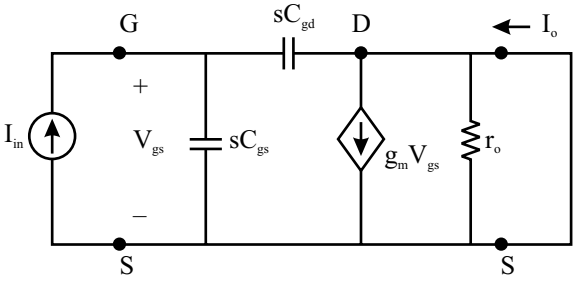


Fig. 34 High frequency model of Common Source MOSFET in s-domain with drain terminal shorted with source terminal

Applying KCL drain terminal, we have,

$$\frac{0-V_{gs}}{1/sC_{gd}}+g_m V_{gs}-I_o = 0$$

$$\Rightarrow \quad I_o = g_m V_{gs} - sC_{gd}V_{gs}$$

$$\Rightarrow \quad V_{gs} = \frac{I_o}{g_m - sC_{gd}} \tag{141}$$

Applying KCL at node 'G', we have,

$$\frac{V_{gs}}{1/sC_{gs}}+\frac{V_{gs}-0}{1/sC_{gd}}-I_{in} = 0$$

$$\Rightarrow \quad (sC_{gs}+sC_{gd})V_{gs} = I_{in}$$

Putting expression of V_{gs} from equation (141) in above equations, we have,

$$\frac{s\left(C_{gs}+C_{gd}\right)}{g_m - sC_{gd}}\times I_o = I_{in} \tag{142}$$

$$\frac{I_o}{I_{in}} = \frac{g_m - sC_{gd}}{s\left(C_{gs}+C_{gd}\right)} \tag{143}$$

Here sC_{gd} is very small in comparison of g_m.

$$\therefore \quad \frac{I_o}{I_{in}} = \frac{g_m}{s\left(C_{gs}+C_{gd}\right)} \tag{144}$$

For frequency domain $s = j\omega$

$$\Rightarrow \quad \frac{I_o}{I_{in}} = \frac{g_m}{j\omega\left(C_{gs}+C_{gd}\right)} = \frac{\omega_T}{j\omega} = \frac{2\pi f_T}{j2\pi f} = \frac{f_T}{jf} \tag{145}$$

Where, $$\omega_T = \frac{g_m}{C_{gs}+C_{gd}} = 2\pi f_T \tag{146}$$

$$\Rightarrow \qquad f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{147}$$

When $f = f_T$, the short circuit current gain of MOSFET become unity. Therefore, the parameter f_T called unity gain frequency of MOSFET.

6.8.4 High Frequency Response of Common Source Amplifier

Consider a common source amplifier using NMOS as shown in Fig. 35. Let Rsig is resistance of source of input signal connected at input of the amplifier.

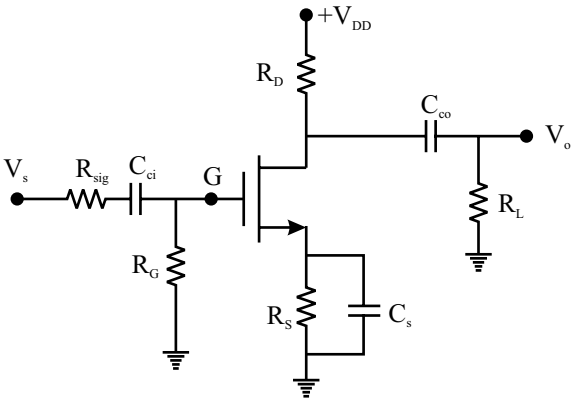


Fig. 35 High frequency response of common source MOSFET amplifier

The coupling and bypass capacitors of amplifier behave like short circuit at high frequencies so the high frequency equivalent model of the common source amplifier shown above can be drawn as shown in Fig. 36.

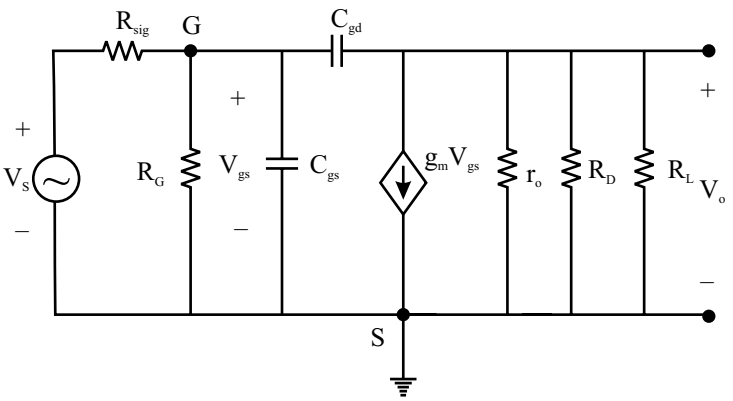


Fig. 36 High frequency equivalent circuit of common source MOSFET amplifier

Above high frequency equivalent circuit of the amplifier can be redrawn by reducing the components of the circuit as under,

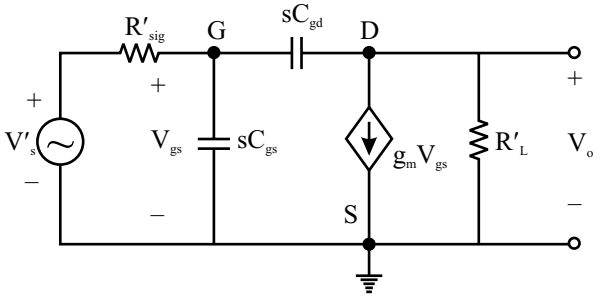


Fig. 37 Simplified high frequency equivalent circuit of common source MOSFET amplifier

Here, $R'_L = r_o \| R_D \| R_L$ (148)

$R'_{sig} = R_{sig} \| R_G$ (149)

$$V'_s = \frac{R_G}{R_{sig} + R_G} \times V_s \quad (150)$$

Output voltage of circuit, $V_o = -g_m R'_L V_{gs}$ (151)

$$V_{gs} = -\frac{V_o}{g_m R'_L} \quad (152)$$

Applying KCL at node 'G', we have,

$$\frac{V_{gs} - V_o}{1/sC_{gd}} + \frac{V_{gs}}{1/sC_{gs}} + \frac{V_{gs} - V'_s}{R'_{sig}} = 0$$

$$\Rightarrow \left(sC_{gd} + sC_{gs}\right)V_{gs} + \frac{1}{R'_{sig}}V_{gs} - sC_{gd}V_o - \frac{V'_s}{R'_{sig}} = 0$$

$$\Rightarrow \left[\frac{1}{R'_{sig}} + s\left(C_{gd} + C_{gs}\right)\right]V_{gs} - sC_{gd}V_0 = \frac{V'_s}{R'_{sig}}$$

Putting expression of V_o from equation (152) in above equation, we have,

$$\left[\frac{1}{R'_{sig}} + s\left(C_{gd} + C_{gs}\right) + sC_{gd}R'_L\right]V_{gs} = \frac{V'_s}{R'_{sig}}$$

$$\Rightarrow \frac{V_{gs}}{V'_s} = \frac{1}{1 + s\left[C_{gs} + \left(1 + g_m R'_L\right)C_{gd}\right]R'_{sig}} \quad (153)$$

Putting expression of V_{gs} from equation (152), we have

$$\frac{V_o}{V_{s'}} = -\frac{g_m R'_L}{1+s\left[C_{gs}+\left(1+g_m R'_L\right)C_{gd}\right]R'_{sig}} \quad (154)$$

Putting expression of V'_s from equation (150) in above equation, we have,

$$\frac{V_o}{V_s} = -\frac{\frac{R_G}{R_s+R_{sig}}\times g_m R'_L}{1+s\left[C_{gs}+\left(1+g_m R'_L\right)C_{gd}\right]R'_{sig}} \quad (155)$$

$$\frac{V_o}{V_s} = \frac{A_M}{1+sC_{in}R'_{sig}} \quad (156)$$

Where, $$A_M = -\frac{R_G}{R_G+R_{sig}}g_m R'_L = -\frac{R_G}{R_G+R_{sig}}\times g_m \times\left(r_o \parallel R_D \parallel R_L\right) \quad (157)$$

and $$C_{in} = C_{gs} + (1 + g_m R'_L)C_{gd} \quad (158)$$

Here A_M is represents the midband gain of the amplifier.

In frequency domain, s = jω.

$$\Rightarrow \quad \frac{V_o}{V_s} = +\frac{A_M}{1+\frac{j\omega}{\omega_H}} \quad (159)$$

Where, $$\omega_H = \frac{1}{C_{in}R'_{sig}} = \frac{1}{C_{in}\left(R_{sig} \parallel R_G\right)} = \text{Upper cutoff frequency of amplifier} \quad (160)$$

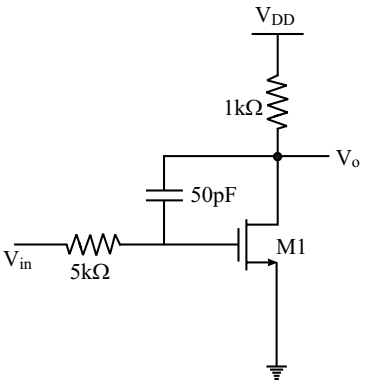
$$\Rightarrow \quad f_H = \frac{1}{2\pi C_{in}R'_{sig}} \quad (161)$$

It can be observed from above equation that highs cutoff frequency of MOSFET is determined by parasitic capacitance of MOSFET.

Note :
i. Upper cutoff frequency reduces with increase in signal source resistance (R_{sig})
ii. The capacitance C_{gd} appears as $(1 + g_m R'_L) C_{gd}$ when it is transferred as input terminals. This effect is called miller effect and factor $(1 + g_m R'_L)$ is called miller multiplication factor or miller multiplier.
iii. Emitter bypass capacitor (C_E) in BJT amplifier and source by pass capacitor (C_S) in MOSFET determine overall lower cutoff frequencies because value of C_E & C_S as highs than coupling capacitors.

Example 5

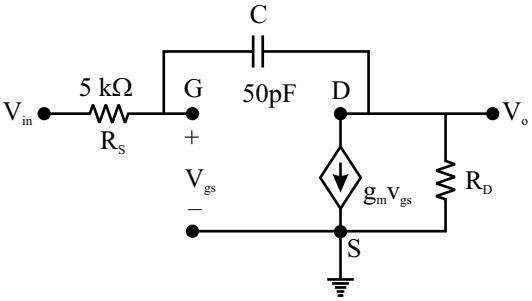
In the circuit shown in the figure, transistor M1 is in saturation and has transconductance g_m = 0.01 Siemens. Ignoring internal parasitic capacitances and assuming the channel length modulation λ to be zero, the small signal input pole frequency (in kHz) is .....



GATE(EC-III/2016/2M)

Solution : Ans. (56 to 63)

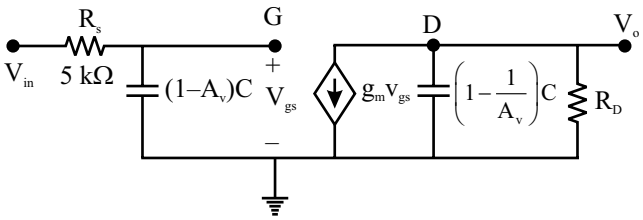
Small signal AC equivalent circuit of given amplifier can be drawn as under,



Voltage gain of amplifier, $A_v = \dfrac{V_o}{V_{gs}} = -g_m R_D = -0.01 \times 1 \times 10^3$

$\Rightarrow \quad A_v = -10$

The circuit can be redrawn by applying Miller's Theorem as under,



Input pole frequency of amplifier,

$$f = \frac{1}{2\pi R_s (1 - A_v) C}$$

$$\Rightarrow \quad f = \frac{1}{2\pi \times 5 \times 10^3 \times [1 - (-10)] \times 50 \times 10^{-12}} = 57.87\,\text{kHz}$$

6.9 Step Response of An Amplifier

A measure of fidelity an amplifier is reproduction of an input signal. A step signal or square wave signal can be easily generated & can be used to study response of an amplifier. There is close relation between leading edge of step signal and high frequency response of amplifier. Similarly, there is close relation between low frequency response and distance of flat top of a step signal. High frequency response of amplifier measures ability of amplifier to reproduce fast varying high frequency signals and low frequency response is measure of fidelity of amplifier for slow varying low frequency signal. An important characteristics of step is fast or abrupt change at beginning and very small or negligible variation during flat top position.

Rise Time :

Rise time is measure of high frequency response of an amplifier. When a step voltage is applied to an amplifier, the response of amplifier to abrupt change of input is high frequency response. The behavior of amplifier is similar to a low pass equivalent RC circuit as shown in Fig. 38.

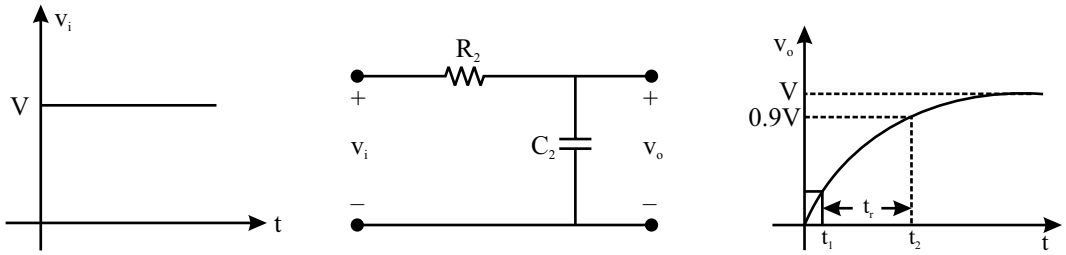


Fig. 38 Response of low pass RC circuit to step signal

Where R_2 is equivalent resistance amplifier & C_2 is equivalent capacitance of amplifier at high frequency. The response of high pass RC circuit is given by,

$$v_o(t) = V\left(1 - e^{-\frac{t}{R_2C_2}}\right) \quad (162)$$

The rise time is time required when output voltage of amplifier changes from 10% to 90% of steady value of output.

Let at $t = t_1$, $v_o(t) = 0.1\ V$

$$\Rightarrow \quad 0.1\ V = V\left(1 - e^{-\frac{t}{R_2C_2}}\right) \quad (163)$$

$$\Rightarrow \quad t_1 = 0.1\ R_2\ C_2 \quad (164)$$

Let at $t = t_2$, $v_o(t) = 0.9\ V$

$$\Rightarrow \quad 0.9\ V = V\left(1 - e^{-\frac{t}{R_2C_2}}\right) \quad (165)$$

$$\Rightarrow \quad t_2 = 2.3\ R_2\ C_2 \quad (166)$$

Rise time, $t_r = t_2 - t_1 = (2.3 - 1)\, R_2\, C_2 = 2.2\, R_2\, C_2$ (167)

For a low pass circuit upper cut off frequency is given by,

$$f_H = \frac{1}{2\pi C_2 R_2} \quad (168)$$

$$\Rightarrow \quad C_2 R_2 = \frac{1}{2\pi f_H} \quad (169)$$

$$\therefore \text{ Rise time of amplifier, } t_r = \frac{2.2}{2\pi f_H} \quad (170)$$

$$\Rightarrow \quad \boxed{t_r = \frac{0.35}{f_H}} \quad (171)$$

Tilt or Sag :

Tilt or sag is measure of low frequency response of an amplifier. An amplifier at low frequency behaves like a high pass RC circuit as shown in Fig. 39. When a step signal of amplitude 'V' is applied to a high pass filter, the output of circuit become,

$$v_o(t) = Ve^{-\frac{t}{R_1C_1}} \approx V\left(1 - \frac{t}{R_1C_1}\right) \quad (172)$$

The output voltage at any time t_1 becomes,

$$V' = V\left(1 - \frac{t_1}{R_1C_1}\right)$$

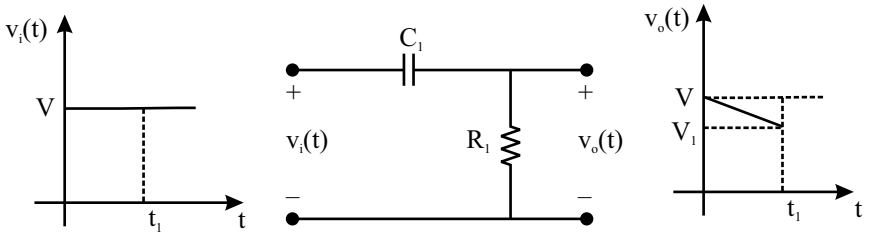


Fig. 39 Response of high pass RC circuit to step signal

% age sag or tilt, $P = \frac{V - V'}{V} \times 100 = \frac{t_1}{R_1C_1} \times 100$ (173)

If input is a square wave with $t_1 = \frac{T}{2}$

Then $P = \frac{T}{2R_1C_1} \times 100 = \frac{1}{2f\, R_1\, C_1} \times 100$ (174)

For high pass filter, lower cutoff frequency, $f_L = \frac{1}{2\pi R_1 C_1}$ (175)

$$\Rightarrow \quad R_1 C_1 = \frac{1}{2\pi f_L} \tag{176}$$

$$\therefore \quad P = \frac{\pi f_L}{f} \times 100 \tag{177}$$

The output amplifier for square wave input becomes as under,

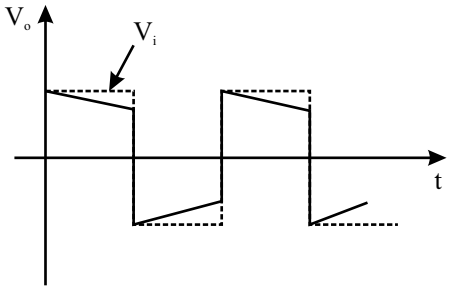


Fig. 40 Response of high pass RC circuit to a square wave input signal

Example 6

An amplifier is assumed to have a single-pole high-frequency transfer function. The rise time of its output response to a step function input is 35 nsec. The upper –3 dB frequency (in MHz) for the amplifier to a sinusoidal input is approximately at

(a) 4.55 (b) 10

(c) 20 (d) 28.6

GATE(EC/1999/2M)

Solution Ans.(b)

The rise time of an amplifier response to step input is given by,

$$t_r = \frac{0.35}{f_H}$$

$$\Rightarrow \quad f_H = \frac{0.35}{t_r}$$

given, $t_r = 35$ n sec.

$$\Rightarrow \quad f_H = \frac{0.35}{35 \times 10^{-9}}$$

$$\Rightarrow \quad \boxed{f_H = 10\text{MHz}}$$

6.10. Noise

When no signal is applied to an amplifier a small output is still obtained from output of the amplifier which is called amplifier noise. Noise is hiss or crackle sound is case of audio amplifier and it is called snow in case of a video amplifier. The various noise sources found in an amplifier are discussed as

follows,

1. Thermal or Johnson Noise

The electrons in a conductor possess varying amount of thermal energy which produces small noise potential within the conductor. These random fluctuations produced by thermal agitation of electrons are called Thermal or Johnson Noise. The rms value of thermal noise voltage of is given by,

$$V_n = \sqrt{4k\,TRB}$$

Where,

k = Baltzmann constant in J/°K

T = Resistor temperature is °K

R = Resistance

$B = f_H - f_L$ = Bandwidth in Hz

The thermal noise gives same noise power per bandwidth over complete bandwidth. Such distribution giving same noise per bandwidth over complete bandwidth is called white noise.

If such resistor is connected at input of an audio amplifier then there is amplified noise at output of the amplifier. Thermal noise can be reduced by reducing the bandwidth of amplifier & noise resistance at input of amplifier.

Note : A transistor does not generate white noise except over midband region. The amount of noise generated depends on center frequency, Q-point & source resistance

2. Shot or Schottky Noise

The fluctuation in number of minority carriers flowing through base from emitter to collector junction of a BJT is the source of noise called shot noise. The rms current due to shot noise is given by,

$$I_n = \sqrt{2q\,I_{dc}\,B}$$

Where

I_{dc} = DC current

B = Bandwidth

If R_L is load resistance then noise voltage of magnitude $V_L = I_n R_L$ appears across the load.

3. Transistor Noise or Transit Time Noise

This noise appears due to random motion of carriers crossing emitter and collector junctions and due to random recombination of holes and electrons in the base region. There is partition effect arising from random fluctuation in division of current between collector and base.

4. Flicker Noise

A low frequencies noise varies in proportion to 1/f and is called excess or flicker noise. Flicker noise is proportional to emitter current and temperature. The source of flicker is not clearly known but it is thought to be caused by recombination and generation of carriers on surface of the crystal.

Note : (i) At intermediate frequencies noise is independent of frequencies. This white noise is caused by bulk resistance of semiconductor & statistical variations of the currents (Shot noise).

(ii) At high frequencies noise figure increases with frequency due to decreasing power gain with frequency.

Noise Figure :

Noise figure is the ratio of the noise power at output of the circuit to the noise power at input which would be obtained in the same bandwidth if the only source of noise were thermal noise in the internal resistance of the signal source.

Mathematically, it is ratio of signal t noise ratio at input to the signal to noise ratio at output of the amplifier.

$$NF = 10\log\frac{S_{pi} / N_{pi}}{S_{po} / N_{po}}$$

Where S_p represents signal power and N_p represents noise power.

Noise in FET :

The FETs exhibit excellent noise characteristics. The main source of noise in FET is thermal noise of conducting channel. Shot noise is caused by gate leakage current and 1/f noise caused by surface effects.

Note : Noise figure of FET is independent of Q-point.

❐❐❐

GATE QUESTIONS

Q.1 α–cut off frequency of a bipolar junction transistor

(a) Increases with the increase in base width

(b) Increases with the increases in emitter width

(c) Increases with increase in the collector width

(d) Increases with decrease in the base width

GATE(EC/1993/2M)

Q.2 The f_T of a BJT is related to its g_m, C_π and C_μ as follows:

(a) $f_T = \dfrac{C_\pi + C_\mu}{g_m}$ (b) $f_T = \dfrac{e\pi\left(C_\pi + C_\mu\right)}{g_m}$

(c) $f_T = \dfrac{g_m}{C_\pi + C_\mu}$ (d) $f_T = \dfrac{g_m}{2\pi\left(C_\pi + C_\mu\right)}$

GATE(EC/1998/1M)

Q.3 From a measurement of the rise time of the output pulse of an amplifier whose input is a small amplitude square wave, one can estimate the following parameter of the amplifier :

(a) Gain-bandwidth product (b) Slow rate

(c) Upper 3-dB frequency (d) Lower3-dB frequency

GATE(EC/1998/1M)

Q.4 The current gain of a bipolar transistor drops at high frequencies bacause of

(a) transistor capacitances (b) high current effects in the base

(c) parasitic inductive elements (d) the early effect

GATE(EC/2000/1M)

Q.5 An npn BJT has $g_m = 38$ mA/V, $C_\mu = 10^{-14}$ F, $C_\pi = 4\times10^{-13}$ F, and DC gain $\beta_0 = 90$. For this transistor f_T and f_β are

(a) $f_T = 1.64 \times 10^8$Hz and $f_\beta = 1.47 \times 10^{10}$Hz (b) $f_T = 1.47 \times 10^{10}$Hz and $f_\beta = 1.64 \times 10^8$Hz

(c) $f_T = 1.33 \times 10^{12}$Hz and $f_\beta = 1.47 \times 10^{10}$Hz (d) $f_T = 1.47 \times 10^{10}$Hz and $f_\beta = 1.33 \times 10^{12}$Hz

GATE(EC/2001/2M)

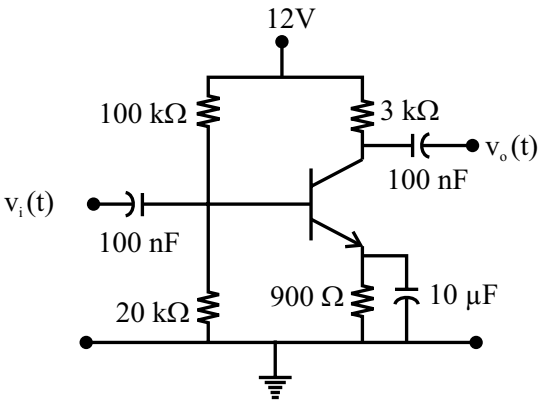
Q.6 Generally, the gain of a transistor amplifier falls at high frequencies due to the

(a) internal capacitances of the device (b) coupling capacitor at the input

(c) skin effect (d) coupling capacitor at the output

GATE(EC/2003/1M)

Q.7 A small signal source $v_i(t) = A\cos 20t + B\sin 10^6t$ is applied to a transistor amplifier as shown below. The transistor has $\beta = 150$ and $h_{ie} = 3k\Omega$. Which expression best approximates $v_0(t)$?



(a) $v_0(t) = -1500 (A \cos 20t + B \sin 10^6 t)$ (b) $v_0(t) = -150 (A \cos 20t + B \sin 10^6 t)$

(c) $v_0(t) = -1500B \sin 10^6 t$ (d) $v_0(t) = -150B \sin 10^6 t$

GATE(EC/2009/2M)

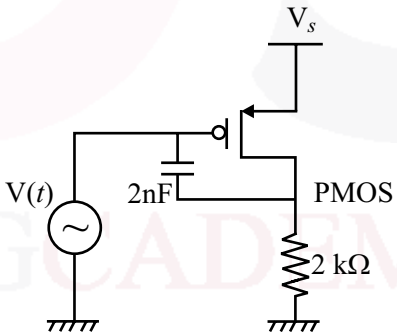
Q.8 A pulse having a rise time of 40 ns is passed through a dc amplifier with a bandwidth of 12 MHz. The rise time of the pulse at the output of the pulse at the output of the amplifier nearly equals

(a) 30 ns (b) 40 ns

(c) 50 ns (d) 80 ns

GATE(IN/1997/1M)

Q.9 In the circuit shown, the voltage source $V(t) = 15 + 0.1 \sin (100\ t)$ volts. The PMOS transistor is biased such that it is in saturation with its gate-source capacitance being 4 nF and its transconductance at the operating point being 1 mA/V. Other parasitic impedances of the MOSFET may be ignored. An external capacitor of capacitance 2 nF is connected across the PMOS transistor as shown. The input impedance in mega ohm as seen by the voltage source is ..... MΩ.



GATE(IN/2015/2M)

Q.10 The Miller effect in the context of a Common Emitter amplifier explains

(a) an increase in the low-frequency cutoff frequency

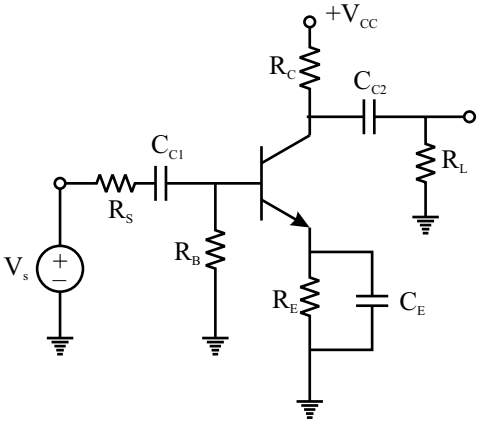
(a) an increase in the high-frequency cutoff frequency

(c) a decrease in the low-frequency cutoff frequency

(d) a decrease in the high-frequency cutoff frequency

GATE (EC-I/2017/1M)

Q.11 Common emitter amplifier shown in fig. below has $C_{C1} = C_E = C_{C2} = 1$ μF, $R_B = 100$ kΩ, $R_S = 5$ kΩ, $R_L = 5$ kΩ, $R_C = 8$ kΩ,, $R_E = 1$ kΩ. The transconductance (g_m) of BJT is 40 mA/V and input resistance (r_π) is 2.5 kΩ.

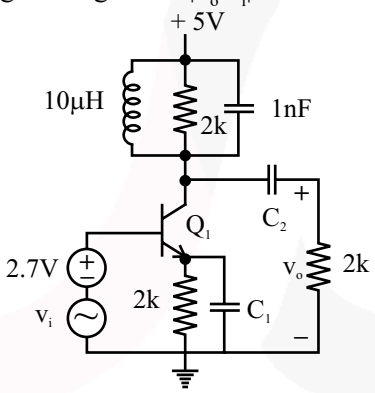


The cutoff frequency of amplifier due to C_E is.....

(a) 1.5 kHz (b) 3.8 kHz

(c) 2.35 kHz (d) 6.2 kHz

Q.12 In the circuit shown below, capacitors C_1 and C_2 are very large and are shorts at the input frequency. v_i is a small signal input. The gain magnitude $|v_o/v_i|$ at 10 Mrad/s is



(a) maximum (b) minimum

(c) unity (d) zero

GATE(EC/2011/1M)

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ANSWERS & EXPLANATIONS

Q.1 Ans.(d)

The β-cutoff frequency and α-cutoff frequencies of BJT are related by,

$$f_\beta = (1-\alpha)\, f_\alpha$$

$$\Rightarrow \quad f_\alpha = \frac{1}{1-\alpha} f_\beta$$

When basewidth of BJT is decreased the carriers recombination in the base region reduces. So the common base gain, α, increases. Therefore (1 – α) decreases which in turn increases f_α and vice-versa. Hence f_α increases with decrease in the base width.

Q.2 ***Ans.(d)***

The Short circuit unity gain frequency of BJT is given by

$$\boxed{f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}}$$

where, $C_\pi = C_e$ = Emitter junction capacitance

$C_\mu = C_c$ = Collector junction capacitance

Q.3 ***Ans.(c)***

The rise time of output pulse of an amplifier to small amplitude square wave is given by

$$t_r = \frac{0.35}{f_H}$$

where f_H = 3 – dB upper cutoff frequency.

So, rise time can be used to find upper 3-dB frequency of amplifier.

Q.4 ***Ans.(a)***

The gain of a BJT drops at high frequency due to transistors capacitance C_π and C_μ.

Q.5 ***Ans.(b)***

The short circuit unity gain frequency of BJT is given by

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

Given, $g_m = 38$ mA/V, $C_\mu = 10^{-14}$ F, $C_\pi = 4\times10^{-13}$ F and $\beta_0 = 90$

$$\Rightarrow \quad f_T = \frac{38\times10^{-3}}{2\pi(10^{-14} + 4\times10^{-13})}$$

$$\Rightarrow \quad f_T = 1.47 \times 10^{10}\,\text{Hz}$$

The unity gain frequency interms of β-cutoff frequency is given by

$$f_T = h_{fe} f_\beta = \beta f_\beta$$

$$\Rightarrow \quad \beta f_\beta = f_T$$

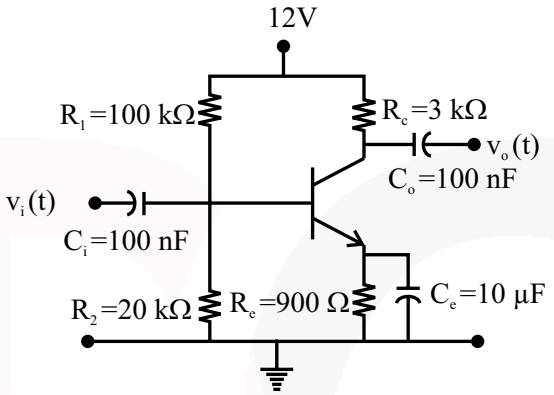
$$\Rightarrow \quad f_\beta = f_T / \beta = 1.47 \times 10^{10} / 90$$

$$\Rightarrow \quad f_\beta = 1.64 \times 10^8 \text{Hz}$$

Q.6 ***Ans.(a)***

The gain of transistor amplifier falls at high frequencies due to the internal capacitances of the device

Q.7 ***Ans.(d)***



Lower cutoff frequency of above amplifier is given by,

$$f_L = \frac{1}{2\pi C_i (R_s + R_i)} \qquad \text{.....(i)}$$

Here, $R_s = 0$, $C_i = 100\text{nF}$ and $R_i = R_1 || R_2 || h_{ie}$

$$\Rightarrow \quad R_i = 100\text{k} \,||20\text{k}||3\text{k} = 2.5\text{ k}$$

Putting above values in equation (i), we have,

$$f_L = \frac{1}{2\pi \times 100 \times 10^{-9} \times 2.5 \times 10^3} = 636\text{ Hz}$$

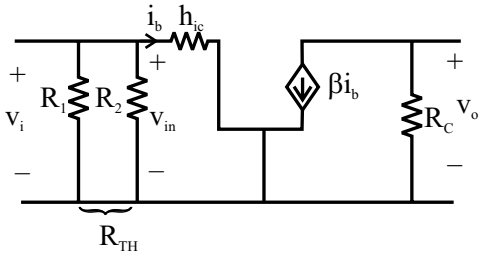
Given input signal, $v_i(t) = A \cos 20t + B \sin 10^6 t$

$$\Rightarrow \quad v_i(t) = A \cos 2\pi f_1 t + B \sin 2\pi f_2 t$$

where, $f_1 = \frac{20}{} \quad 3.18\text{Hz}$

and $f_2 = \frac{10^6}{2\pi} = 159\text{kHz}$

As frequency f_1 is less than the cutoff frequency of the amplifier so component of input with frequency f_1 is blocked by the amplifier only compenent with frequency f_2 is amplified. For second component the coupling and bypass capacitors behave like short circuit. Replacing the BJT with its equivalent h-parameter model the ac equivalent circuit of amplifier can be drawn as under,



Base current, $i_b = \dfrac{v_i}{h_{ie}}$

From output circuit,

$$v_o = -\beta i_b \times R_C = -\frac{\beta R_C}{h_{ie}} \cdot v_i$$

$$\Rightarrow \quad v_o = -\frac{150 \times 3k}{3k} \cdot B \sin 10^6 t$$

$$\Rightarrow \quad v_o = -150B \sin 10^6 t$$

Q.8 ***Ans.(a)***

The rise time of an amplifier for pulse inputs is given by,

$$t_r = \frac{0.35}{f_H}$$

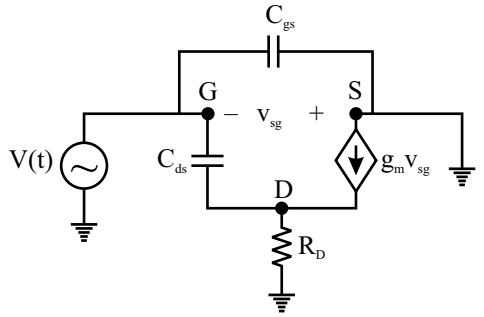
where, f_H is upper cutoff frequency of amplifier.

Given, $f_H = 12$ MHz

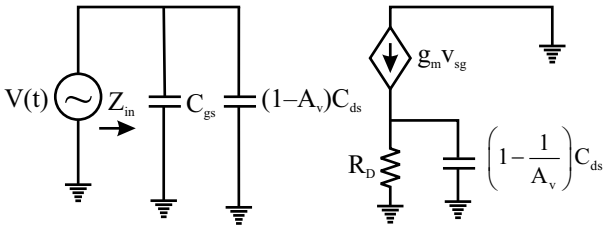
$$\Rightarrow \quad t_r = \frac{0.35}{12 \times 10^6} \approx 30 \text{ n sec}$$

Q.9 ***Ans.: 1***

AC equivalent circuit of given amplifier can be drawn as under,



Above circuit can be redrawn by applying Miller's Theorem as under,



Here A_v represents voltage gain V_o/V_{sg}. For the given circuit,

$$A_v = \frac{v_D}{v_{sg}} \approx g_m \left(R_D \,||\, \frac{1}{j\omega\left(1-\frac{1}{A_v}\right)C_{ds}} \right) \approx g_m R_D = -1\times10^{-3}\times2\times10^{3}$$

$\Rightarrow$ $A_v = -2$

Impedance seen by the source,

$$Z_{in} = \frac{1}{j\omega C_{gs}} \,||\, \frac{1}{j\omega(1-A_v)C_{ds}}$$

$\Rightarrow$ $$Z_{in} = \frac{1}{j\omega C_{eq}}$$

Where $C_{eq} = C_{gs} + (1 - A_v)\, C_{ds}$

$\Rightarrow$ $C_{eq} = 4 + [1 - (-2)] \times 2 = 10$ nF

Given, input voltage, $V(t) = 15 + 0.5 \sin 100\, t$

Frequency of signal, $\omega = 100$ rad/s

$\therefore$ $$Z_{in} = \frac{1}{j\omega C_{eq}} = \frac{1}{j100\times10\times10^{-9}} = -j1\text{M}\Omega$$

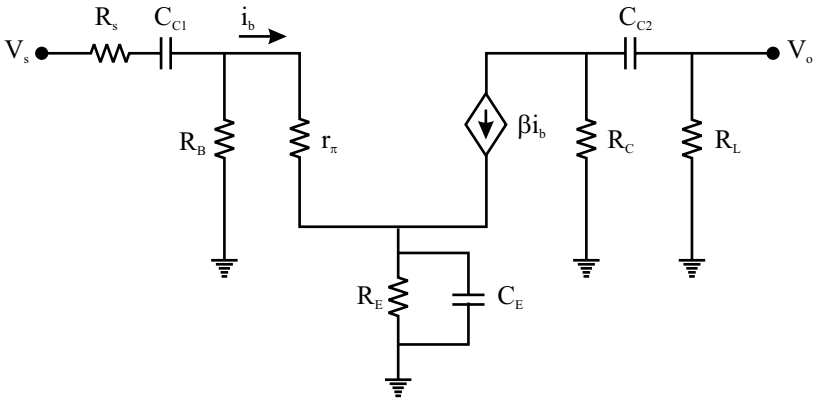
or $|Z_{in}| = 1\ \text{M}\Omega$

Q.10 Ans.(d)

The Miller's effect increases the effective capacitances of the circuit on input as well as output circuit of amplifier. The increase in effective capacitance results in increase in time constant and decrease in higher cutoff frequency of the amplifier.

Q.11 Ans.(c)

The ac equivalent of the given amplifier can be drawn as under,



Cut off frequency due to C_E is obtained by neglecting effects of C_{C1} & C_{C2} or replacing these capacitors by short circuit.

Cutoff frequency of to C_E is given by,

$$f_{C3} = \frac{1}{2\pi R_{eq3} C_E}$$

Here, R_{eq3} is equivalent resistance seen across C_E.

$$R_{eq3} = R_E \| \left(\frac{r_\pi + R_S \| R_B}{1+\beta} \right)$$

The resistances of base circuit are reduced by factor of 1+β when referred to emitter circuit.

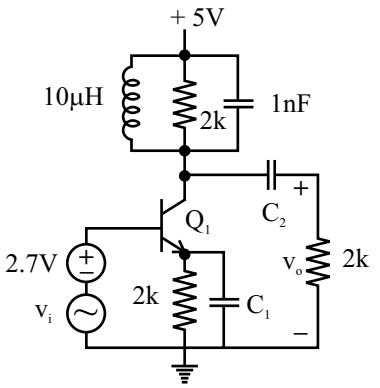
Gain of BJT, $\beta = g_m r_\pi = 40 \times 2.5 = 100$

$$\frac{1}{1+\beta} \times \left(r_\pi + \frac{R_S \times R_B}{R_S + R_B} \right) = \frac{2.5 + \frac{5+100}{5+100}\text{k}\Omega}{101} = 72.6\Omega$$

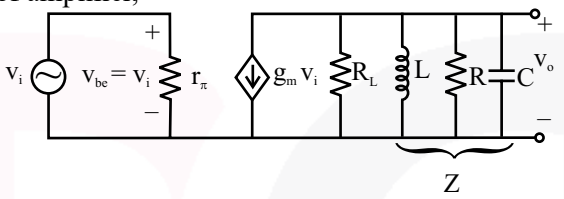
$$R_{eq3} = \frac{1000 \times 72.6}{1000 + 22.6} = 67.68\Omega$$

$$\therefore \quad f_{C3} = \frac{1}{2\pi \times 67.68 \times 1 \times 10^{-6}} = 2.35\,\text{kHz}$$

12. Ans.(a)



Ac equivalent circuit of amplifier,



Resonant frequency of output stage,

$$\omega_o = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{10\times10^{-6}\times1\times10^{-9}}} = 10 \text{ M rad/sec}$$

Output voltage of amplifier,

$$V_0 = (Z \parallel R_L)\, g_m\, v_i$$

$\therefore$ Voltage gain of amplifier,

$$A_v = \frac{v_o}{v_i} = \frac{ZR_L}{Z+R_L}\times g_m$$

$\Rightarrow$

$$A_v = \frac{1}{\frac{1}{Z}+\frac{1}{R_L}}\times g_m$$

At resonant frequency impedance of parallel RLC network is maximum. So Z is maximum at ω = 10 M rad/sec. So, $\frac{1}{Z}$ is minimum and voltage gain is maximum at ω = 10 M rad/sec.

Shortcut :- Given amplifier is tuned amplifier which has maximum voltage gain at resonant frequency of collector circuit. Given frequency is equal to resonant frequency of tank circuit so at given frequency voltage gain of amplifier is maximum.

❐❐❐

Ch 7 Multistage Amplifiers

7.1 Introduction

The performance of single stage amplifier has already been discussed earlier in previous chapters. However, a single stage amplifier may not be able to provide desired voltage gain, current gain, power gain or frequency response. In such cases multi-stage amplifier consisting of a number of amplifier stages are preferred. In a multi-stage amplifier the output of one stage is connected to input of next stage through coupling devices. The purpose of coupling devices is to transfer AC signals of previous stage to next stage and block DC biasing signals passing from one stage to next stage. Multistage amplifiers are normally named after the type of coupling used such as RC coupled, transformer coupled, impedance coupled and direct coupled. The RC coupled amplifier is most commonly used amplifier because of its low cost, compact size, and excellent frequency response.

Note :

i. *In multistage amplifier, CE configuration is most suitable for intermediate stages because of its high voltage & current gain.*

ii. *The voltage gain of CC configuration is less than unity. When CC amplifier is connected in intermediate stages it further reduces overall voltage so CC amplifier is not suitable for intermediate stages.*

iii. *The CB amplifier has current gain less than unity. So, when CB amplifier is connected in intermediate stages it further reduces overall current gain so CB amplifier is not suitable for intermediate stages.*

iv. *CC & CB configurations can be used at input stage for the purpose of impedance matching with source.*

7.2 Voltage, Current and Power Gains of Multistage Amplifiers

Case-I : Multistage Amplifier with Non-interactive Stages

Consider a multistage amplifier having non-interactive stages as shown in Fig. 1. Voltage and current gain of multi-stage amplifier are given as under,

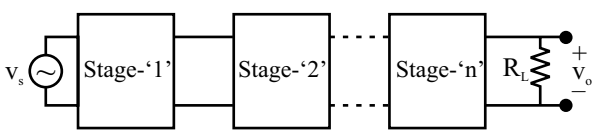


Fig. 1 Block diagram of multistage amplifier

i. Voltage Gain

The overall voltage gain of multistage amplifier is product of voltage gains of individual stages as given under,

$$A_v = A_{v1} A_{v2} \ldots\ldots A_{vn} \quad (1)$$

In decibels $$A_{v,dB} = A_{v1,dB} + A_{v2,dB} + \ldots\ldots + A_{vn,dB} \quad (2)$$

ii. Current Gain

The overall current gain of multistage amplifier is product of current gains of individual stages as given under,

$$A_i = A_{i1} A_{i2} \ldots\ldots A_{in} \quad (3)$$

In decibels $$A_{i,dB} = A_{i1,dB} + A_{i2,dB} + \ldots\ldots + A_{in,dB} \quad (4)$$

iii. Power Gain :

$$A_p = A_{p1} A_{p2} \ldots\ldots A_{pn} \quad (5)$$

In decibels $$A_{p,dB} = A_{p1,dB} + A_{p2,dB} + \ldots\ldots + A_{pn,dB} \quad (6)$$

Case-II : Multistage Amplifier with Interactive Stages

Consider a two stage cascaded amplifier with interactive stages as in Fig. 2. Here, the input resistance of stage 2 is in series with output resistance of stage 1. So, input resistance of stage 2 acts like a load to stage 1.

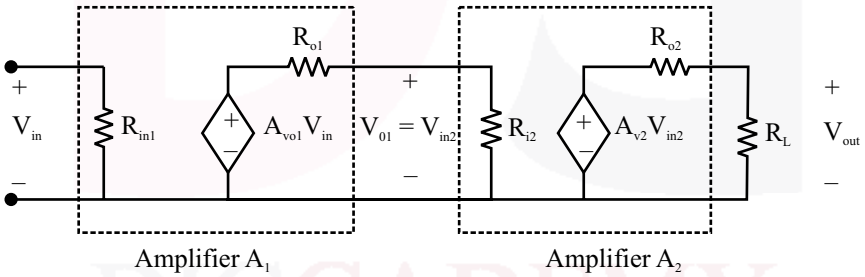


Fig. 2 Two stage amplifier with interactive stages.

Input voltage of amplifier A_2,

$$V_{in2} = \frac{R_{in2}}{R_{o1} + R_{in2}} \times A_{vo1} V_{in} \quad (7)$$

Output voltage of amplifier A_2,

$$V_{out} = \frac{R_L}{R_L + R_{o2}} \times A_{Vo2} V_{in2} \quad (8)$$

Putting the expression of V_{in2} from (7) in above equation, we have,

$$V_{out} = \frac{R_L A_{vo2}}{R_L + R_{o2}} \times \frac{R_{in2}}{R_{o1} + R_{in2}} \times A_{vo1} \times V_{in} \quad (9)$$

Overall voltage gain of the cascade connection,

$$A_v = \frac{V_{out}}{V_{in}} = \frac{A_{vo1} A_{vo2} R_{in2} R_L}{(R_L + R_{o2})(R_{in2} + R_{o1})} \quad (10)$$

It is observed from above equation that the overall gain of multistage amplifier with interactive stages is not simply product of gains of individual stages.

Example 1

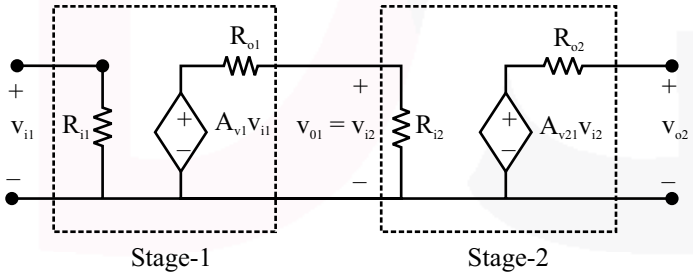
A single-stage amplifier has a voltage gain of 100. The load connected to the collector is 500 Ω and its input impedance is 1 kΩ. Two such stages are connected in cascade through an R-C coupling. The overall gain is

(a) 10000 (b) 6666.66

(c) 5000 (d) 1666.66

IES(E&T,16)

Solution : Ans.(b)



Given, $A_{v1} = A_{v2} = 100, R_{i1} = R_{i2} = 1k\Omega, R_{o1} = R_{o2} = 500\ \Omega$

Output voltage of stage 1,

$$v_{o1} = \frac{R_{i2}}{R_{o1} + R_{i2}} \times A_{V1}\, v_{i1} = v_{i2}$$

Output voltage of stage 2,

$$V_{o2} = A_{v2}\, v_{i2} = A_{v2} \times \frac{R_{i2}}{R_{o1} + R_{i2}} \times A_{v1}\, v_{i1}$$

Over all gain of cascaded combination,

$$A_v = \frac{V_{o2}}{v_{i1}} = \frac{A_{v1} A_{v2} R_{i2}}{R_{o1} + R_{i2}} = \frac{100 \times 100 \times 1000}{500 + 1000}$$

$$\Rightarrow \qquad A_v = \frac{20000}{3} = 6666.66$$

7.3 RC Coupled Multistage Amplifier

The stages of multi-stages amplifier in RC coupled amplifier are coupled through the coupling capacitors as shown in Fig.3.

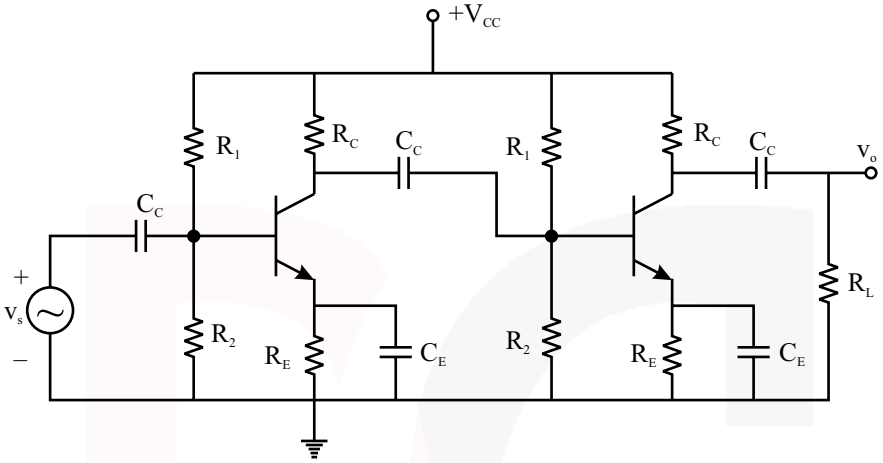


Fig. 3 RC coupled multistage amplifier

The coupling capacitors (C_C) in RC coupled amplifier are used to block the DC biasing signal from entering one stage to another stage. The coupling capacitors are also called blocking capacitors.

Frequency Response :

The frequency response of RC coupled amplifier is shown in Fig. 4. In an RC coupled amplifier, the gain at low frequencies decreases due to coupling and bypass capacitors and at high frequencies it decreases due to internal parasitic capacitances and frequency dependence of gain.

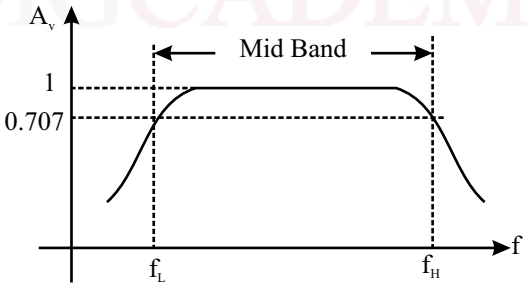


Fig. 4 Frequency response of RC coupled multistage amplifier

Advantages :

(i) Excellent frequency response

(ii) Cheaper in cost

(iii) Compact in size

Disadvantages :

(i) Low voltage & power gain due to low resistance presented by input of each stage to preceding stage.

(ii) It may become noisy with age.

(iii) It has poor impedance matching

Applications :

It is widely used as video amplifier because of its good audio fidelity.

7.4 Transformer Coupled Multistage Amplifier

A transformer coupled amplifier has transformers for coupling of signals at input and output of each stage as shown in Fig. 5. The drawback of low resistance stage of RC coupled amplifier is over come by using transformer coupled amplifier.

This amplifier has transformer which passes the AC signals from one stage to next stage and blocks the DC biasing signals from passing to the next stage.

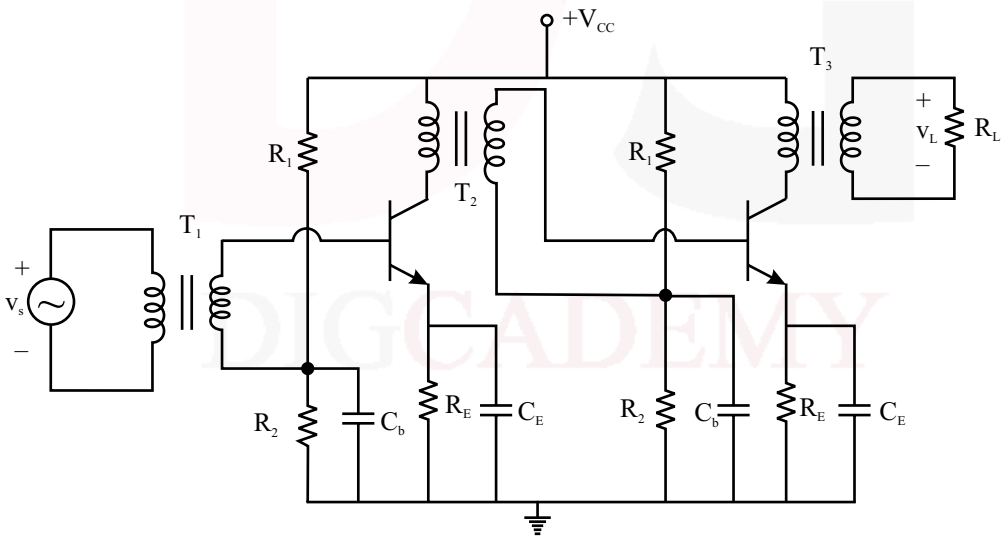


Fig. 5 Transformer coupled multistage amplifier

Frequency Response :

Frequency response of transformer coupled amplifier is very poor as shown in Fig.6. At low frequencies the gain is very poor due to low output voltage which is equal to product of collector current and transformer primary side leakage reactance. The primary leakage reactance is low at

small frequency and hence output voltage of amplifier giving low gain.

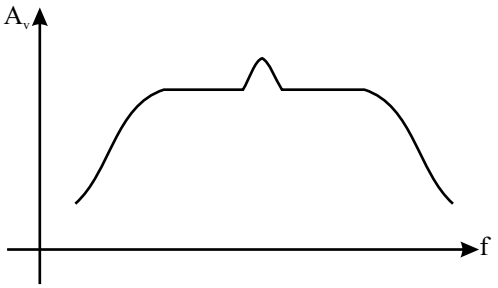


Fig. 6 Frequency response of transformer coupled multistage amplifier

At high frequencies also the inter winding capacitance of primary side acts as bypass capacitor which reduces output voltage & hence gain. Inter winding capacitance may give rise to resonance at a particular frequency which gives high voltage gain at that frequency. So, gain of transforms coupled amplifier not constant like RC coupled amplifier.

Advantages :

(i) As there is no collector resistance so losses are less and efficiency is more.

(ii) It provider excellent impedance matching & provides high gain due to impedance matching.

Disadvantages :

(i) It is not suitable for audio frequencies.

(ii) It has poor frequency response

(iii) It is Bulky & costly

(iv) It has humming noise due to transformer

Applications :

(i) It is widely used for amplifying radio frequencies above 20 kHz.

(ii) It is most suitable for impedance matching.

(iii) It is mostly used at input and output stages but not at intermediate stages.

7.5 Direct Coupled Amplifier

This amplifier does not use any coupling device between the stages of the amplifier as shown in Fig.7. Direct coupled amplifier are mostly used at very low frequency below 10 Hz. At such low frequencies coupling & by pass capacitors are not used.

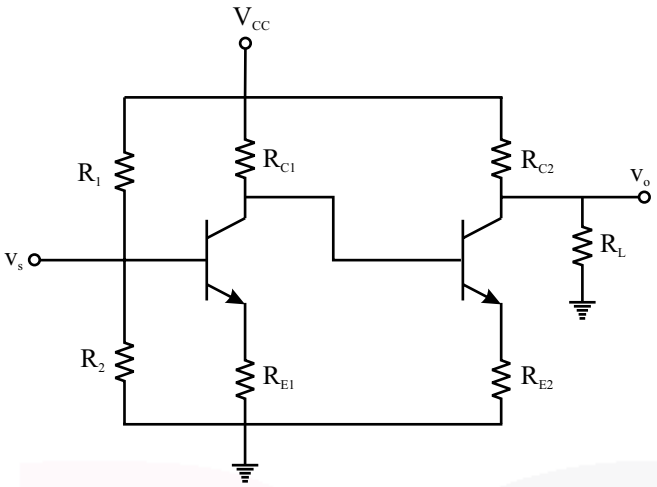


Fig. 7 Direct coupled multistage amplifier

Frequency Response :

The low frequency response of direct coupled amplifier, with no coupling and bypass capacitors, is almost flat and same as that midband but gain at high frequencies gain decreases due to parasitic internal capacitance of the device. The frequency response of direct coupled amplifier is shown in Fig. 8.

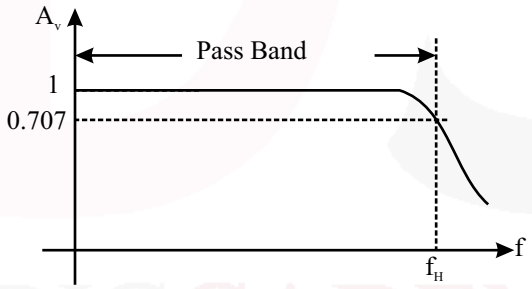


Fig. 8 Frequency response of direct coupled multistage amplifier

Advantages :

(i) It is simple in construction and cheaper in cost

(ii) It has ability to amplify signals of very low frequency.

(iii) It has almost flat response up to upper cutoff frequency.

Disadvantages :

(i) It is not suitable for high frequencies.

(ii) It has poor temperature stability.

Problem associated with design of DC amplifiers :

(i) Variation of Q-point due to temperature variations.

(ii) Current gain reduces if thermal stability is achieved.

Application :

(i) Used for head phones, load speakers etc.

7.6 Effects of Multistaging on Frequency Response

When a number of amplifier are cascaded, the output of amplifier of first stage must be calculated by including wiring capacitance, parasitic capacitance (C_{be} in case of BJT or C_{gs} in case of FET) & Miller capacitance [$C_{gd}(1 - A_v)$ in case of FET or $C_{bc}(1 - A_v)$ in case of BJT] of next state. Under such conditions overall lower cutoff frequency of combination will be equal to cutoff frequency of stage with highest cutoff frequency. Similarly, higher cutoff frequency of the combination will be equal to cutoff frequency of stage with lowest upper cutoff frequency. Multi-staging of amplifiers result in increase in overall gain of the amplifier but the overall bandwidth of the amplifier reduced in comparison to individual constituent stages.

The upper cutoff frequency of multistage amplifier with 'n' identical non-interacting stages is given by,

$$f_H^* = f_H\sqrt{2^{\frac{1}{n}} - 1} \tag{11}$$

Where, f_H is cutoff frequency of individual stage of the multistage amplifier.

The lower cut off frequency of multistage amplifier with 'n' identical non-interacting stages is given by is given by,

$$f_L^* = \frac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}} \tag{12}$$

Where, f_L is cutoff frequency of individual stage of the multistage amplifier.

From equation (11) & (12), we have,

$$f_H^* \; f_L^* = f_H f_L \tag{13}$$

Example 2

A two-stage amplifier is required to have an upper cut off frequency of 2 MHz and a lower cut off frequency of 30 Hz. The upper and lower cut off frequencies of individual stage are respectively approximately

(a) 4 MHz, 60 Hz (b) 3 MHz, 20 Hz

(c) 3 MHz, 60 Hz (d) 4 MHz, 20 Hz

IES(E&T,93)

Solution : Ans.(b)

The upper & lower cutoff frequency of n-stage amplifier is given by,

$$f_H^* = f_H\sqrt{2^{1/n} - 1}$$

Where

$f_H \rightarrow$ upper cutoff frequency of each stage.

$$f_L^* = \frac{f_L}{\sqrt{2^{1/2}-1}}$$

Where

$f_L \rightarrow$ Lower cut off frequency of each stage

Given, $f_L^* = 30$ Hz , $f_H^* = 2$ MHz and $n = 2$

Upper cutoff frequency , $2 = f_H \cdot \sqrt{2^{1/2}-1}$

$\Rightarrow$ $f_H = 3.10$ MHz

Lower cutoff frequency, $30 = \frac{f_L}{\sqrt{2^{1/2}-1}}$

$\Rightarrow$ $f_L = 19.30$ MHz

7.7 Rise Time of Multistage Amplifier

The rise time of a of n-stage amplifier in terms of rise of rise time of constituent stages stage is given by,

$$t_r = 1.1\sqrt{t_{r_1}^2 + t_{r_2}^2 + ... + t_{r_n}^2} \quad (14)$$

where $t_{r1}, t_{r2},.....t_{rn}$ are rise times of stage 1, stage 2.....& stage n respectively. The rise time of n^{th} stage of multistage amplifier is given by,

$$\boxed{t_{r_n} = \frac{0.35}{f_{H_n}}} \quad (15)$$

where f_{Hn} is 3dB upper cutoff frequency of n^{th} stage.

Note : (i) Lower cutoff frequency increases due to cascading of amplifier.

(ii) Upper cutoff frequency decreases due to cascading of amplifier.

(iii) Bandwidth of amplifier decreases due to cascading of amplifier.

(iv) Gain of amplifier increases due to cascading of amplifier.

$$A_v = A_{v1}, A_{v2}, A_{v3},..... A_{vn},$$

Note : (i) If cascade has dominant poles which is much smaller than all other poles then 3 dB cutoff frequency of cascade is equal to dominant pole frequency.

or $f_H = f_D$

where f_D is frequency of dominant pole frequency.

(ii) If dominant pole is just octave away from second pole with all other poles having much higher frquencies then the high 3dB cutoff frequency is given by,

$$f_H = 0.94\, f_D$$

(iii) If pole frequencies are not widely separated then overall cutoff frequency of multistage amplifier,

$$\frac{1}{f_H} = 1.1\sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2} + ... + \frac{1}{f_n^2}} \qquad (16)$$

where $f_1, f_2, ... f_n$ are pole frequency of various stages

Note : *i. First stage is normally used to provide high input resistance.*

ii. Intermediates stage provide most of voltage gain. In multistage amplifier the intermediate stages are made of common-emitter configuration only. Common-collector and common-base configuration can be use at input and output stages only.

iii. Output stage is normally used to provide low output resistance.

Note : *Electrolytic capacitors are often used for construction of bypass capacitors because these capacitors offer high capacitance/volume*

Example 3

The two stages of a cascade amplifier have individual upper cut-off frequencies f_1 = 5 MHz and f_2 = 3..33 MHz. What is the best approximation for the upper cut-off frequency of the cascade combination?

(a) 4.16 Mhz (b) 3.33 MHz

(c) 2.5 MHz (d) 5.00 MHz

IES(E&T,06)

Solution : Ans.(c)

The overall upper cut off frequency of multistage amplifier, with each stage having different upper cut off frequency is given by,

$$\frac{1}{f_H} = 1.1\sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2} + \frac{1}{f_3^2} + ... + \frac{1}{f_n^2}}$$

Here, $f_1, f_2 ..... f_n$ are cutoff frequency of individual stage and f_H is overall upper cutoff frequency.

Given, $n = 2,$

$f_1 = 5.0$ MHz

$f_2 = 3.33$ MHz

$$\Rightarrow \quad \frac{1}{f_H} = 1.1\sqrt{\frac{1}{5^2} + \frac{1}{3.33^2}}$$

$$\Rightarrow \quad f_H = 2.519 \text{ MHz}$$

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GATE QUESTIONS

Q.1 In an RC-coupled common emitter amplifier, which of the following is true ?

(a) Coupling capacitance affects the high frequency response and bypass capacitance affects the low frequency response

(b) Both coupling and bypass capacitance affect the low frequency response only

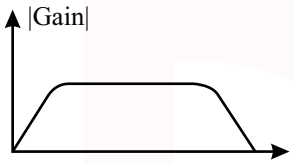
(c) Both coupling and bypass capacitances affect the high frequency response only

(d) Coupling capacitance affects the low frequency response and the bypass capacitance affects the high frequency response.

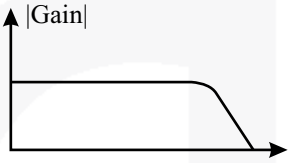
GATE(EE/1992/2 M)

Q.2 The typical frequency response of a two-stage direct coupled voltage amplifier is as shown in

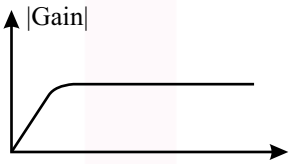
(a)



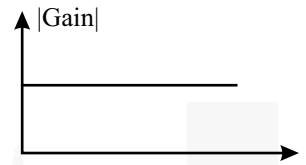
(b)



(c)



(d)



GATE(EE/2005/2 M)

Q.3 The bandwidth of an n-stage tuned amplifier, with each stage having a bandwidth of B, is given by

(a) B/n

(b) $B/\sqrt{n}$

(c) $B\sqrt{2^{1/n}-1}$

(d) $B/\sqrt{2^{1/n}-1}$

GATE(EC/1993/2M)

Q.4 In a multi-stage R-C coupled amplifier the coupling capacitor

(a) Limits the low frequency response

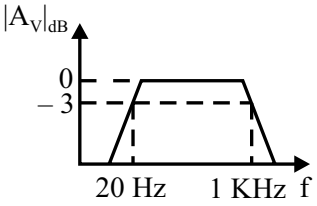
(b) Limits the high frequency response

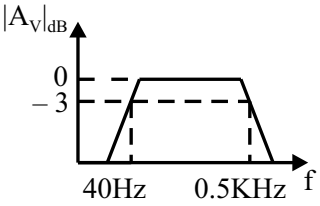
(c) Does not affect the frequency response

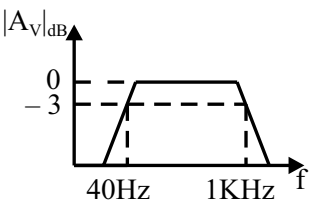
(d) Blocks the d.c. component without affecting the frequency response

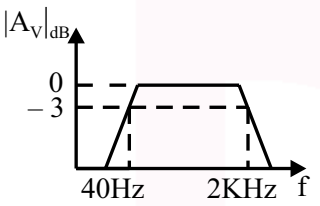
GATE(EC/1993/2M)

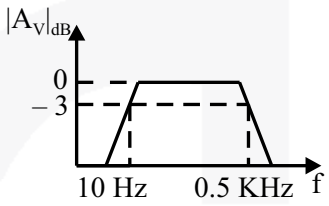
Q.5 Three identical RC-coupled transistor amplifiers are cascaded. If each of the amplifiers has a frequency response as shown in figure , the overall frequency response is as given in



(a)


(b)


(c)


(d)


GATE(EC/2002/1M)

Q.6 Three identical amplifiers with each one having a voltage gain of 50, input resistance of 1 kW and output resistance of 250 Ω, are cascaded. The open circuit voltage gain of the combined amplifier is

(a) 49 dB (b) 51 dB

(c) 98 dB (d) 102 dB

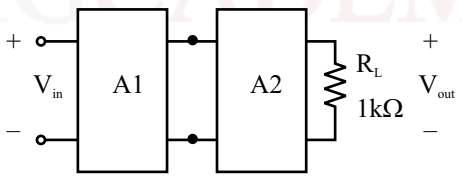
GATE(EC/2003/2M)

Q.7 A cascade connection of two voltage amplifiers A1 and A2 is shown in the figure. The open-loop gain A_{v0}, input resistance R_{in}, and output resistance R_o for A1 and A2 are as follows :

A1 : $A_{v0} = 10$, $R_{in} = 10\ k\Omega$, $R_o = 1\ k\Omega$.

A2 : $A_{v0} = 5$, $R_{in} = 5\ k\Omega$, $R_o = 200\ \Omega$.

The approximate overall voltage gain v_{out}/v_{in} is _____.



GATE(EC-II/2014/1M)

Q.8 Which one of the following statements is correct about an ac-coupled common-emitter amplifier operating in the mid-band region?

(a) The device parasitic capacitances behave like open circuits, whereas coupling and bypass capacitances behave like short circuits.

(b) The device parasitic capacitances, coupling capacitances and bypass capacitances behave like open circuits.

(c) The device parasitic capacitances, coupling capacitances and bypass capacitances behave like short circuits.

(d) The device parasitic capacitances behave like short circuits, whereas coupling and bypass capacitances behave like open circuits.

GATE(EC-II/2016/1M)

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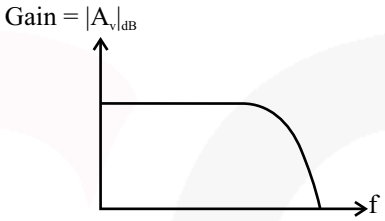
ANSWERS & EXPLANATIONS

Q.1 ***Ans.(b)***

In a multistage common emitter R-C coupled amplifier coupling capacitor and bypass capacitors limit low frequency response and parasitic or junctions or shunt capacitances limit the high frequency response.

Q.2 ***Ans.(b)***

A direct coupled amplifier has capability to amplify even very small frequency signals but its high frequency response is limited by parasitic or junction capacitances, therefore its frequency response will be as shown below,



Q.3 ***Ans.(c)***

The band width of n-stage tuned amplifier with each stage having bandwidth 'B' is given by,

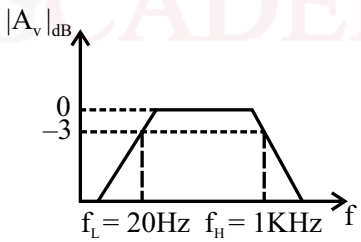
$$B^* = B\sqrt{2^{1/n} - 1}$$

Q.4 ***Ans.(a)***

In a multistage common emitter R-C coupled amplifier coupling capacitor and bypass capacitors limit low frequency response and parasitic or junctions or shunt capacitances limit the high frequency response.

Q.5 ***Ans.(a)***

The frequency response of each stage



When three identical stage each have same frequency response as shown in above figure are cascaded then cut off frequencies of overall amplifier will be,

$$f_L^* = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

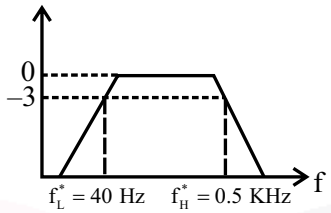
$$\Rightarrow \quad f_L^* = \frac{20}{\sqrt{2^{1/3} - 1}}$$

$\Rightarrow \quad f_L^* = 39.23 \text{ Hz}$

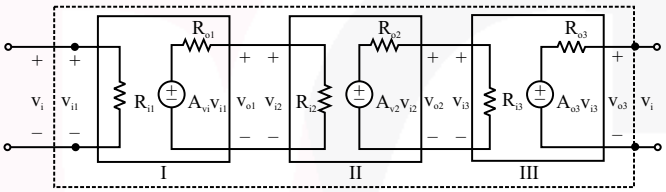
Upper cutoff frequency of the amplifier,

$$f_H^* = f_H\sqrt{2^{1/n}-1} = 1\times10^3\sqrt{2^{1/3}-1} = 509.79 \text{ Hz}$$

So, the overall frequency response becomes as shown below,



Q.6 ***Ans.(c)***



When three identical voltage amplifiers are cascaded the block diagram of overall amplifier can be drawn as under.

$$R_{i1} = R_{i2} = R_{i3} = 1k\Omega,$$

$R_{o1} = R_{o2} = R_{o3} = 250\ \Omega$, $A_{V1} = A_{V2} = A_{V3} = 50$

open circuit gain of each stage,

$$A_{vk} = \frac{V_{ok}}{V_{ik}}$$

Output voltage of stage - III,

$$V_0 = V_{03} = A_{v3}V_{i3} = 50V_{i3} \quad .....(i)$$

For stage- II, $$V_{i3} = V_{02} = \frac{R_{i3}}{R_{02}+R_{i3}}A_{v2}V_{i2} = \frac{1000}{250+1000}\times50V_{i2} = 40V_{i2} \quad .....(ii)$$

From equation (i) and (ii), we have,

$$V_0 = 50 \times 40V_{i2} = 2000V_{i2} \quad .....(iii)$$

For stage - I, $V_{i2} = V_{01}$

$$= \frac{R_{i2}}{R_{01}+R_{i2}}\times A_{Vi}V_{i1} = \frac{200}{5}V_{il} = 40V_{i1} \quad ....(iv)$$

From equations (iii) and (iv), we have,

$\Rightarrow \quad V_0 = 2000\times40\ V_{i1} = 8\times10^4\,V_{i1}$

Also, $V_{i1} = V_{i2} = V_i$ = input to over all amplifier

$\Rightarrow$ $V_0 = 8 \times 10^4 V_i$

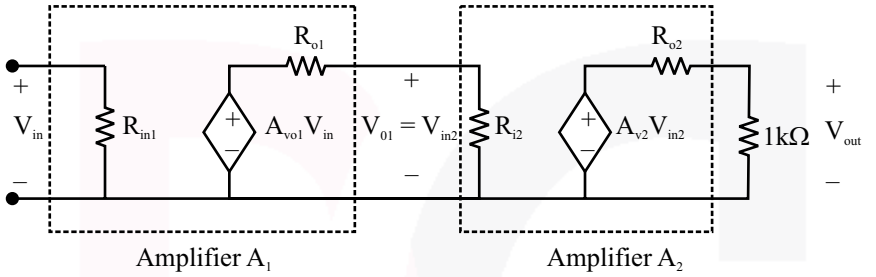
$\therefore$ Overall gain of all cascaded stages,

$$A_v = \frac{V_0}{V_i} = 8 \times 10^4$$

In dB, $A_{V,dB} = 20 \log 8 \times 10^4 = 98.06$ dB

Q.7 ***Ans.(34.0 to 35.3)***

The equivalent circuit diagram of cascaded Connection can be drawn as under



Input voltage of amplifier A_2,

$$V_{in2} = \frac{R_{in2}}{R_{o1} + R_{in2}} \times A_{vo1} V_{in}$$

Output voltage of amplifier A_2,

$$V_{out} = \frac{R_L}{R_L + R_{o2}} \times A_{Vo2} V_{in2}$$

Putting the expression of V_{in2} from (i) in above equation, we have,

$$V_{out} = \frac{R_L A_{vo2}}{R_L + R_{o2}} \times \frac{R_{in2}}{R_{o1} + R_{in2}} \times A_{vo1} \times V_{in}$$

Overall voltage gain of the cascade connection,

$$A_v = \frac{V_{out}}{V_{in}} = \frac{A_{vo1} A_{vo2} R_{in2} R_L}{(R_L + R_{o2})(R_{in2} + R_{o1})}$$

Given, A_{vo1} =10, R_{in1} = 10 kΩ, R_{o1} = 1 kΩ, R_L = 1 kΩ, A_{v2} =5, R_{in2} = 5 kΩ, R_{o2} = 200 Ω

$$A_v = \frac{10 \times 5 \times 5 \times 10^3 \times 1 \times 10^3}{(1 \times 10^3 + 200)(5 \times 10^3 + 1 \times 10^3)} = 34.722$$

Q.8 ***Ans.(a)***

In the mid-band region of an ac-coupled common-emitter amplifier, the device parasitic capacitances behave like open circuits, whereas coupling and bypass capacitances behave like short circuits.

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Ch 8 Compound Circuits of BJT & MOSFET

8.1 Introduction

In previous chapters a number BJT & MOSFET circuits based on CE,CB and CC in case BJT and CS,CG and CD in case MOSFET have been discussed in detail. This chapter introduces a number of BJT and MOSFET circuits which are very popular and have got a number of important applications.

8.2 Cascade Connection

When the amplification of single stage is not sufficient or input and output impedances are of not correct magnitude, two or more amplifier stages may be connected in cascade to meet the requirement. The cascade connection consists of output of one stage fed to input of next stage. Cascade connection may consists of similar configurations of amplifiers or dissimilar configurations depending upon application. Fig. 1 shows the cascade connection of two RC coupled CE BJT amplifiers.

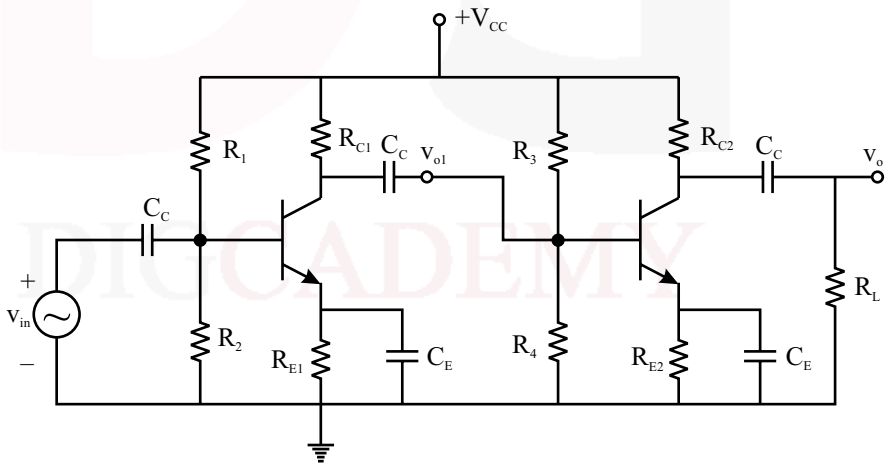


Fig. 1 Cascade connection of two CE BJT amplifier

Assuming, the BJTs to be identical, the AC equivalent circuit of the combination can be drawn by replacing the BJTs by their r_π-model, coupling and bypass capacitors by short circuit and biasing signals by ground as shown in Fig. 2.

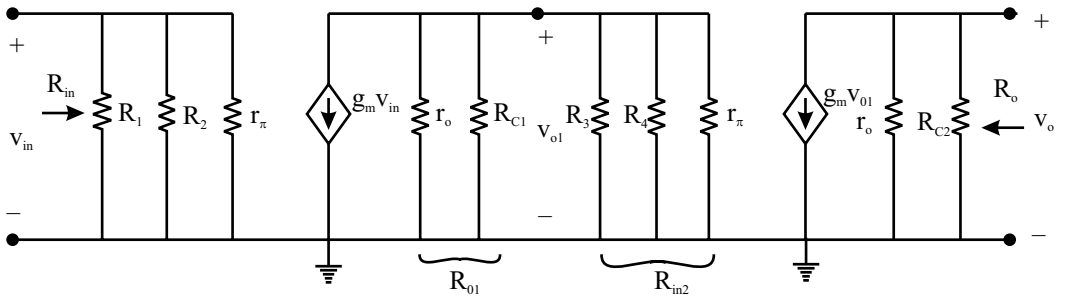


Fig. 2 Cascade connection of two CE BJT amplifier

Input resistance of combination is the input of stage 1 which can be given by,

$$R_{in} = R_{in1} = R_1 \parallel R_2 \parallel r_\pi \quad (1)$$

Output resistance of combination is the output of stage 2 which can be given by,

$$R_o = R_{o2} = r_o \parallel R_{c2} \quad (2)$$

Output resistance of stage 1,

$$R_{o1} = r_o \parallel R_{c1} \quad (3)$$

Input resistance of stage 2,

$$R_{in2} = R_3 \parallel R_4 \parallel r_\pi \quad (4)$$

Output voltage of stage 1,

$$v_{o1} = (R_{o1} \parallel R_{in2})\, g_m v_{in} = (r_o \parallel R_{c1} \parallel R_3 \parallel R_4 \parallel r_\pi)\, g_m v_{in} \quad (5)$$

Voltage gain of stage 1, $$A_{v1} = \frac{v_{o1}}{v_{in}} = -(R_o \parallel R_{in})\, g_m = -\frac{\beta(R_o \parallel R_{in})}{r_\pi} \quad (6)$$

Output voltage of stage 2, $$v_o = g_m v_{o1}\,(r_o \parallel R_{c2}) \quad (7)$$

Voltage gain of stage 2, $$A_{v2} = \frac{v_o}{v_{o1}} = -g_m (r_o \parallel R_{c2}) = -\frac{\beta(r_o \parallel R_{c2})}{\beta} \quad (8)$$

From equations (5) and (7), we have,

$$v_o = g_m(r_o \parallel R_{c2}) \times (r_o \parallel R_{c1} \parallel R_3 \parallel R_4 \parallel r_\pi)\, g_m v_{in} \quad (9)$$

Overall voltage gain, $$A_v = \frac{v_o}{v_{in}} = g_m^2(r_o \parallel R_{c2}) \times (r_o \parallel R_{c1} \parallel R_3 \parallel R_4 \parallel r_\pi) \quad (10)$$

It is noted here that the voltage gain of stage 1 is affected by input resistance of second stage 2 because of interaction among the stages.

Note : i. For interactive stages : voltage gain, $A_v \neq A_{v1}A_{v2}$

ii. For non-interactive stages : voltage gain, $A_v = A_{v1}A_{v2}$

8.3 Darlington Pair

A Darlington pair is a cascade connection of two emitter follower or common collector (CC)

amplifiers in which emitter terminal of first stage is directly connected input base terminal of second stage. The output is taken form emitter terminal of second stage as shown in Fig. 3.

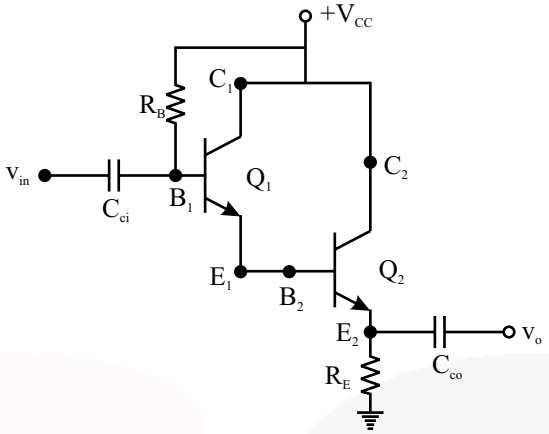


Fig.3 Darlington pair amplifier

Replacing BJTs by their approximate r_π-model, the ac equivalent circuit can be drawn as shown in Fig.4.

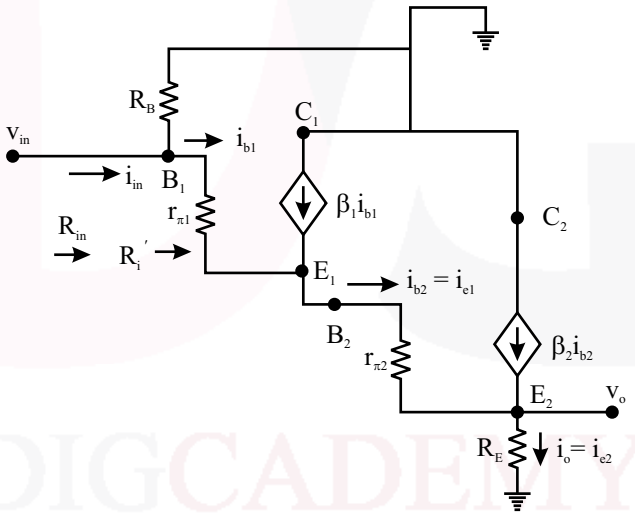


Fig.4 Small signal equivalent circuit of Darlington pair amplifier

Applying KCL in input circuit, have

$$v_{in} = r_{\pi 1} i_{b1} + r_{\pi 2} i_{b2} + R_E i_{e2} \quad (11)$$

Applying KCL at node E_1 & E_2, we have,

$$i_{b2} = i_{b1} + \beta_1 i_{b1} = (1 + \beta_1) i_{b1} \quad (12)$$

$$i_{e2} = i_{b1} + \beta_2 i_{b2} = (1 + \beta_2) i_{b2} = (1 + \beta_2)(1 + \beta_1) i_{b1} \quad (13)$$

From equation (11), (12) and (13), we have,

$$v_{in} = r_{\pi 1} i_{b1} + (1+\beta_1) r_{\pi 2} i_{b1} + (1+\beta_1)(1+\beta_2) R_E i_{b1} \quad (14)$$

$$\Rightarrow \quad R'_i = \frac{v_{in}}{i_{b1}} = r_{\pi 1} + (1+\beta_1) r_{\pi 2} + (1+\beta_1)(1+\beta_2) R_E \tag{15}$$

For large value of β_1 and β_2,

$$1 + \beta_1 \approx \beta_1 \tag{16}$$

and
$$1 + \beta_2 \approx \beta_2 \tag{17}$$

$$\Rightarrow \quad R'_i = r_{\pi 1} + \beta_1 r_{\pi 2} + \beta_1 \beta_2 R_E \tag{18}$$

Input Resistance :

Total input impedance of circuit,

$$R_{in} = R'_i \,||\, R_B \tag{19}$$

When R_B is large, $R_i \approx R'_i = r_{\pi 1} + (1+\beta_1) r_{\pi 2} + (1+\beta_1)(1+\beta_2) R_E \approx r_{\pi 1} + \beta_1 r_{\pi 2} + \beta_1 \beta_2 R_E$ (20)

If $\beta_1 = \beta_2 = \beta$ then $R_i \approx \beta^2 R_E$ (21)

Output voltage $v_o = R_E i_{e2} = (1 + \beta_2)(1 + \beta_1) R_E i_{b1}$ (22)

From eq. (14), $i_{b1} = \frac{v_{in}}{R'_i} = \frac{v_{in}}{r_{\pi 1} + (1+\beta_1) r_{\pi 2} + (1+\beta_1)(1+\beta_2) R_E}$ (23)

Voltage Gain:

From equation (22) and (23), we have,

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = \frac{(1+\beta_1)(1+\beta_2) R_E}{r_{\pi 1} + (1+\beta_1) r_{\pi 2} + (1+\beta_1)(1+\beta_2) R_E} \tag{24}$$

From above relation it is clear that voltage gain, $A_v < 1$

For large value of β_1 & β_2

$$r_{\pi 1} + (1+\beta_1) r_{\pi 2} + (1+\beta_1)(1+\beta_2) R_E \approx (1+\beta_1)(1+\beta_2) R_E \tag{25}$$

$$\therefore \quad \boxed{A_v \approx 1} \tag{26}$$

Current Gain:

Output current, $i_o = i_{e2} = (1 + \beta_1)(1 + \beta_2) i_{b1}$ (27)

Base current of Q_1, $i_{b1} = \frac{R_B}{R_B + R'_i} \times i_{in}$

$$\Rightarrow \quad i_o = \frac{(1+\beta_1)(1+\beta_2)}{R_B + R'_i} \times R_B i_{in} \tag{28}$$

Current gain, $$A_i = \frac{i_o}{i_{in}} = \frac{(1+\beta_1)(1+\beta_2)R_B}{R_B + R_i'} \quad (29)$$

If R_B is selected to be much greater than R'_i then $R_B + R'_i \approx R_B$ (30)

$\Rightarrow$ $$A_i \approx (1+\beta_1)(1+\beta_2) \quad (31)$$

Since β_1 & β_2 are much greater than unity therefore current gain,

$$\boxed{A_i \approx \beta_1 \beta_2} \quad (32)$$

If both transistors are identical with, $\beta_1 = \beta_2 = \beta$ then,

$$\boxed{A_i = \beta^2} \quad (33)$$

Output Resistance :

The output resistance of Darlington's pair can be obtained by setting $v_{in} = 0$. When $v_{in} = 0$, the AC equivalent circuit of Darlington pair can be drawn as shown in Fig.5.

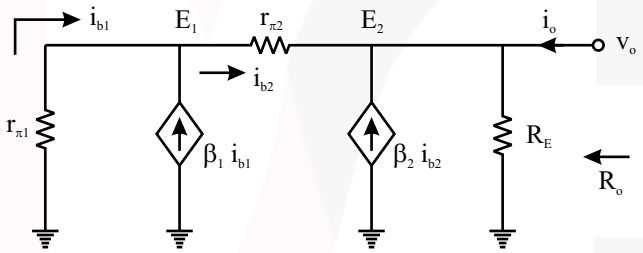


Fig.5 Equivalent circuit of Darlington pair amplifier for output resistance

Voltage at node E_1, $$v_{E1} = -r_{\pi 1} i_{b1} \quad (34)$$

Applying KCL at node E_1, we have,

$$i_{b2} = i_{b1} + \beta i_{b1} = (1+\beta_1) i_{b1} \quad (35)$$

Applying KCL at node E_2, we have,

$$\frac{v_o}{R_E} - i_{b2} - \beta_2 i_{b2} - i_o = 0$$

$\Rightarrow$ $$v_o - (1+\beta_2) R_E i_{b2} - i_o R_E = 0 \quad (36)$$

Putting expression of i_{b2} from equation (35) in above equation, we have,

$$v_o - (1+\beta_2)(1+\beta_1) R_E i_{b1} - i_o R_E = 0 \quad (37)$$

Output voltage circuit can be related to i_{b1} & i_{b2} as under,

$$v_o = -r_{\pi 2} i_{b2} - r_{\pi 1} i_{b1}$$

$\Rightarrow$ $$v_o = -(1+\beta_1) r_{\pi 2} i_{b1} - r_{\pi 1} i_{b1}$$

$\Rightarrow$ $$i_{b1} = \frac{}{r + (1+\beta_1) r_2} \quad (38)$$

From equation (37) and (38), we have,

$$v_o + \frac{(1+\beta_1)(1+\beta_2)R_E}{r_{\pi 1} + (1+\beta_1)r_{\pi 2}} v_o = i_o R_E$$

Output resistance, $$R_o = \frac{v_o}{i_o} = \frac{R_E\left[r_{\pi 1} + (1+\beta_1)r_{\pi 2}\right]}{r_{\pi 1} + (1+\beta_1)r_{\pi 2} + (1+\beta_1)(1+\beta_2)R_E} \quad (39)$$

If both transistors are identical with, $\beta_1 = \beta_2 = \beta$, $r_{\pi 1} = r_{\pi 2} = r_\pi$ then

$$R_o = \frac{v_o}{i_o} = \frac{(2+\beta)r_\pi R_E}{(2+\beta)r_\pi + (1+\beta)^2 R_E} \quad (40)$$

If β is large, so $(1 + \beta) \approx \beta$, $(2 + \beta) \approx \beta$ and

$$\Rightarrow \quad R_o = \frac{\beta r_\pi R_E}{\beta r_\pi + \beta^2 R_E} = \frac{r_\pi R_E}{r_\pi + \beta R_E} \quad (41)$$

For large value of β, $r_\pi + \beta R_E \approx \beta R_E$

$$\Rightarrow \quad \boxed{R_o = \frac{r_\pi R_E}{\beta R_E} = \frac{r_\pi}{\beta}} \quad (42)$$

But $r_\pi = (1 + \beta)\, r_e \approx \beta\, r_e$

$$\boxed{R_o \approx r_e} \quad (43)$$

The resistance of BJT seen from emitter terminal of output stage of Darlington pair is approximately is equal to r_e. As the resistance r_e is small, so, output resistance of Darlington pair is small.

Note : The small signal analysis of Darlington pair discussed above can be converted from r_π model to approximately h-parameter by simply replacing r_π by h_{ie} and β by h_{fe}.

Advantages :

i. Darlington pair provides very high current gain and almost unity voltage gain so it can be used to raise power level without raising voltage level

ii. It has very high input impedance and low output impedance so it provides excellent impedance matching between load and source.

Drawback of Darlington Pair :

Major drawback of Darlington pair is that leakage current of input emitter follower is large and it is amplified by second stage. Hence, overall leakage current becomes high due to which the Darlington connection of three or more stages is impractical.

Boot strapped Darlington Circuit :

Bootstrapped Darlington circuit is used to increase overall input resistance of Darlington pair. It consists of a capacitor C_o connected between collector of first stage and emitter of second stage. A resistance is also connected between collector and supply terminal in first stage of the pair. Fig. 6 exhibits the circuit diagram of a bootstrapped Darlington pair. Approximate value of input resistance

of bootstrapped Darlington pair is given by,

$$R_i = h_{fe1}\, h_{fe}\, R_E = \beta_1 \beta_1 R_E \quad (44)$$

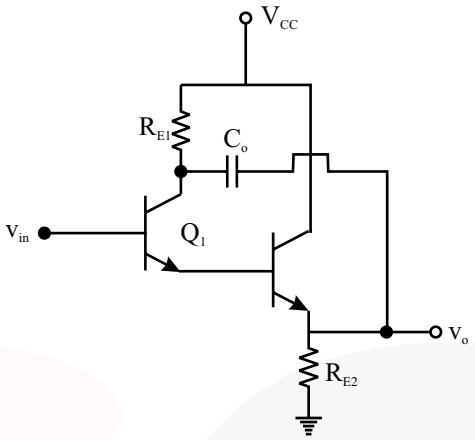


Fig.6 Bootstrapped Darlington pair amplifier

Note : i. Darlington pair has very high input resistance.

$$R_i \approx \beta^2 R_E$$

ii. Voltage gain of Darlington pair is small and less than unity of order of 0.998.

iii. Current gain of Darlington pair is very high.

$$R_i = \beta_1 \beta_2 \approx \beta^2$$

iv. Output resistance of Darlington pair is low.

$$R_o \approx r_e$$

v. Darlington pair is used to get overall high current gain.

vi. Overall gain conductance of Darlington pair is equal to transconductance stage 2.

$$\therefore \quad g_m = g_{m2}$$

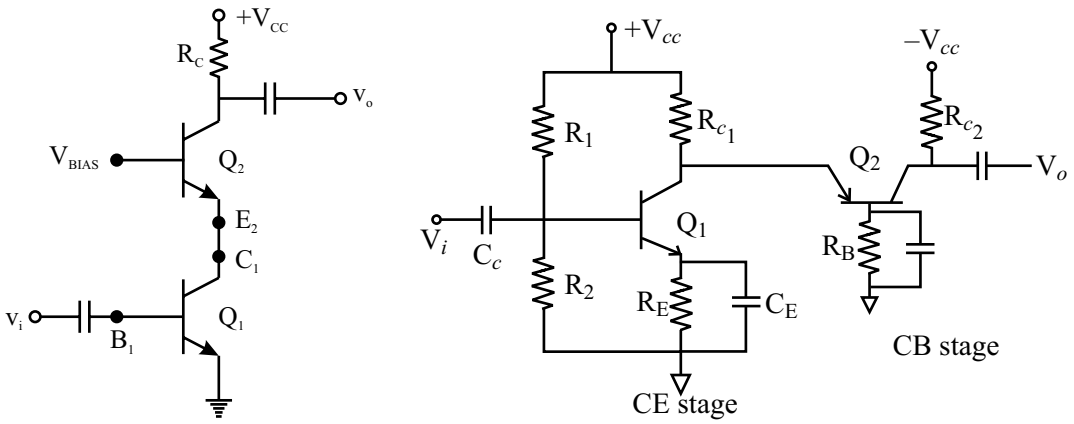
Note : i. A Darlington pair is cascading of two emitter follower circuits with infinite resistance in emitter of first stage.

ii. Darlington pair is used to achieve very high input resistance in comparison to an emitter follower circuit.

iii. Output resistance of Darlington pair is almost double of that of single stage emitter follower

8.4 Cascode Connection

A cascode amplifier consists of a CE configuration at input stage and CB configuration at output stage. A cascode amplifier combines the advantages of high input resistance and large transconductance of CE amplifier with current buffering property and superior high frequency response of CB amplifier. A cascode amplifier provides wide bandwidth but almost same DC gain as provided by CE amplifier. A cascode amplifier is used to amplify video signals over a wide band of frequencies. Fig. 7 shows the circuit diagram of a cascode amplifier using BJT.



(a) Using npn transistors at both stages (b) Using npn CE at input and pnp CB at output stage

Fig. 7 Cascode amplifier using BJT

The small signal equivalent of cascode connection of Fig. 7(a) using r_π-model of BJT can be drawn as shown in the Fig. 8.

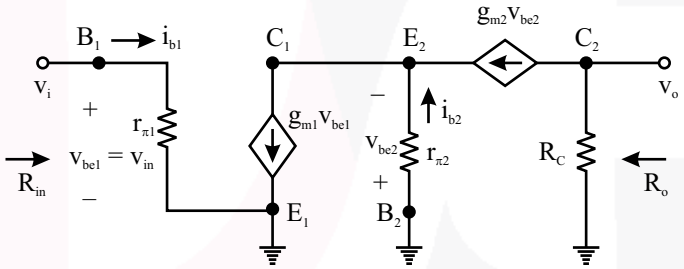


Fig. 8 Small signal equivalent of cascode amplifier

Input Resistance :

$$R_{in} = R_{in1} = r_{\pi 1} \tag{45}$$

Note : Input resistance of cascode amplifier is same as input resistance of input CE stage.

Applying KCL at node E_2 , we have,

$$\frac{v_{E2}}{r_{\pi 2}} + g_{m1} v_{in} - g_{m2} v_{be2} = 0 \tag{46}$$

From input circuit, $v_{be1} = v_{in}$

$$\Rightarrow \frac{v_{E2}}{r_{\pi 2}} + g_{m1} v_{in} - g_{m2} v_{be2} = 0 \tag{47}$$

but $$v_{E2} = -v_{be2} = v_{CE1} \tag{48}$$

$$\therefore \quad -\frac{v_{be2}}{r_{\pi 2}} + g_{m1} v_{in} - g_{m2} v_{be2} = 0 \tag{49}$$

$$\Rightarrow \qquad \left(\frac{1}{r_{\pi 2}} + g_{m2}\right) v_{be2} = g_{m1} v_{in}$$

Voltage gain of input stage,

$$A_{v1} = \frac{v_{ce1}}{v_{in}} = -\frac{v_{be2}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + \dfrac{1}{r_{\pi 2}}} = -\frac{g_{m1} r_{\pi 2}}{1 + g_{m2} r_{\pi 2}} \approx -1 \qquad (50)$$

Output voltage of output stage,

$$v_o = -g_{m2} v_{be2} \times R_C \qquad (51)$$

Voltage gain of output, $A_{v2} = \dfrac{v_o}{v_{be2}} = -g_{m2} R_C$ (52)

Overall voltage gain, $A_v = A_{v1} A_{v2} \approx (-1)(-g_{m2} R_C) = g_{m2} R_C$ (53)

It is observed here that most of voltage gain of cascode combination is provided by the second or output stage of the combination.

Output resistance :

Output resistance of cascode connection can be obtained by setting $v_{in} = 0$. When input voltage is zero or $v_{in} = v_{be1} = 0$, the dependent current source $g_m v_{be1}$ becomes zero and behave like open circuit. In that case output resistance becomes,

$$R_o \approx R_C$$

Note :

i. The output resistance of cascode connection is equal to the output resistance of CB stage.

ii. In cascode amplifier the overall transconductance of cascode connection it equal to conductance of CE stage $g_m = g_{m1}$.

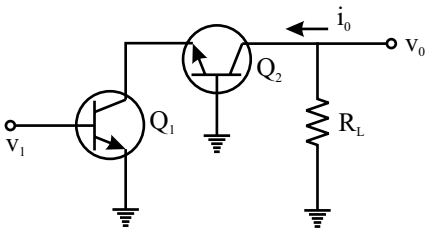
iii. Input resistance and current gain of cascode amplifier essentially same as that of input CE stage and output resistance and voltage gain are same as that of output CB stage. The overall voltage gain is equal to product of voltage gain of CE and CB stages.

iv. Voltage gain of input CE stage is normally kept about unity in order to eliminate miller effect. And CB stage provide most of voltage gain of cascode combination.

v. Cascode amplifier is used to amplify video signals over a wide band of frequencies.

Example 1

In the cascode amplifier shown in figure if the common emitter stage (Q_1) has a transconductance g_{m1}, and the common base stage (Q_2) has a transconductance g_{m2} then the overall transconductance g ($= i_0/v_i$) of the cascade amplifier is

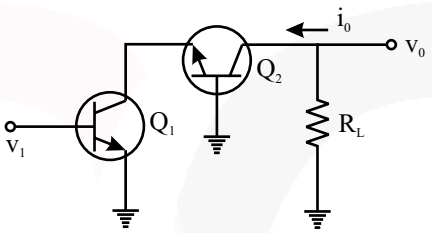


(a) g_{m1} (b) g_{m2}

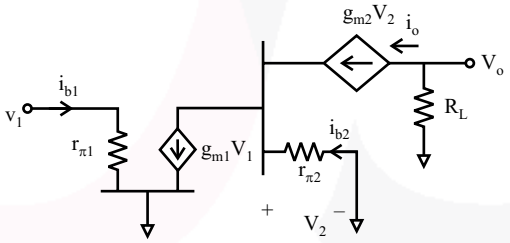
(c) $g_{m1}/2$ (c) $g_{m2}/2$

GATE(EC/1999/1M)

Solution : Ans.(a)



Replacing BJTs by their ac equivalent circuits, we have



From above circuit,

$$g_{m1} V_i = i_o + i_{b2} \approx i_o$$

$$\Rightarrow \quad \boxed{g = \frac{i_o}{v_i} = g_{m1}}$$

8.5 Current Mirror

A current mirror provides constant current and is used primarily in integrated circuit due to requirement of matched transistors. Currents mirrors are used in constant current biasing circuits. The current mirrors can fabricated either using BJT or MOSFET which are discussed in following sections.

8.5.1 Current Mirror Using BJT

The current mirror using two BJTs is shown in Fig.9 The current mirrors using BJTs will be discussed in two cases with matched and unmatched transistors.

Case-I : When both BJTs are Matched

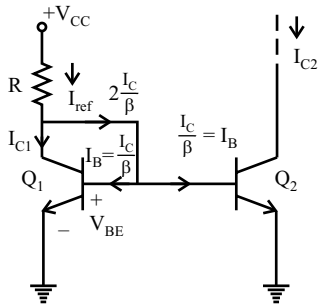


Fig. 9 Current mirror using matched BJTs

When both transistors are matched or identical with $\beta_1 = \beta_2 = \beta$ and $V_{BE1} = V_{BE2} = V_{BE}$. The collector current of both transistors will also be same

i.e. $$I_{C1} = I_{C2} = I_C \quad (54)$$

The reference current can be given by,

$$I_{ref} = \frac{V_{CC} - V_{BE1}}{R} \quad (55)$$

Base current, $$I_{B1} = I_{B2} = I_B = \frac{I_C}{\beta} \quad (56)$$

Reference current in terms of I_{C1},

$$I_{ref} = I_{C1} + 2I_B = I_C + 2 \times \text{—} \quad (57)$$

$$\Rightarrow \quad I_C = \frac{\beta}{\beta + 2} \cdot I_{ref} \quad (58)$$

For a BJT, $\beta >> 2$,

Therefore, $$I_C \approx I_{ref} \quad (59)$$

Current transfer ratio or current gain = $$\frac{I_C}{I_{ref}} = \frac{\beta}{\beta + 2} \approx 1 \quad (60)$$

Case-II : When both BJTs are not Matched

Collector current of two BJTs will be different if Emitter-Base Junction (EBJ) area of both BJTs of the current mirror are different. Fig. 10 shows the circuit of current mirror with unmatched BJTs.

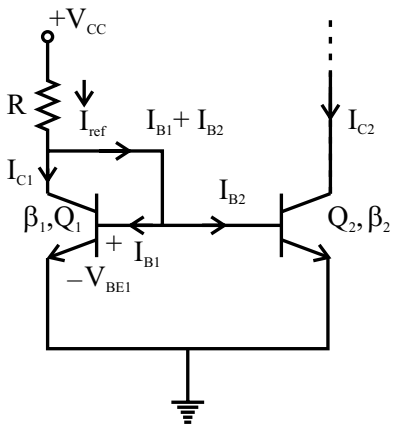


Fig. 10 Current mirror using unmatched BJTs

Let area of EBJ of Q_2 is 'm' times the area of EBJ of Q_1. The collector current of BJT is given by,

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{61}$$

Where, I_S is reverse saturation current, V_{BE} is base to emitter voltage and V_T is thermal voltage.

The reverse saturation current of BJT is given by,

$$I_S = \frac{qA_E D_n n_{Bo}}{W_B} \tag{62}$$

Where, A_E is are of emitter-base junction (EBJ), D_n is diffusion constant of electrons, n_{Bo} is steady state concentration of electrons in p-type base and W_B is widith of base region.

$\Rightarrow$ $I_S \propto A_E$

$\Rightarrow$ $I_C \propto A_E$

If area of EBJ of Q_2 is 'm' times the EBJ of Q_1 then,

$$\frac{I_{C2}}{I_{C1}} = \frac{A_{E2}}{A_{E1}} = m \tag{63}$$

$$\Rightarrow \quad I_{C2} = m\, I_{C1} \tag{64}$$

$$\Rightarrow \quad I_{C1} = \frac{I_{C2}}{m} \tag{65}$$

Base current of Q_2, $$I_{B2} = \frac{I_{C2}}{\beta_2} \tag{66}$$

Base current of Q_1, $$I_{B1} = \frac{I_{C1}}{\beta_1} = \frac{I_{C2}}{m\beta_1} \tag{67}$$

Reference current, $$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{68}$$

$$\Rightarrow \quad I_{ref} = \frac{I_{C2}}{m} + \frac{I_{C2}}{m\beta_1} + \frac{I_{C2}}{\beta_2} \tag{69}$$

$$\Rightarrow \quad I_{C2}=\frac{I_{ref}}{\frac{1}{m}+\frac{1}{m\beta_1}+\frac{1}{\beta_2}} \tag{70}$$

If $\beta_1 = \beta_2 = \beta$ (71)

$$\Rightarrow \quad I_{C2} = \frac{I_{ref}}{\frac{1}{m}+\frac{1}{m\beta}+\frac{1}{\beta}} \tag{72}$$

$$\Rightarrow \quad I_{C2} = \frac{m\, I_{ref}}{1+\frac{1+m}{\beta}} \tag{73}$$

when β is large, $1 + \frac{1+m}{\beta} \approx 1$ (74)

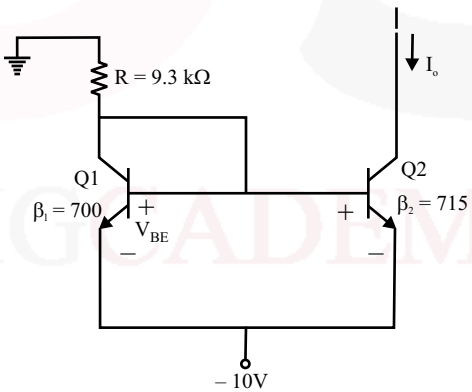
$$\Rightarrow \quad I_{C2} = mI_{ref} \tag{75}$$

The reference current can be given by,

$$I_{ref} = \frac{V_{CC} - V_{BE1}}{R} \tag{76}$$

Example 2

In the silicon BJT circuit shown below, assume that the emitter area of transistor Q1 is half that of transistor Q2.



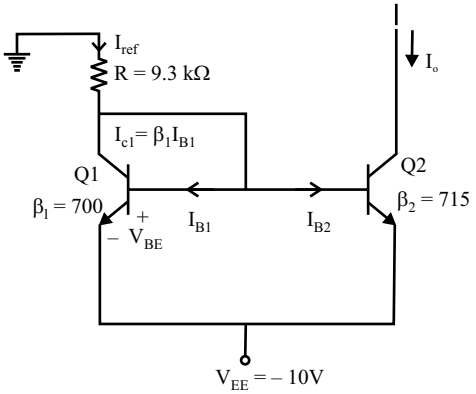
The value of current I_o is approximately.

(a) 0.5 mA (b) 2 mA

(c) 9.3 mA (d) 15 mA

GATE(EC/2010/1M)

Solution : Ans.(b)



$$I_{ref} = \frac{0 - V_{BE} + V_{EE}}{R} = \frac{-0.7 + 10}{9.3k}$$

$$\Rightarrow \quad I_{ref} = \frac{9.3}{9.3k} = 1\,mA$$

Since area of emitter of Q_1 is half of that of Q_2, therefore collector current of Q_1 is half of that of Q_2.

$$\therefore \quad I_{C1} = \frac{1}{2} I_{C2}$$

Base current of Q_2, $$I_{B2} = \frac{I_{C2}}{\beta_2} = \frac{I_{C2}}{715}$$

Base current of Q_1, $$I_{B1} = \frac{I_{C1}}{\beta_1} = \frac{I_{C2}}{2 \times 700}$$

Referance current,

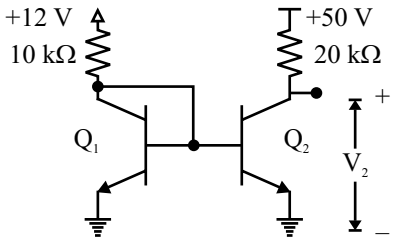
$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$\Rightarrow \quad 1mA = \frac{I_{C2}}{2} + \frac{I_{C2}}{715} + \frac{I_{C2}}{2 \times 700}$$

$$\Rightarrow \quad I_{C2} = \frac{1}{\frac{1}{2} + \frac{1}{715} + \frac{1}{2 \times 700}} mA = 2\ mA$$

Example 3

The matched transistor Q_1 and Q_2 shown in the adjoining figure have $\beta = 100$. Assuming the base-emitter voltage to be 0.7 V, the collector-emitt er voltage V_2 of the transistor Q_2 is

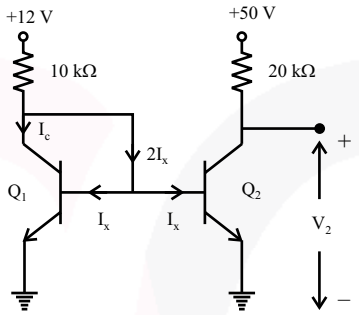


(a) 33.9 V (b) 27.8 V

(c) 16.2 V (d) 0.7 V

GATE(IN/2010/2M)

Solution : Ans.(b)



$12 - 10 \times 10^3 (I_c + 2I_x) - 0.7 = 0$

Collector current, $I_c = \beta I_x = 100\, I_x$

$\Rightarrow \quad I_x = \dfrac{12 - 0.7}{10 \times 10^3 (102)} = 11.078 \text{ mA}$

$\Rightarrow \quad I_c = (11.078 \text{ MA} \times 100 = 1.107 \text{ mA}$

Voltage, $V_2 = 50 - 20 \text{ k } (I_c)$

$\Rightarrow \quad V_2 = 50 - 20 \times 10^3 \times 1.107 \times 10^{-3}$

$\Rightarrow \quad V_2 = 27.8 \text{ V}$

8.5.2 Current Repeater

A basic current mirror can be used to source the current to more than one load as shown in Fig. 11. Such circuit is called current repeater.

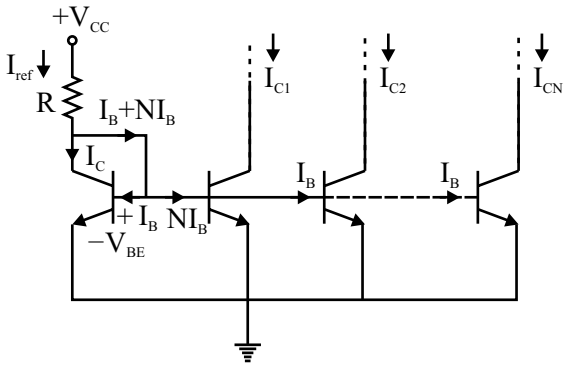


Fig. 11 Current repeater using current mirror

Assumption : All transistor are identical

$$I_{ref} = I_C + I_B + NI_B \tag{77}$$

Base current of each transistor,

$$I_B = \frac{I_C}{\beta} \tag{78}$$

$$\Rightarrow \quad I_{ref} = \left[1 + \frac{1+N}{\beta}\right] I_C \tag{79}$$

$$I_C = \frac{1}{1 + \frac{1+N}{\beta}} I_{ref} \tag{80}$$

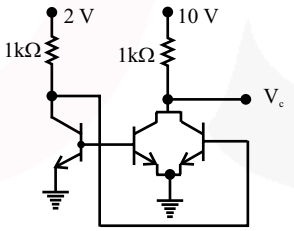
$$\Rightarrow \quad I_C = \frac{\beta}{\beta + 1 + N} \cdot I_{ref} \tag{81}$$

It is possible to achieve different values of I_{C1}, I_{C2} .... I_{CN} by scaling emitter area of Q_1, Q_2 .... Q_N.

Here $$I_{ref} = \frac{V_{CC} - V_{BE}}{R} \tag{82}$$

Example 4

The three transistors in the circuit shown below are identical, with V_{BE}=0.7 V and β = 100.



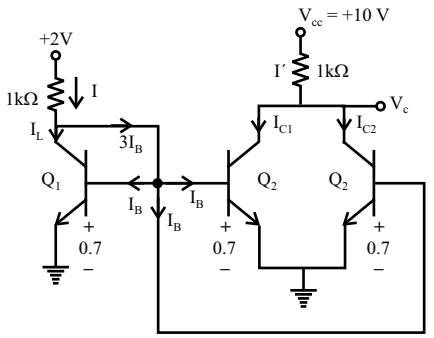
The voltage V_c is

(a) 0.2 V (b) 2 V

(c) 7.4 V (d) 10 V

GATE(IN/2007/2M)

Solution : Ans.(c)



From circuit of Q_1, $I = \frac{2-0.7}{1} = 1.3$ mA

If all BJTs are identical then,

$I = I_C + 3I_B$,

For active region, $I_C = \beta I_B$

$\Rightarrow$ $I = [\beta + 3]\, I_B$

$\Rightarrow$ $I_b = \frac{I}{\beta + 3}$

Given, $\beta = 100$

$\Rightarrow$ $I_B = \frac{1.3}{100+3} = 0.0126$ mA

$\therefore$ $I_{C1} = I_{C2} = \beta I_B = 100 \times 0.0126$ mA

$\Rightarrow$ $I_{C1} = I_{c2} = I_C = 1.262$

Then current, $I' = 2I_C = 2 \times 1.262$ mA

$\Rightarrow$ $I' = 2.524$ mA

The voltage, $V_c = V_{CC} - 2I_C$

$\Rightarrow$ $V_c = 10 - 1 \times 2.524$ V

$\Rightarrow$ $V_c = 7.47$ V

8.5.3 Current Mirror Using MOSFETs

A current mirror using MOSFETs is similar to a current mirror designed using BJTs. Fig. 12 illustrates the current mirror using MOSFETs. It consists of two MOSFETs which may or may not have equal (W/L) ratio of the channels.

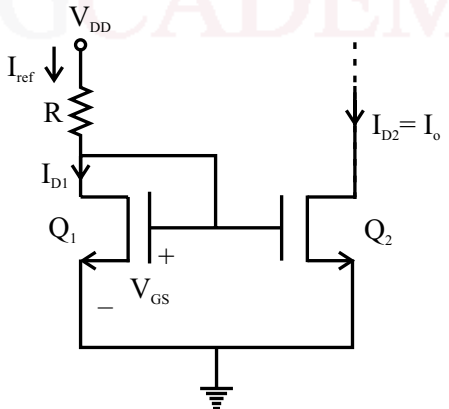


Fig. 12 Current mirror using MOSFETs

Drain current of a MOSFET is given by,

$$I_D = \frac{1}{2}k'\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 \quad (83)$$

where,

W $\rightarrow$ Width of channel

L $\rightarrow$ Length of channel

V_{th} $\rightarrow$ Threshold voltage

$k = \mu_n C_{ox}$ = Transconductance parameter

Reference current of Q_1, $I_{ref} = \frac{V_{DD} - V_{GS}}{R}$ (84)

Since, gate current of MOSFET is zero therefore, drain current of MOSFET Q2 is same as reference current.

$$\therefore \quad I_{D1} = I_{ref} = \frac{V_{DD} - V_{GS}}{R} \quad (85)$$

Case-I : For MOSFETs with same W/L ratios

If both MOSFETs are matching with $(W/L)_2 = (W/L)_1$ then the drain current is same for both the MOSFETs.

$$\therefore \quad I_o = I_{D2} = I_{D1} = I_{ref} \quad (86)$$

$$\Rightarrow \quad \frac{I_o}{I_{ref}} = 1 \quad (87)$$

Case-II : For MOSFETs with different W/L ratios

When MOSFETs have different W/L ratios the drain currents of MOSFETs are related by,

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \quad (88)$$

$$\Rightarrow \quad \frac{I_o}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \quad (89)$$

8.5.4 Wilder Current Source

A wilder current source generates small constant current using relatively small resistors. A resistance R_E is added in emitter circuit of trasistor Q as shown in Fig.13 The output resistance of wilder current source is high.

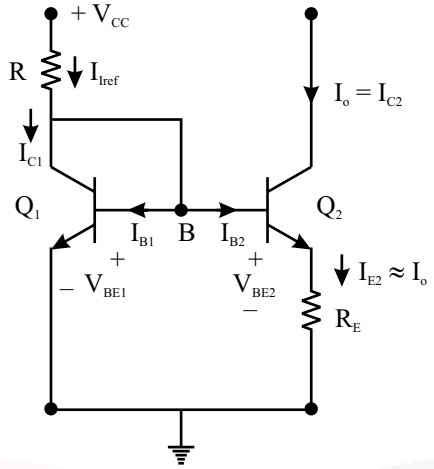


Fig. 13 Wilder Current Source using BJTs

It is assumed that both Q_1 & Q_2 are matched and current gain β of both transistors is large and base currents are negligible.

For negligible base current,

$$I_{ref} = I_{C1} = I_{s1} e^{\frac{V_{BE1}}{V_T}} \quad (90)$$

and

$$I_o = I_{s2} e^{\frac{V_{BE2}}{V_T}} \quad (91)$$

For matched transistors, $I_{S1} = I_{S2}$

$$\Rightarrow \frac{I_o}{I_{ref}} = e^{\frac{V_{BE2} - V_{BE1}}{V_T}} \quad (92)$$

$$\Rightarrow I_o = I_{ref} e^{\frac{V_{BE2} - V_{BE1}}{V_T}} \quad (93)$$

For base circuit of Q_2, we have,

$$V_{BE1} = V_{BE2} + I_o R_E \quad (94)$$

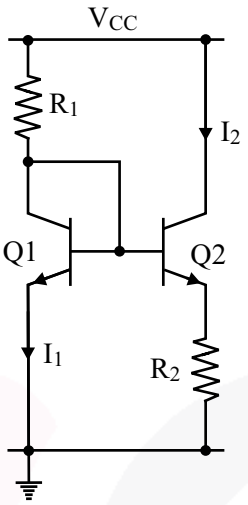
$$\Rightarrow V_{BE2} - V_{BE1} = -I_o R_E \quad (95)$$

$$\Rightarrow I_o = I_{ref} e^{-\frac{I_o R_E}{V_T}} \quad (96)$$

Example 5

Resistor R_1 in the circuit below has been adjusted so that I_1 = 1 mA. The bipolar transistors Q1 and Q2 are perfectly matched and have very high current gain, so their base currents are negligible. The

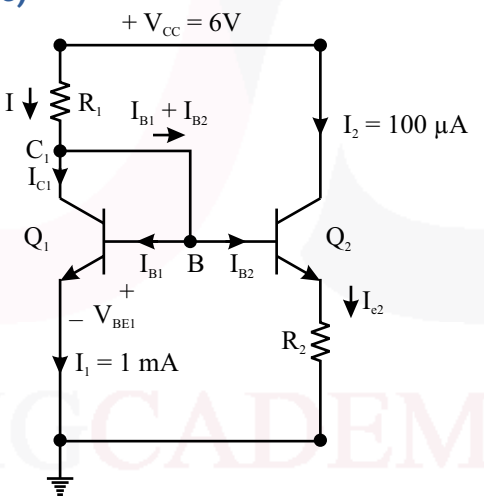
supply voltage V_{CC} is 6 V. The thermal voltage $\frac{kT}{q}$ is 26 mV.



The value of R_2 (in Ω) for which $I_2 = 100\ \mu A$ is .....

GATE(EC-II/2016/1M)

Solution : Ans. (570 to 610)



If β is large, then $I_{B1} = \frac{I_1}{1+\beta} = \text{negligible}$

And $I_{B2} = \frac{I_1}{\beta} = \text{negligible}$

In such case, $I_{C1} \approx I_{e1} = I_1 = 1\ mA$

$I_{e2} \approx I_{C2} = 100\ \mu A$

The collector current of Q_1 is given by

$$I_{C1} = I_{s1} e^{\frac{V_{BE1}}{V_T}}$$

The collector current of Q_2 is given by

$$I_{C2} = I_{s2} e^{\frac{V_{BE2}}{V_T}}$$

For matched transistors, $I_{S1} = I_{S2}$

$$\therefore \quad \frac{I_{C2}}{I_{C1}} = e^{\frac{V_{BE2} - V_{BE1}}{V_T}}$$

$$\Rightarrow \quad V_{BE2} = V_{BE1} + V_T \ell n \frac{I_{C2}}{I_{C1}}$$

Let $V_{BE1} = 0.7\ V$ for Q_1

$$\therefore \quad V_{BE2} = 0.7 + 0.026 \ell n \frac{100 \times 10^{-6}}{1 \times 10^{-3}}$$

Voltage at node B, $V_B = V_{BE1}$

For Base circuit of Q_2,

$$V_{BE1} - V_{BE2} - I_2 R_2 = 0$$

$$R_2 = \frac{V_{BE1} - V_{BE2}}{I_2} = \frac{0.7 - 0.64}{100 \mu A}$$

$$\Rightarrow \quad R_2 = 598.67\ \Omega$$

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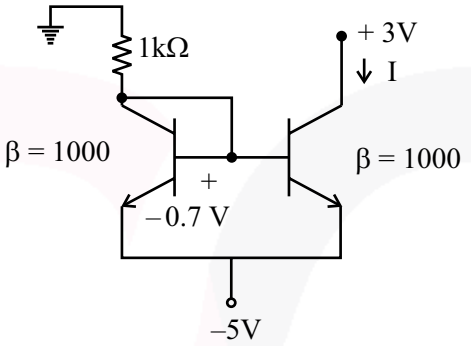
GATE PRACTICE QUESTIONS

Q.1 One of the application of current mirror is

(a) Output current limiting
(b) Obtaining a very high current gain
(c) Current feedback
(d) Temperature stabilized biasing

GATE(EE/1998/1 M)

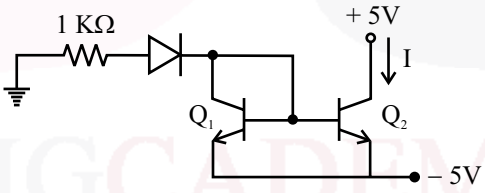
Q.2 Two perfectly matched silicon transistor are connected as shown in figure. The value of the current I is



(a) 0 mA
(b) 2.3 mA
(c) 4.4 mA
(d) 7.3 mA

GATE(EE/2004/1M)

Q.3 Two perfectly matched silicon transistors are connected as shown in the figure. Assuming the β of the transistors to be very high and the forward voltage drop in diodes to be 0.7V, the value of current I is

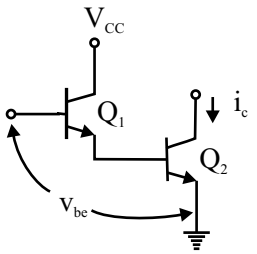


(a) 0 mA
(b) 3.6 mA
(c) 4.3 mA
(d) 5.7 mA

GATE(EE/2008/2 M)

Q.4 A darlington stage is shown in figure If the transconductance of Q_1 is g_{m1} and Q_2 is g_{m2}, then the overall transconductance

$g_{mc}\left[\overset{\Delta}{=}\frac{i_c}{v_{be}}\right]$ is given by



(a) g_{m1} (b) $0.5\ g_{m1}$

(c) g_{m2} (d) $0.5\ g_{m2}$

GATE(EC/1996/2M)

Q.5 A cascode amplifier stage is equivalent to

(a) A common emitter stage followed by a common base stage

(b) A common base stage followed by an emitter follower

(c) An emitter follower stage followed by a common base stage

(d) A common base stage followed by a common emitter stage

GATE(EC/1997/2M)

Q.6 Two identical FETs, each characterized by the parameters g_m and r_d are connected in parallel. The composite FET is then characterized by the parameters

(a) $\frac{g_m}{2}$ and $2r_d$ (b) $\frac{g_m}{2}$ and $\frac{r_d}{2}$

(c) $2g_m$ and $\frac{r_d}{2}$ (d) $2g_m$ and $2r_d$

GATE(EC/1998/1M)

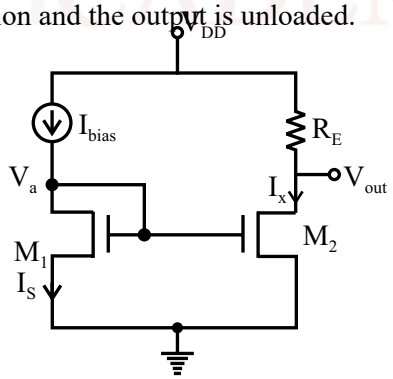
Q.7 The cascode amplifier is a multistage configuration of

(a) CC-CB (b) CE-CB

(c) CB-CC (d) CE-CC

GATE(EC/2005/1M)

Q.8 For the circuit shown in the following figure, transistors M_1 and M_2 are identical NMOS transistors. Assume that M2 is in saturation and the output is unloaded.



The current I_x is related to I_{bias}

(a) $I_x = I_{bias} + I_s$ (b) $I_x = I_{bias}$

(c) $I_x = I_{bias} - I_s$

(d) $I_x = I_{bias} - \left(V_{DD} - \frac{V_{out}}{R_E} \right)$

GATE(EC/2008/2M)

Q.9 Bootsrapping in a buffer amplifier circuit is used for

(a) increasing the input resistance

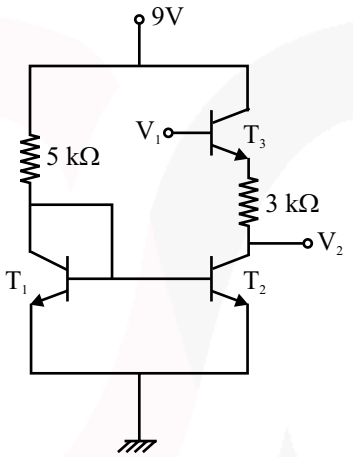
(b) reducing the power consumption

(c) decreasing the output resistance

(d) improving the frequency response

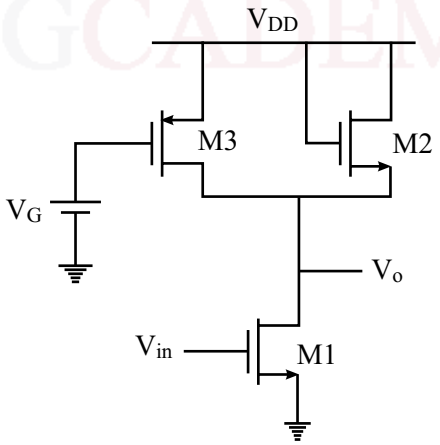
GATE(IN/1999/1M)

Q.10 In the figure, transistors T_1 and T_2 have identical characteristics. $V_{CE\,(sat)}$ of transistor T_3 is 0.1 V. The voltage V_1 is high enough to put T_3 in saturation. Voltage V_{BE} of transistors T_1, T_2 and T_3 is 0.7 V. The value of $(V_1 - V_2)$ in V is_____.



GATE(IN/2014/2M)

Q.11 In the circuit shown in the figure, the channel length modulation of all transistors is non-zero ($\lambda \neq 0$). Also, all transistors operate in saturation and have negligible body effect. The ac small signal voltage gain $\left(\frac{V_o}{V_{in}} \right)$ of the circuit is



(a) $-g_{m1}(r_{o1} \| r_{o2} \| r_{o3})$

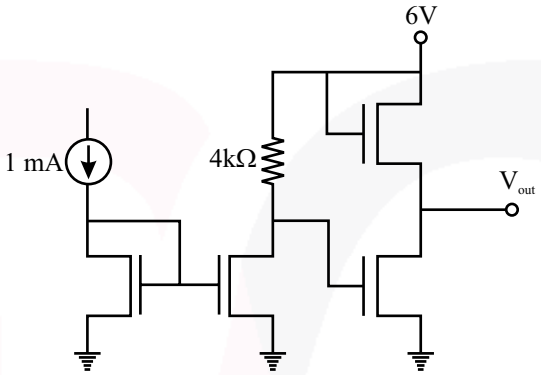
(b) $-g_{m1}\left(r_{o1} \| \frac{1}{g_{m3}} \| r_{o3}\right)$

(c) $-g_{m1}\left(r_{o1} \| \left(\frac{1}{g_{m2}} \| r_{o2}\right) \| r_{o3}\right)$

(d) $-g_{m1}\left(r_{o1} \| \left(\frac{1}{g_{m3}} \| r_{o3}\right) \| r_{o2}\right)$

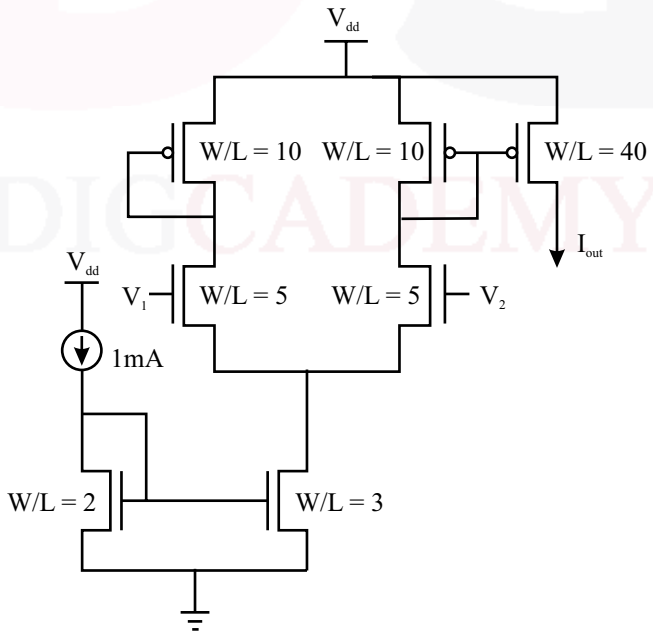
GATE(EC-III/2016/2M)

Q.12 In the circuit shown below, all transistors are n-channel enhancement mode MOSFETs. They are identical and are biased to operate in saturation mode. Ignoring channel length modulation, the output voltage V_{out} is _____V.



GATE(IN/2019/2M)

Q.13 In the circuit shown, V = 0 and $V_2 = V_{dd}$. The other relevant parameters are mentioned in the figure. Ignoring the effect of channel length modulation and the body effect, the value of I_{out} is _____mA (rounded off to 1 decimal place).



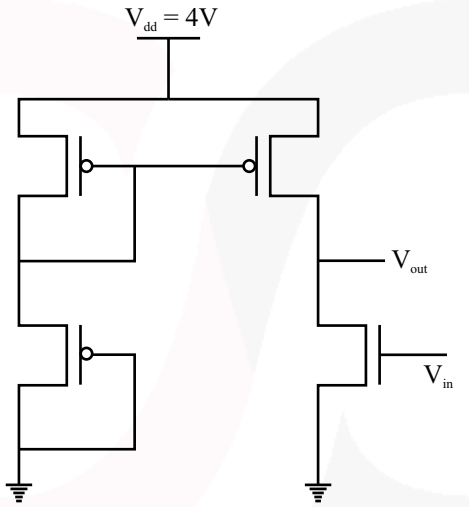
GATE(EC/2019/2M)

Q.14 In the circuit shown, the threshold voltages of the pMOS ($|V_{tp}|$) and nMOS (V_{tn}) transistors are both equal to 1 V. All the transistors have the same output resistance r_{ds} of 6 MΩ. The other parameters are listed below:

$$\mu_n C_{ox} = 60\mu A / V^2; \left(\frac{W}{L}\right)_{nMOS} = 5$$

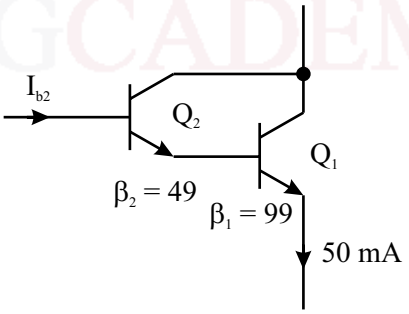
$$\mu_n C_{ox} = 30\mu A / V^2; \left(\frac{W}{L}\right)_{pMOS} = 10$$

μ_n and μ_p are the carrier mobilities, and C_{ox} is the oxide capacitance per unit area. Ignoring the effect of channel length modulation and body bias, the gain of the circuit is _____ (rounded off to 1 decimal place).



GATE(EC/2019/2M)

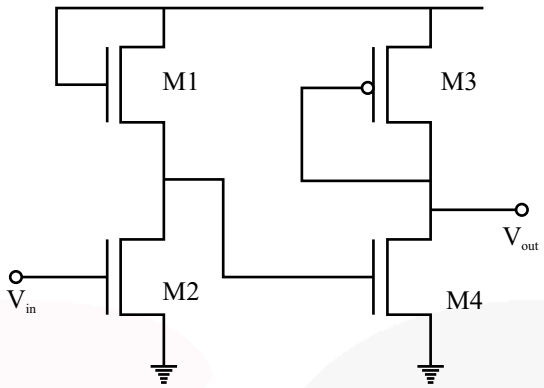
Q.15 The transistor Q_i has a current gain $\beta_i = 99$ and the transistor Q_2 has a current gain $\beta_2 = 49$. The current I_{b2} in microampere is _____.



GATE(IN/2021/1M)

Q.16 A voltage amplifier is constructed using enhancement mode MOSFETs labeled M1, M2, M3 and M4 in the figure below. M1, M2 and M4 are n-channel MOSFETs and M3 is a p-channel MOSFET. All MOSFETs operate in saturation mode and channel length modulation can be ignored. The low frequency, small signal input and output voltages are v_{in} and vout respectively

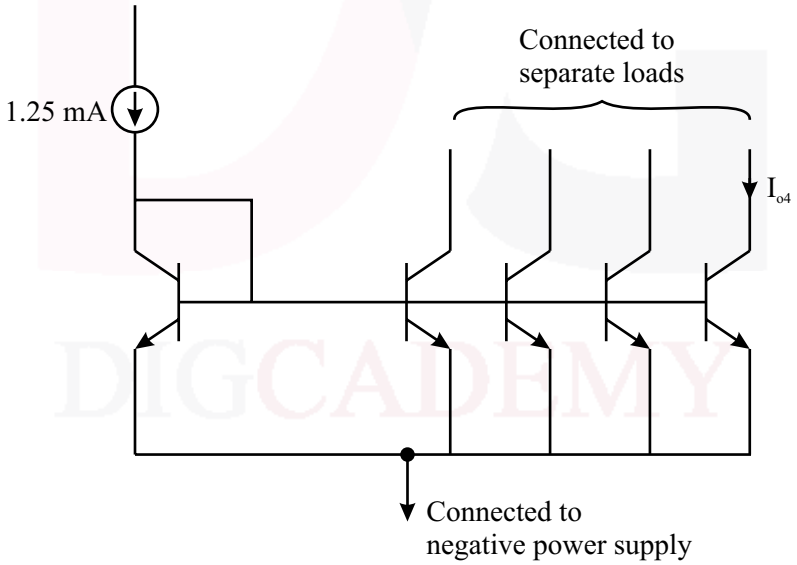
and the dc power supply voltage is V_{DD} . All n-channel MOSFETs have identical transconductance g_{mn} while the p-channel MOSFET has transconductance gmp. The expressions for the low frequency small signal voltage gain v_{out}/v_{in} is



(a) $-g_{mn}/g_{mp}$
(b) $-g_{mn}(g_{mn} + g_{mp})^{-1}$
(c) $+g_{mn}/g_{mp}$
(d) $g_{mn}(g_{mn} + g_{mp})^{-1}$

GATE(IN/2019/2M)

Q.17 All the transistors used in the circuit are matched and have a current gain β of 20. Neglecting the Early effect, the current I_{o4} in milliampere is _____.



GATE(IN/2021/2M)

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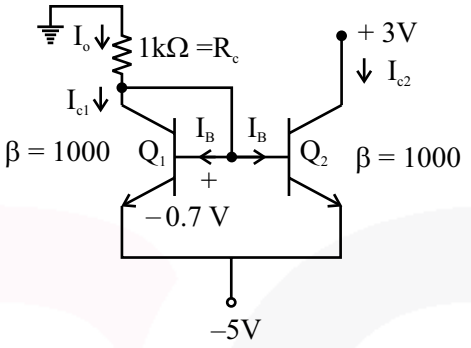
ANSWERS & EXPLANATIONS

Q.1 ***Ans.(d)***

Current mirror is used for temperature stabilized biasing.

Q.2 ***Ans.(c)***



From BJT1,

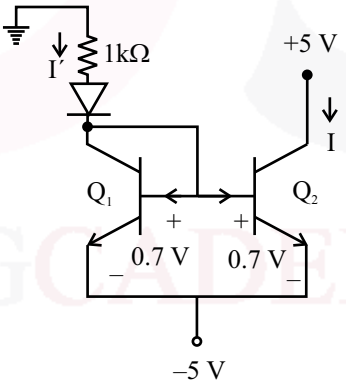
$$1\times10^3\times I_0 + 0.7 - 5 = 0$$

$$I_o = 4.3 \text{ mA}$$

For identical matched BJTs $I_{c1} \approx I_{c2} \approx I_0$

$\therefore$ $I_{c2} \approx 4.3$ mA

Q.3 ***Ans.(b)***



Applying KVL in circuit of transistor Q_1, we have,

$$1 \times I' + 0.7 + 0.7 - 5V = 0$$

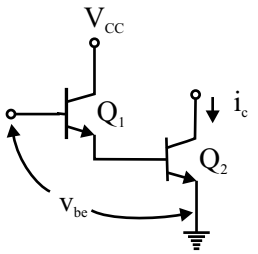
$$I' = 3.6 \text{ mA}$$

The circuit shown above is a current mirror with

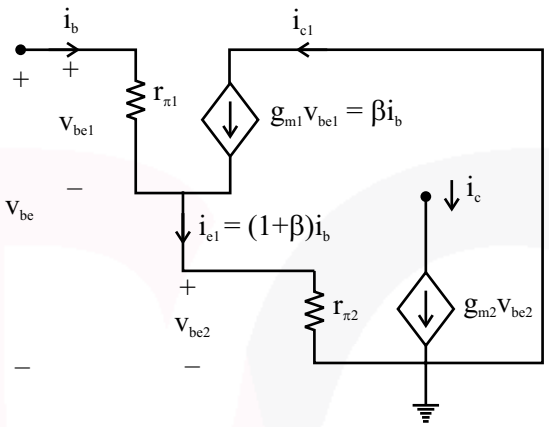
$$I = I'$$

$\therefore$ $I = 3.6$ mA

Q.4 ***Ans.(c)***



Replacing BJT by its a.c. equivalent we have,



Overall transconductance of circuit,

$$g_m = \frac{i_c}{v_{be}} = \frac{i_c}{v_{be1} + v_{be2}} = \frac{g_{m2}v_{be2}}{v_{be1} + v_{be2}}$$

$$v_{be1} = r_{\pi 1} i_b$$

$$v_{be2} = r_{\pi 2}(1 + \beta) i_b$$

$$\therefore \quad g_m = \frac{g_{m2} r_{\pi 2}(1+\beta) i_b}{r_{\pi 1} i_b + r_{\pi 2}(1+\beta) i_b} = \frac{g_{m2} r_{\pi 2}(1+\beta)}{r_{\pi 1} + r_{\pi 2}(1+\beta)}$$

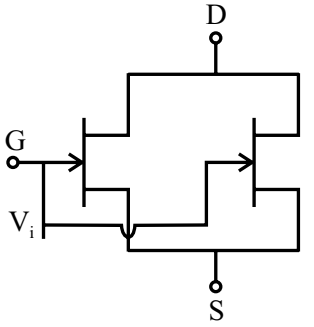
As $\beta >> 1$, therefore, $r_{\pi 2}(1+\beta) >> r_{\pi 1}$

$$\Rightarrow \quad g_m \approx \frac{g_{m2} r_{\pi 2}(1+\beta)}{r_{\pi 2}(1+\beta)} \approx g_{m2}$$

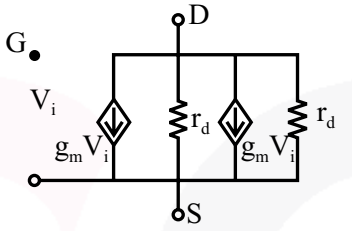
Q.5 ***Ans.(a)***

A cascode amplifier stage is equivalent to a common emitter stage followed by a common base stage.

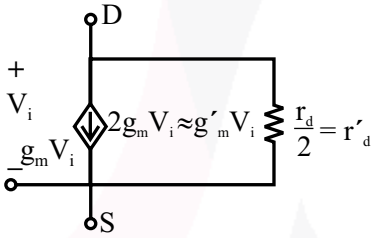
Q.6 ***Ans.(c)***



Replacing Both FETs by their ac equivalent circuits,



Above circuit can be drawn as,



Thus equivalent g_m & r_d of parallel combination of two identical FETs is,

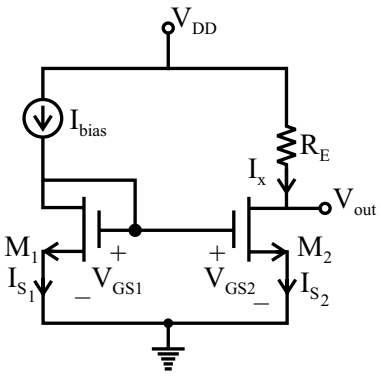
$$g_m' = 2\, g_m$$

$$r_d' = \frac{r_d}{2}$$

Q.7 ***Ans.(b)***

The cascode amplifier is a multistage configuration CE-CB.

Q.8 ***Ans.(b)***



If both transistors are identical,

$$V_{GS1} = V_{GS2}$$

and $$I_{S1} = I_{S2}$$

For MOSFET, drain current in saturation region is given by.

$$I_D = k(V_{GS} - V_T)^2$$

For transistor M_1,

$$I_{D1} = I_{bias} = k(V_{GS} - V_T)^2$$

Since both transistors are identical, therefore,

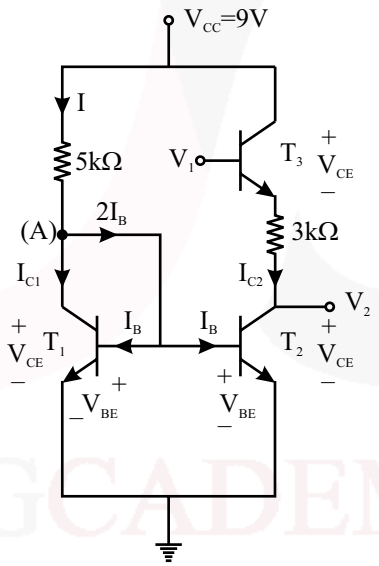
Given, $$I_x = I_{D1} = I_{bias} = k(V_{GS} - V_T)^2$$

Note : *Given circuit is called a current mirror.*

Q.9 Ans.(a)

Bootsraping in a buffer amplifier circuit is used for increasing the input resistance.

Q.10 Ans.5.5 to 5.8



Given, saturation voltage of T_3

$$V_{CE(sat)} = 0.1V$$

Base to emitter voltages of T_1, T_2 & T_3,

$$V_{BE} = 0.7V$$

KVL in collector circuit of T_1,

$$V_{CC} - 5k \times I - V_{CE} = 0$$

For transistor, T_1, $V_{CE} = V_{BE} = 0.7V$

& $$V_{CC} = 9V$$

$\therefore \quad 9 - 5k \times I - 0.7 = 0$

$$I = \frac{8.3}{5}\text{mA} = 1.66\text{ mA}$$

Applying KCL at node (A), we have,

$$I = I_C + 2I_B = I_{C_1} + 2 \times \frac{I_{C_1}}{\beta}$$

If β is large them, $\quad I \approx I_{C1} = 1.66$ mA

Since both transistor T_1 and T_2 are identical, therefore,

$$I_{C2} \approx I_{C1} = 1.66\text{ mA}$$

Voltage, $\quad V_1 = V_{BE} + 3k \times I_{C2} + V_2$

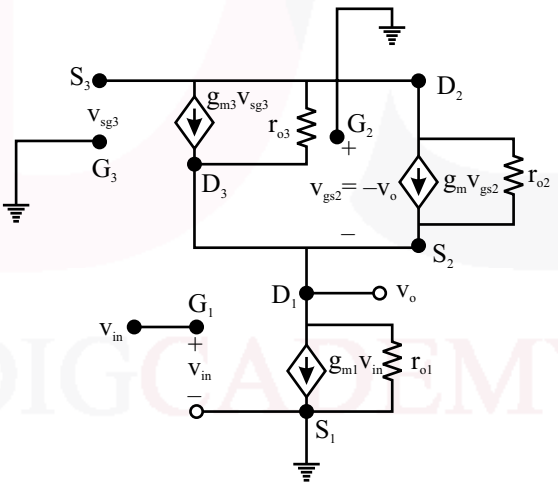
$\Rightarrow \quad V_1 - V_2 = V_{BE} + 3k \times I_{C2}$

$\Rightarrow \quad V_1 - V_2 = 0.7 + 3 \times 1.66$

$\Rightarrow \quad V_1 - V_2 = 5.68\text{V}$

Q.11 Ans. (c)

Replacing MOSFETs by their small signal models, and biasing source by ground & short circuit the AC equivalent of the circuit becomes as shown below,



Applying KCL at node D_1, we have,

$$\frac{v_o}{r_{o3}} + \frac{v_o}{r_{o2}} - g_{m2}v_{gs2} + \frac{v_o}{r_{o1}} + g_{m1}v_{in} = 0$$

Also, $\quad v_{gs2} = -v_o$

$$\Rightarrow \quad \frac{v_o}{r_{o3}} + \frac{v_o}{r_{o2}} - g_{m2}v_o + \frac{v_o}{r_{o1}} + g_{m1}v_{in} = 0$$

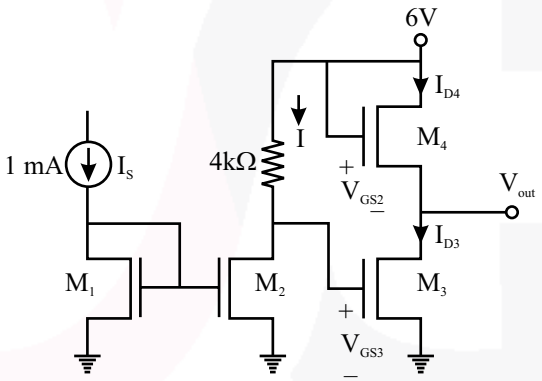
$$\Rightarrow \quad v_o\left[\frac{1}{r_{o1}}+\frac{1}{r_{o2}}+\frac{1}{r_{o3}}+g_{m2}\right]=-g_{m1}v_{in}$$

$$\Rightarrow \qquad \frac{v_o}{v_{in}} = -\frac{g_{m1}}{\frac{1}{r_{o1}}+\frac{1}{r_{o2}}+\frac{1}{r_{o3}}+g_{m2}}$$

Voltage gain, $$A_v = \frac{v_o}{v_{in}} = -\frac{g_{m1}}{\frac{1}{r_{o1}}+\frac{1}{r_{o2}}+\frac{1}{r_{o3}}+g_{m2}}$$

$$\Rightarrow \qquad A_v = -g_{m1}\times\left[r_o \,\|\left(r_{o2}\,\|\frac{1}{g_{m2}}\right)\|\, r_{o3}\right]$$

Q.12 Ans.(4 to 4)



MOSFETs M_1 & M_2 constitute a current mirror. The current I through 4kΩ resistance can be given by using of property of current mirror as under,

$$I = I_s = 1 \text{ mA}$$

Gate to source voltage of M_3,

$$V_{GS3} = 6 - 4k \times I = 6 - 4 \times 1 = 2V$$

Gate to source voltage of M_4,

$$V_{GS4} = 6 - V_{out}$$

Drain current of M_3, in saturation region,

$$I_{D3} = \frac{\mu_n C_{ox}}{2}\cdot\frac{W}{L}\left(V_{GS3}-V_T\right)^2 = \frac{\mu_n C_{ox}}{2}\cdot\frac{W}{L}\left(2-V_T\right)^2$$

Drain current of M_4 in saturation region,

$$I_{D4} = \frac{\mu_n C_{ox}}{2}\cdot\frac{W}{L}\left(V_{GS4}-V_T\right)^2$$

$$\Rightarrow \quad I_{D4} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left(6 - V_{out} - V_T\right)^2$$

As gate current of a MOSFET is zero, so,

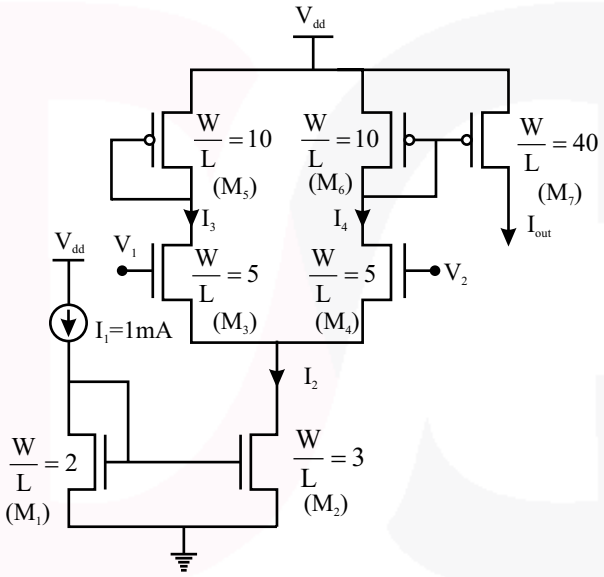
$$I_{D3} = I_{D4}$$

$$\Rightarrow \quad \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left(2 - V_T\right)^2 = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left(6 - V_{out} - V_T\right)^2$$

$$\Rightarrow \quad 2 - V_T = 6 - V_{out} - V_T$$

$$\Rightarrow \quad V_{out} = 6 - 2 = 4V$$

Q.13 Ans.(5.9 to 6.1)



In the given circuit shown above, the transistors M_1 & M_2 and M_6 & M_7 form the current mirrors.

The relation between drain currents of current mirror constituted by transforms M_1 & M_2 is given by

$$\frac{I_2}{I_1} = \frac{\left(\frac{W}{L}\right)_{T2}}{\left(\frac{W}{L}\right)_{T1}} = \frac{3}{2}$$

Given, $I_1 = 1mA$

$$\Rightarrow \quad I_2 = \frac{3}{2} \times I_1 = \frac{3}{2} \times 1 = 1.5mA$$

The transsistor M_3 is off when $V_1 = 0$ and T_4 is off when $V_2 = V_{dd}$

$$\therefore \quad I_3 = 0$$

and $$I_4 = I_2 = 1.5 \text{ mA}$$

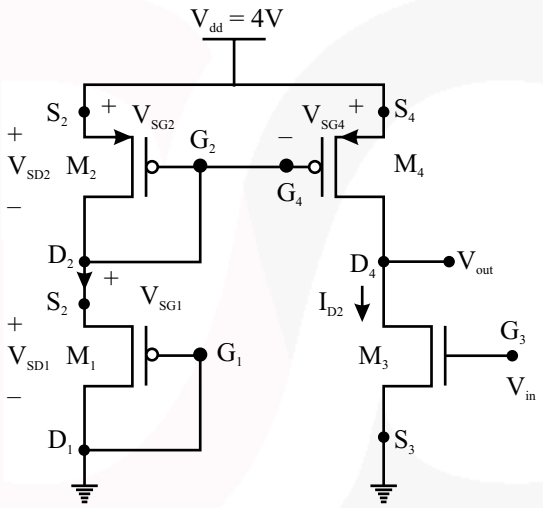
The relation between current mirrors constituted by transistor M_6 & M_7 is given by,

$$\frac{I_{out}}{I_4} = \frac{\left(\frac{W}{L}\right)_{T_7}}{\left(\frac{W}{L}\right)_{T_6}} = \frac{40}{10}$$

$$\Rightarrow \quad I_{out} = \frac{40}{10} \times I_4 = \frac{40}{10} \times 1.5 \text{ mA}$$

$$\Rightarrow \quad I_{out} = 6 \text{ mA}$$

Q.14 Ans.(-905.0 to -895.0 OR 895.0 to 905.0)



Given $\mu_n C_{ox} = 60\mu A/V^2$

$\mu_n C_{ox} = 30\mu A/V^2$

$$\left(\frac{W}{L}\right)_{nMOS} = 5$$

$$\left(\frac{W}{L}\right)_{pMOS} = 10$$

$$|V_{tp}| = V_{tn} = 1V$$

A MOSFET works in saturation region when drain terminal is shorted with the gate terminal . Therefore MOSFETs M_1 & M_2 in the given circuit work in saturation region with drain current,

$$I_{D1} = \frac{\mu_p C_{ox}}{2} \cdot \frac{W}{L}\left(V_{GS} - |V_{tp}|\right)$$

Transconductance of pMOS M_1 & M_2

$$g_{m1} = g_{m2} = \mu_p C_{ox} \frac{W}{L}\left(V_{GS} - |V_{tp}|\right)$$

If both M_1 & M_2 are identical then

$$V_{dd} = V_{SD2} + V_{SD1} = V_{SG2} + V_{SG1} = 2V_{SG}$$

$$\Rightarrow \quad V_{SG} = \frac{V_{dd}}{2} = \frac{4}{2} = 2V$$

$$\therefore \quad g_{m1} = 30 \times 10 \times (2-1)\mu\text{℧}$$

$$g_{m1} = 300\mu\text{℧}$$

Gate to source voltage of M_4,

$$V_{SG4} = V_{dd} - V_{SG1} = 4 - 2 = 2V$$

Transconductance of M_4,

$$g_{m4} = \mu_p C_{ox} \cdot \frac{W}{L}\left(V_{SG} - |V_{tp}|\right)$$

$$\Rightarrow \quad g_{m4} = 30 \times 10 \times (2-1)\ \mu\text{℧}$$

$$\Rightarrow \quad g_{m4} = 300\mu\text{℧}$$

Drain current of M_1 & M_2,

$$I_{D1} = \frac{\mu_p C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{SG1} - |V_{tp}|\right)^2$$

$$\Rightarrow \quad I_{D1} = \frac{30}{2} \times 10(2-1)^2\ \mu A$$

$$\Rightarrow \quad I_{D1} = 150\ \mu A$$

The transistors M_2 & M_4 constitute a current mirror. Applying the property of current mirror, we have,

$$I_{D2} = I_{D1} = 150\ \mu A$$

The drain current of NMOS is given by,

$$I_{D2} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}\left(V_{GS} - V_{tn}\right)^2$$

$$150 = \frac{60}{2} \times 5\left(V_{GS} - 1\right)^2$$

$$\Rightarrow \quad V_{GS} - 1 = 1$$

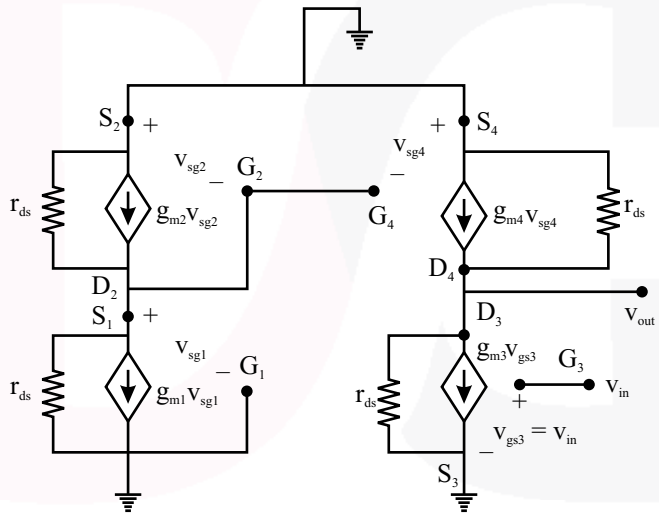
$$V_{GS} = 2V$$

$\therefore$ Transconductance of NMOS,

$$g_{m3} = \mu_n C_{ox} \cdot \frac{W}{L}\left(V_{GS} - V_{tn}\right)$$

$$= 60 \times 5\left(2 - 1\right) = 300\mu\text{ℭ}$$

Replacing PMOS & NMOS of given circuit by their small signal model & basing voltage source by ground the AC equivalent circuit of given network can be drawn as under,



Applying KCL at node D_3, we have,

$$\frac{v_{out}}{r_{ds}} + \frac{v_{out}}{r_{ds}} + g_{m3}v_{in} - g_{m4}v_{sg4} = 0 \qquad \text{.....(i)}$$

$$v_{sg4} = 0 - v_{g4} = -v_{g4}$$

Applying KCL at node G_4, we have,

$$\frac{v_{g4}}{r_{ds}} + \frac{v_{g4}}{r_{ds}} - g_{m2}v_{sg2} + g_{m1}v_{sg1} = 0$$

From the circuit,

$$v_{sg2} = 0 - v_{g2} = 0 - v_{g4} = -\ v_{g4}$$

$$v_{sg1} = v_{s1} - v_{g1} = v_{g4} - 0 = v_{g4}$$

$$\Rightarrow \quad \frac{v_{g4}}{r_{ds}} + \frac{v_{g4}}{r_{ds}} - g_{m2}v_{g4} + g_{m1}v_{g4} = 0$$

$$\Rightarrow \qquad v_{g4} = 0$$

$$\therefore \qquad v_{sg4} = 0 - v_{g4} = 0$$

Putting $v_{sg4} = 0$ in equations (i) we have,

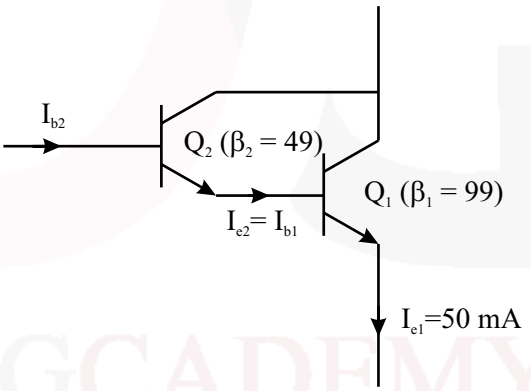
$$\frac{v_{out}}{r_{ds}} + \frac{v_{out}}{r_{ds}} + g_{m3}v_{in} = 0$$

$$\Rightarrow \qquad \frac{v_{out}}{v_{in}} = -\frac{g_{m3}}{\frac{1}{r_{ds}} + \frac{1}{r_{ds}}}$$

$\therefore$ Voltage gain,

$$\Rightarrow \qquad A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m3}r_{ds}}{2} = \frac{300\times10^{-6}\times6\times10^{6}}{2} = -900$$

Q.15 Ans.(10 to 10)



Base current of Q_1 $\quad I_{b1} = \frac{1}{1+\beta_1}\times I_{e1}$

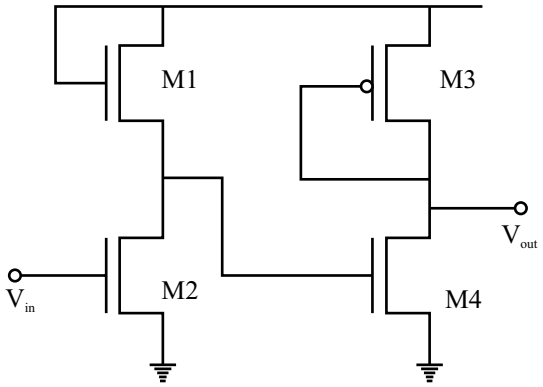
Emitter current of Q_2, $\quad i_{e2} = I_{b1} = \frac{1}{1+\beta_1}\times I_{e1}$

Base current of I_{b2}, $\quad I_{b2} = \frac{1}{1+\beta_2} I_{e2}$

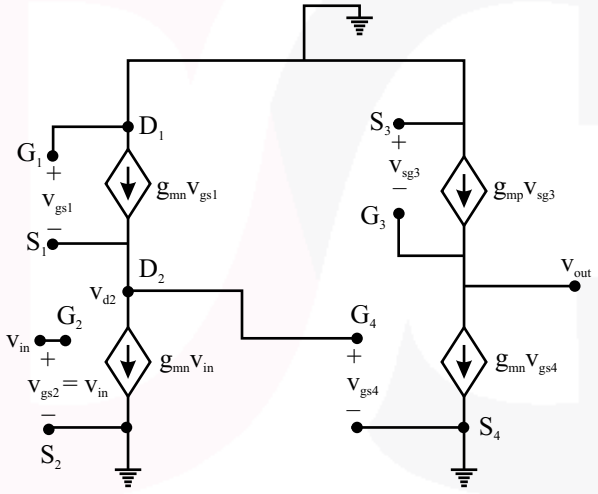
$$\Rightarrow \qquad I_{b2} = \frac{1}{(1+\beta_1)}\times\frac{1}{(1+\beta_2)}\times I_{e1} = \frac{1}{(1+99)(1+49)}\times 50\,\text{mA}$$

$$\Rightarrow \qquad I_{b2} = 10\ \mu\text{A}$$

Q.16 Ans.(c)



Replacing MOSFETs by their small signal models and biasing voltage source by ground, the ac equivalent circuit becomes as under,



From above circuit, $v_{out} = -v_{sg3}$ .....(i)

From M_3 & M_4, $g_{mn}v_{gs4} = g_{mp}v_{sg3}$

$\Rightarrow$ $v_{sg3} = \frac{g_{mn}}{g_{mp}}V_{gs4}$ .....(ii)

Voltage at node D_2, $v_{d2} = v_{qs4} = -v_{gs1}$

$\therefore$ $v_{sg3} = \frac{g_{mn}}{g_{mp}}(-V_{gs1})$ .....(iii)

From M_1 & M_2, $g_{mn}\,v_{in} = g_{mn}\,v_{gs1}$

$\Rightarrow$ $v_{gs1} = v_{in}$ .....(iv)

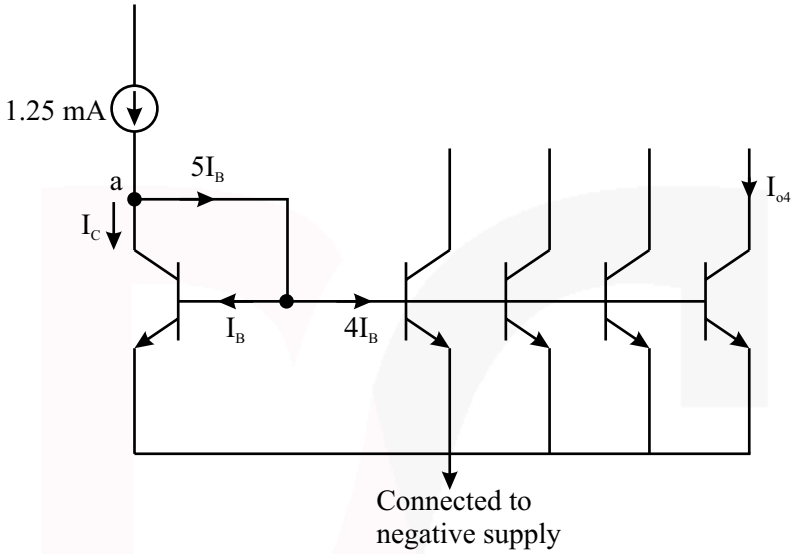
From (i), (iii) & (iv), we have,

$$v_{out} = -\frac{g_{mn}}{g_{mp}}(-V_{in})$$

$$\Rightarrow \quad v_{out} = \frac{g_{mn}}{g_{mp}} V_{in}$$

$$\Rightarrow \quad \frac{V_{out}}{V_{in}} = \frac{g_{mn}}{g_{mp}}$$

Q.17 Ans.(1 to 1)



If all BJTs are matched the base and collector currents are same for all BJTs.

Applying KCL at node 'a' we have,

$$I_C + 5I_B = 1.25$$

$$\Rightarrow \quad I_C + 5\frac{I_C}{\beta} = 1.25$$

Given, $\beta = 20,$

$$\Rightarrow \quad I_C\left(1+\frac{5}{20}\right) = 1.25$$

$$\Rightarrow \quad I_C = \frac{1.25}{5} \times 4 = 1\text{mA}$$

$$\therefore \quad I_{o4} = I_C = 1\text{mA}$$

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About the Author

Dr. Ram Niwas is from Indian Railways Services of Electrical Engineers. He obtained BE degree in Electronics and Power Engineering from NIT(VRCE), Nagpur in 1998, ME degree in Control and Instrumentation Engineering in 2003 and Ph.D in 2015 from IIT, Delhi. He worked with TATA Infotech from January 2000 to June 2000. From August 2000 to December 2001 he worked as lecturer in the Department of Electronics and Communication Engineering in Krishna Institute of Engg. & Tech. Ghaziabad, U. P. From December 2001 to August 2002 he worked in Bharat Sanchar Nigam Limited as Junior Telecom Officer(JTO). Author has vast experience of competitive examinations and has been mentoring the students for cracking various competitive and univsersity examinations for past several years. Author qualified IES examination twice in year 2001 and 2004.

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